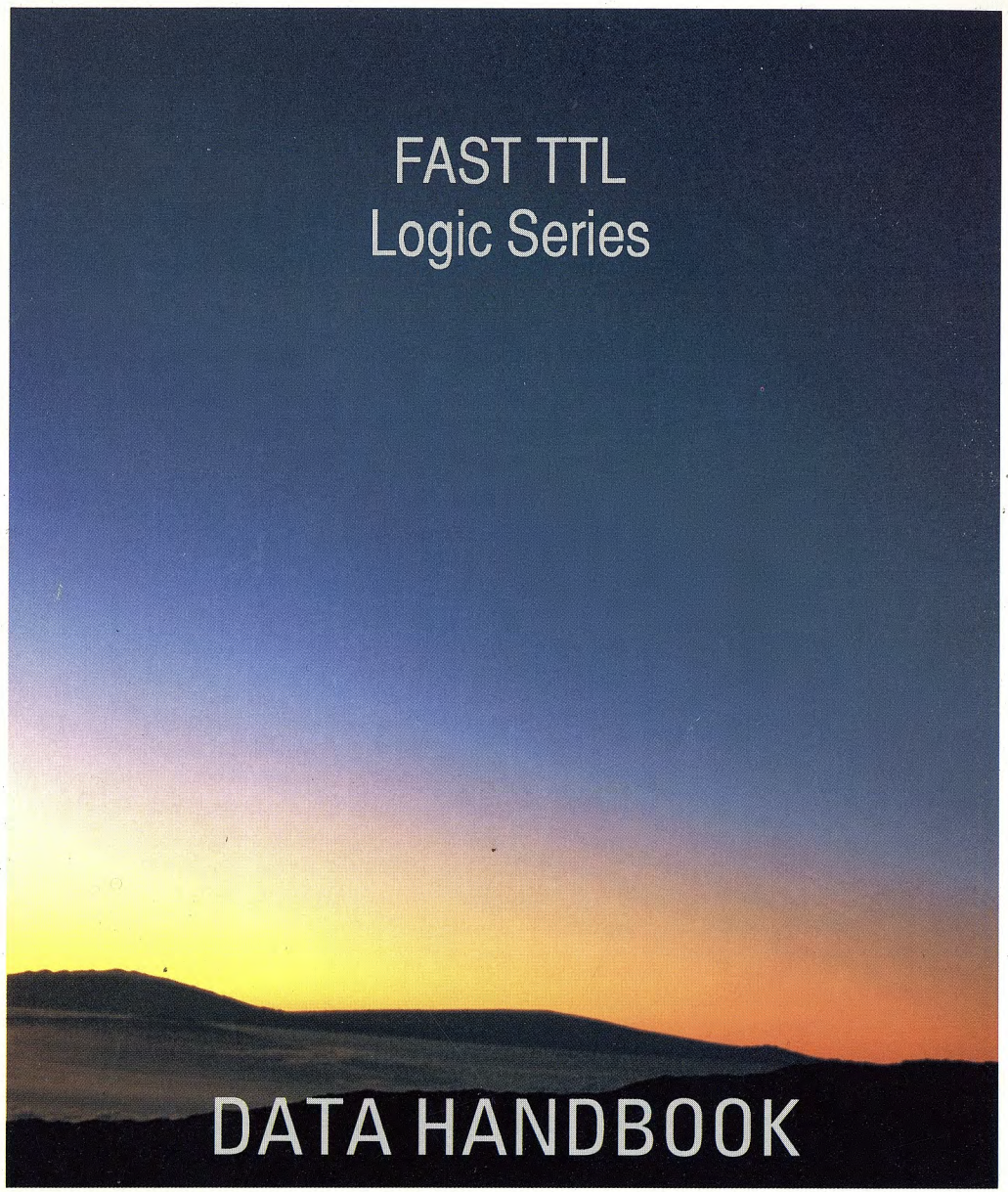

BOOK IC15 1992

Philips Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programs; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility toward the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical,' 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

FAST TTL
Logic Series

Philips Semiconductors

PHILIPS

Preface

FAST TTL Logic from Philips Semiconductors–Signetics

Philips Semiconductors–Signetics would like to thank you for your interest in our FAST product line. Because of its wide customer acceptance, FAST has become the preferred high performance bipolar logic family. With over 230 products in production, Signetics offers the widest selection of FAST products with an emphasis on integrated MSI and LSI solutions.

This 1992 FAST Data Handbook updates the 1989 FAST Data Handbook and 1990 FAST Supplement Handbook. Specifications for several new products have been added, some Preliminary Specifications have been updated to Product Specifications, specifications for a number of industrial temperature grade products (-40° to +85°C) have been added and several products which are being discontinued have been highlighted to alert the user.

Each data sheet contained in this handbook is designed to stand alone and reflect the listed DC and AC specification for a particular product. Each commercial 74F product is specified over a 10% V_{CC} range, both for AC and DC parameters. Additionally, DC specifications for V_{OH} and V_{OL} are provided over the 5% V_{CC} range.

All reference to military products has been deleted, specifically to reflect government requirements imposed by Revision C of MIL-STD 883, including the general provisions of Paragraph 1.2. Specifications for military grade FAST products are available from your nearest Philips Semiconductors–Signetics sales office, sales representative or authorized distributor.

If you require additional information regarding these products, please contact your nearest Philips Semiconductors–Signetics sales office, sales representative or authorized distributor.

PHILIPS SEMICONDUCTORS–SIGNETICS STANDARD PRODUCTS GROUP

Product Status

FAST TTL Logic Series

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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FAST TTL Logic Series

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Introduction

FAST TTL Logic Series

74F FAST TTL Product Description

Signetics has combined advanced oxide-isolated fabrication techniques with standard TTL functions to create a new family designed for the 1980's and '90's. The high operating speeds of FAST can push system operating speeds into areas previously reserved for 10K ECL, but with simple TTL design rules and single 5V power supplies. Low input loading allows the user to mix LS, ALS, and HCMOS in the same system without the need for translators and restrictive fanout requirements.

FAST circuits are pin-for-pin replacements for 74S types. These circuits offer dissipation three to four times lower than the 74S types and higher operating speeds. Existing systems can achieve much lower power and improved performance by replacing the 74S types with the corresponding FAST devices.

The input structure provides better noise immunity because of higher thresholds, while the oxide-isolation and new circuit techniques create devices that have less variation with temperature or supply voltage than existing TTL logic families. Signetics guarantees all AC parameters under realistic system conditions – across the supply voltage spread and the temperature range, and with 50pF output loads.

The use of high-capacitance PNP inputs has been avoided, and clamping diodes have been added to both the inputs and outputs to prevent negative overshoots. High input breakdown voltages allow unused inputs to be tied directly to V_{CC} without pull-up resistors.

Features

- 3ns Propagation delays
- 4mW/gate Power dissipation
- Guaranteed AC performance over temperature and extended V_{CC} range: 5V ±10%
- High impedance NPN base input structure on many types for reduced bus loading in LOW state (I_{IL} = 20μA)
- Standard TTL functions and pinouts
- Replacement for "S" types at 1/4 the power

Introduction

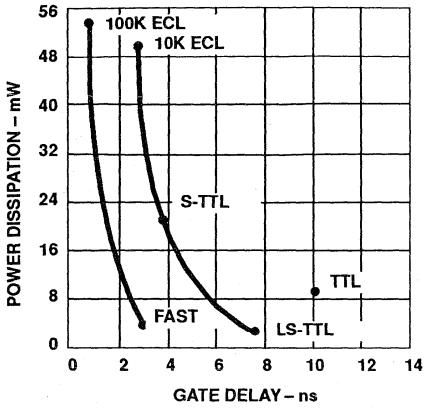


Figure 1. The Speed/Power Spectrum

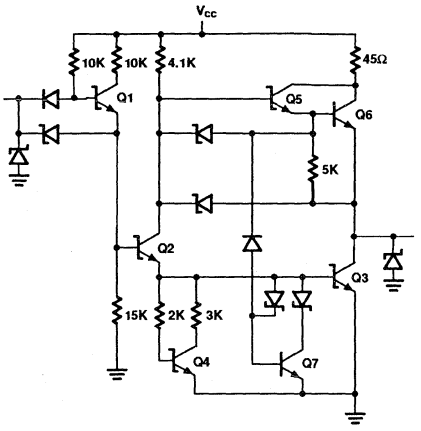


Figure 2. Basic FAST Gate

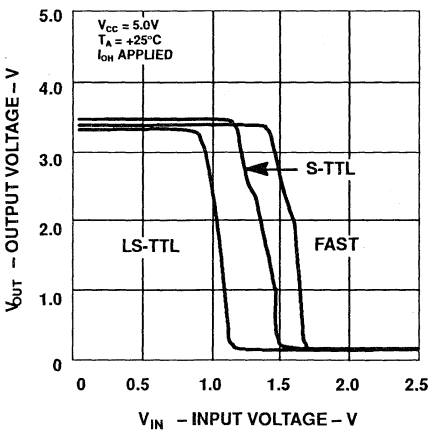


Figure 3. Transfer Functions at Room Temperature

Introduction

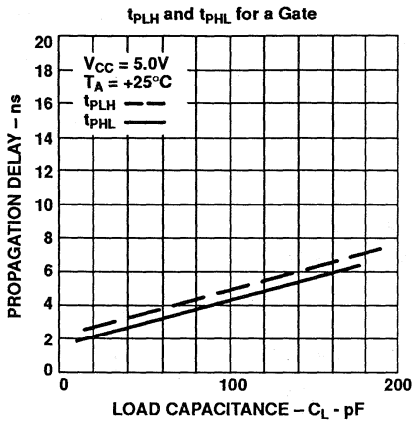


Figure 4. Propagation Delay vs. Load Capacitance (74F00)

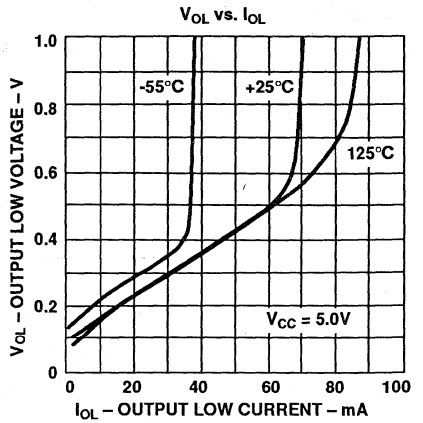


Figure 5. Output LOW Characteristics (74F00)

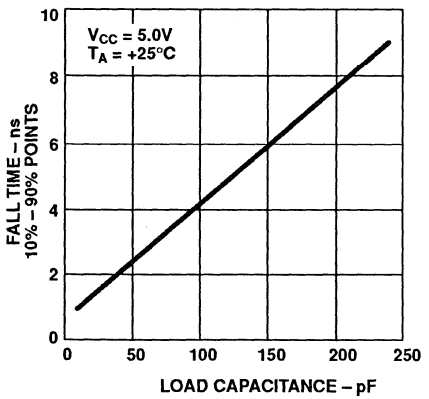


Figure 6. Fall Time vs. Load Capacitance (74F00)

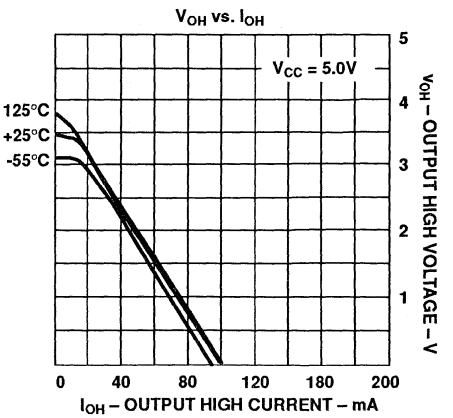


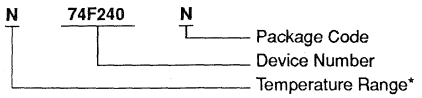
Figure 7. Output HIGH Characteristics (74F00)

Ordering Information

Signetics' commercial FAST products are generally available in both standard dual-in-line and surface mounted options. The ordering code specifies temperature range, device number, and package style as shown below. For commercial products, the standard temperature range is 0°C to 70°C. Available package options are shown on individual data sheets in the "Ordering Code" block. For surface mounted devices the SO plastic dual-in-line package is supplied up to and including 28 pins. Above 28 pins, the plastic leaded chip carrier is utilized.

A wide variety of functions and package options are available for military products. Information on military products is available from the nearest Signetics sales office, sales representative or authorized dealer. The Signetics Military Products Data Manual contains specifications, package and ordering information for all military-grade products.

ORDERING CODE EXAMPLES



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE CODE
Commercial Range: 0°C to 70°C	74FXXX	N = Plastic Dual In-Line Package (DIP) D = Plastic SO DIP (surface mounted) A = Plastic Leaded Chip Carrier (PLCC)
Military Range: -55°C to 125°C	*See Military Products Data Manual*	

* Please note that the temperature range prefix "N" is omitted on the package due to dimensional constraints.

Section 1
Indices

FAST TTL Logic Series

CONTENTS

Availability Guide

DEVICE	NO. OF PINS	DESCRIPTION	AVAILABILITY	
			DIP	SMD
74F00	14	Quad 2-Input NAND Gate	A	SO
74F02	14	Quad 2-Input NOR Gate	A	SO
74F04	14	Hex Inverter	A	SO
74F06	14	Hex Inverter Buffer/Driver (OC)	A	SO
74F06A	14	Hex Inverter Buffer/Driver (OC)	A	SO
74F07	14	Hex Buffer/Driver (OC)	A	SO
74F07A	14	Hex Buffer/Driver (OC)	A	SO
74F08	14	Quad 2-Input AND Gate	A	SO
74F10	14	Triple 3-Input NAND Gate	A	SO
74F11	14	Triple 3-Input AND Gate	A	SO
74F14	14	Hex Inverter Schmitt Trigger	A	SO
74F20	14	Dual 4-Input NAND Gate	A	SO
74F27	14	Triple 3-Input NOR Gate	A	SO
74F30	14	8-Input NAND Gate	A	SO
74F32	14	Quad 2-Input OR Gate	A	SO
74F37	14	Quad 2-Input NAND Buffer (OC)	A	SO
74F38	14	Quad 2-Input NAND Buffer	A	SO
74F40	14	Dual 4-Input NAND Buffer	A	SO
74F51	14	Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gate	A	SO
74F64	14	4-2-3-2 Input AND/OR Gate	A	SO
74F74	14	Dual D-Type Flip-Flop	A	SO
74F85	16	4-Bit Magnitude Comparator	A	SOL
74F86	14	Quad 2-Input Exclusive-OR Gate	A	SO
I74F86	14	Quad 2-Input Exclusive-OR Gate (Industrial)	A	SO
74F109	16	Dual $\overline{JK}$ Positive Edge Triggered Flip-Flop	A	SO
74F112	16	Dual JK Negative Edge Triggered Flip-Flop	A	SO
I74F112	16	Dual JK Negative Edge Triggered Flip-Flop (Industrial)	A	SO
74F113	14	Dual JK Negative Edge Triggered Flip-Flop without Reset	A	SO
74F114	14	Dual JK Negative Edge Triggered Flip-Flop	A	SO
74F125	14	Quad Buffer	A	SO
74F126	14	Quad Buffer	A	SO
74F132	16	Quad 2-Input NAND Schmitt Trigger	A	SO
74F133	16	13-Input NAND Gate	A	SO
74F138	16	1-of-8 Decoder/Demultiplexer	A	SO
74F139	16	Dual 1-of-4 Decoder/Demultiplexer	A	SO
74F148	16	8 Line to 3 Line Priority Encoder	A	SO
74F151A	16	8-Input Multiplexer	A	SO
74F153	16	Dual 4-Input Multiplexer	A	SO
74F154	14	1-of-16 Decoder/Demultiplexer	A	SO
74F157	16	Quad 2-Input Data Selector/Multiplexer NINV	A	SO
74F157A	16	Quad 2-Input Data Selector/Multiplexer NINV	A	SO
74F158	16	Quad 2-Input Data Selector/Multiplexer INV	A	SO
74F158A	16	Quad 2-Input Data Selector/Multiplexer INV	A	SO
74F161A	16	4-Bit Binary Counter, Asynchronous Reset	A	SO
74F163A	16	4-Bit Binary Counter, Synchronous Reset	A	SO
74F164	14	8-Bit Serial/Parallel-In, Serial Out Shift Register	A	SO
74F166	16	8-Bit Bidirectional Universal Shift Register	A	SO
74F169	16	4-Bit Up/Down BCD Binary Synchronous Counter	A	SO
74F173	16	Quad D Flip-Flop (3-State)	A	SO

DEVICE	NO. OF PINS	DESCRIPTION	AVAILABILITY	
			DIP	SMD
74F174	16	Hex D Flip-Flop with Master Reset	A	SO
74F175	16	Quad D Flip-Flop with Master Reset	A	SO
I74F175	16	Quad D Flip-Flop with Master Reset (Industrial)	A	SO
74F181	24	4-Bit Arithmetic Logic Unit	A	SOL
74F182	16	Look Ahead Carry Generator	A	SO
74F189A	16	64-Bit Random Access Memory, INV (3-State)	A	SO
74F191	16	Asynchronous Presettable Up/Down BCD Binary Counter	A	SO
74F193	16	Up/Down BCD Binary Counter with Separate Up/Down Clocks	A	SO
74F194	16	4-Bit Bidirectional Universal Shift Register	A	SO
74F195	16	4-Bit Parallel Access Shift Register	A	SO
74F198	24	8-Bit Bidirectional Universal Shift Register	A	SOL
74F199	24	8-Bit Parallel Access Shift Register	A	SOL
74F219A	16	64-Bit Random Access Memory, NINV (3-State)	A	SO
74F225	20	16 × 5 Asynchronous FIFO (3-State)	A	SO
74F240	20	Octal Inverter Buffer, INV (3-State)	A	SOL
74F241	20	Octal Buffer, NINV (3-State)	A	SOL
74F242	14	Octal Bus Transceiver, INV (3-State)	A	SO
74F243	14	Octal Bus Transceiver, NINV (3-State)	A	SO
74F244	20	Octal Buffer, NINV (3-State)	A	SOL
I74F244	20	Octal Buffer, NINV (3-State) (Industrial)	A	SOL
74F245	20	Octal Transceiver (3-State)	A	SOL
74F251A	16	8-Input Multiplexer (3-State)	A	SO
74F253	16	Dual 4-Input Multiplexer	A	SO
74F256	16	Dual Addressable Latch	A	SO
74F257A	16	Quad 2-Line to 1-Line Selector/Multiplexer, NINV (3-State)	A	SO
74F258A	16	Quad 2-Line to 1-Line Selector/Multiplexer, INV (3-State)	A	SO
74F259	16	8-Bit Addressable Latch	A	SO
74F260	14	Dual 5-Input NOR Gate	A	SO
74F269	24	8-Bit Bidirectional Binary Counter (3-State)	A	SO
74F273	20	Octal D Flip-Flop	A	SOL
74F280A	14	9-Bit Odd/Even Parity Generator/Checker	A	SO
74F280B	14	9-Bit Odd/Even Parity Generator/Checker (Higher Speed 74F280A)	A	SO
I74F280B	14	9-Bit Odd/Even Parity Generator/Checker (Higher Speed 74F280A) (Industrial)	A	SO
74F283	16	4-Bit Binary Adder with Fast Carry	A	SO
74F298	16	Quad 2-Input Multiplexer with Storage	A	SO
74F299	20	8-Bit Universal Shift/Storage Register (3-State)	A	SOL
74F322	20	8-Bit Serial/Parallel Register with Sign Extend (3-State)	A	SOL
74F323	20	8-Bit Universal Shift/Storage Register with Sync Reset and Common I/O Pins (3-State)	A	SOL
74F350	16	4-Bit Shifter	A	SO
74F353	16	Dual 4-Input Multiplexer (Inverted 74F253)	A	SO
74F365	16	Hex Buffer Driver (3-State)	A	SO
74F366	16	Hex Inverter (3-State)	A	SO
74F367	16	Hex Buffer Driver (3-State)	A	SO
74F368	16	Hex Inverter Driver (3-State)	A	SO
74F373	20	Octal Transparent Latch (3-State)	A	SO
74F374	20	Octal D Flip-Flop (3-State)	A	SO
74F377	20	Octal D Flip-Flop with Enable	A	SO
74F378	16	Hex D Flip-Flop with Enable	A	SO
74F379	16	Quad D Flip-Flop with Enable	A	SO

DEVICE	NO. OF PINS	DESCRIPTION	AVAILABILITY	
			DIP	SMD
74F381	20	4-Bit Arithmetic Logic Unit	A	SOL
74F382	20	4-Bit Arithmetic Logic Unit	A	SOL
74F385	20	Quad Serial Adder/Subtractor	A	SOL
74F393	16	Dual 4-Bit Binary Ripple Counter	A	SO
74F395	16	4-Bit Cascadable Shift Register (3-State)	A	SO
74F398	20	Quad 2-Port Register with True and Complementary Outputs	A	SOL
74F399	16	Quad 2-Port Register	A	SO
74F410	18	Register Stack – 16 × 4 RAM 3-State Output Register (3-State)	A	
74F455	24	Octal Buffer with Parity Generator Checker, INV (3-State)	A	SOL
74F456	24	Octal Buffer with Parity Generator Checker, NINV (3-State)	A	SOL
74F521	20	Octal Identity Comparator	A	SOL
74F524	20	8-Bit Register Comparator (OC + 3-State)	A	SOL
74F533	20	Octal Transparent Latch,, INV (3-State)	A	SOL
74F534	20	Octal D Flip-Flop, INV (3-State)	A	SOL
74F537	20	1-of-10 Decoder (3-State)	A	SOL
74F538	20	1-of-8 Decoder (3-State)	A	SOL
74F539	20	Dual 1-of-4 Decoder (3-State)	A	SOL
74F540	20	Octal Inverted Buffer (3-State) (Broadside Pin-out of 74F240)	A	SOL
74F541	20	Octal Buffer (3-State) (Broadside Pin-out of 74F244)	A	SOL
74F543	24	Octal Registered Transceiver, NINV (3-State)	A	SOL
74F544	24	Octal Registered Transceiver, INV (3-State)	A	SOL
74F545	20	Octal Bidirectional Transceiver with 3-State Inputs/Outputs, NINV	A	SOL
74F552	28	Octal Registered Transceiver with Parity and Status Flags, NINV (3-State)	A	SOL
74F564	20	Octal D Flip-Flop (3-State) (Broadside Pin-out of 74F534)	A	SOL
74F569	20	4-Bit Bidirectional Binary Synchronous Counter	A	SOL
74F573	20	Octal Transparent Latch (3-State) (Broadside Pin-out of 74F373)	A	SOL
74F574	20	Octal D Flip-Flop (3-State) (Broadside Pin-out of 74F374)	A	SOL
74F579	20	8-Bit Bidirectional Binary Counter (3-State)	A	SOL
74F595	16	8-Bit Shift Register with Output Latches (3-State)	A	SO
74F597	16	8-Bit Shift Register with Input Latches	A	SO
74F598	20	8-Bit Shift Register with Input Latches (3-State)	A	SOL
74F604	28	Dual Octal Register (3-State)	A	SOL
74F620	20	Octal Bus Transceiver, INV (3-State)	A	SOL
74F621	20	Octal Bus Transceiver, NINV (OC)	A	SOL
74F623	20	Octal Bus Transceiver, NINV (3-State)	A	SOL
74F640	20	Octal Bus Transceiver, INV (3-State)	A	SOL
74F641	20	Octal Bus Transceiver with Common Output Enable, NINV (OC)	A	SOL
74F642	24	Octal Bus Transceiver with Common Output Enable, INV (OC)	A	SOL
74F646	24	Octal Bus Transceiver/Register, NINV (3-State)	A	SOL
74F646A	24	Octal Bus Transceiver/Register, NINV (3-State)	A	SOL
74F647	24	Octal Bus Transceiver/Register, NINV (OC)	A	SOL
74F648	24	Octal Bus Transceiver/Register, INV (3-State)	A	SOL
74F648A	24	Octal Bus Transceiver/Register, INV (3-State)	A	SOL
74F649	24	Octal Bus Transceiver/Register, INV (OC)	A	SOL
74F651	24	Octal Bus Transceiver/Register, INV (3-State)	A	SOL
74F651A	24	Octal Bus Transceiver/Register, INV (3-State)	A	SOL
74F652	24	Octal Bus Transceiver/Register, NINV (3-State)	A	SOL
74F652A	24	Octal Bus Transceiver/Register, NINV (3-State)	A	SOL
74F653	24	Octal Bus Transceiver/Register, INV (3-State + OC)	A	SOL

Availability Guide

DEVICE	NO. OF PINS	DESCRIPTION	AVAILABILITY	
			DIP	SMD
74F655A	24	Octal Buffer/Driver with Parity, INV (3-State)	A	SOL
I74F655A	24	Octal Buffer/Driver with Parity, INV (3-State) (Industrial)	A	SOL
74F656A	24	Octal Buffer/Driver with Parity, NINV (3-State)	A	SOL
I74F656A	24	Octal Buffer/Driver with Parity, NINV (3-State) (Industrial)	A	SOL
74F657	24	Octal Transceiver with 8-Bit Parity Generator/Checker (3-State)	A	SOL
I74F657	24	Octal Transceiver with 8-Bit Parity Generator/Checker (3-State) (Industrial)	A	SOL
74F670	16	4 × 4 Register File	A	SOL
74F674	24	16-Bit Serial/Parallel-In, Serial-Out Shift Register (3-State)	A	SOL
74F676	24	16-Bit Parallel-In, Serial-Out Shift Register (3-State)	A	SOL
74F711A	20	Quint 2-to-1 Data Selector Multiplexer (3-State)	A	SOL
74F711-1	20	Quint 2-to-1 Data Selector Multiplexer with 30Ω Series Termination Resistors	A	SOL
74F712A	24	Quint 3-to-1 Data Selector Multiplexer (3-State)	A	SOL
74F712-1	24	Quint 3-to-1 Data Selector Multiplexer with 30Ω Series Termination Resistors	A	SOL
74F723A	24	Quint 3-to-1 Data Selector Multiplexer (3-State)	A	SOL
74F723-1	24	Quint 3-to-1 Data Selector Multiplexer with 30Ω Series Termination Resistors	A	SOL
74F725A	24	Quint 4-to-1 Data Selector Multiplexer (3-State)	A	SOL
74F725-1	24	Quint 4-to-1 Data Selector Multiplexer with 30Ω Series Termination Resistors	A	SOL
74F733	20	Quad Data Multiplexer, INV	A	SOL
74F756	20	Octal Inverter Buffer, INV (Open Collector 74F240)	A	SOL
74F757	20	Octal Buffer, NINV (Open Collector 74F241)	A	SOL
74F760	24	Octal Buffer, NINV (Open Collector 74F244)	A	SOL
74F764-1	40	DRAM Dual Ported Controller with Latch	A	PLCC
74F765-1	40	DRAM Dual Ported Controller without Latch	A	PLCC
74F776	28	Octal Bidirectional Latched Pi-Bus Transceiver (3-State + OC)	A	SOL/P
I74F776	28	Octal Bidirectional Latched Pi-Bus Transceiver (3-State + OC) (Industrial)	A	SOL/P
74F779	16	8-Bit Bidirectional Counter (3-State)	A	SOL
74F786	16	4-Input Asynchronous Bus Arbiter	A	SOL
74F804	20	Hex 2-Input NAND Driver	A	SOL
74F805	24	Hex 2-Input NOR Driver	A	SOL
74F807	28	Octal Shift/Count Transceiver with Adder and Parity	A	SOL/PLCC
74F808	20	Hex 2-Input AND Driver	A	SOL
74F821	20	10-Bit Interface Register, NINV (3-State)	A	SOL
74F822	24	10-Bit Interface Register, INV (3-State)	A	SOL
74F823	24	9-Bit Interface Register, NINV (3-State)	A	SOL
74F824	24	9-Bit Interface Register, INV (3-State)	A	SOL
74F825	24	8-Bit Interface Register, NINV (3-State)	A	SOL
74F826	24	8-Bit Interface Register, INV (3-State)	A	SOL
74F827	24	10-Bit Buffer/Line Driver, NINV (3-State)	A	SOL
74F828	24	10-Bit Buffer/Line Driver, INV (3-State)	A	SOL
74F832	20	Hex 2-Input OR Driver	A	SOL
74F835	24	8-Bit Shift Register with 2:1 Multiplexer-In, Latched "B" Inputs & Serial-Out	A	SOL
74F841	20	10-Bit Bus Interface Latch, NINV (3-State)	A	SOL
74F842	24	10-Bit Bus Interface Latch, INV (3-State)	A	SOL
74F843	24	9-Bit Bus Interface Latch, NINV (3-State)	A	SOL
74F844	24	9-Bit Bus Interface Latch, INV (3-State)	A	SOL
74F845	24	8-Bit Bus Interface Latch, NINV (3-State)	A	SOL
74F846	24	8-Bit Bus Interface Latch, INV (3-State)	A	SOL
74F861	24	10-Bit Bus Transceiver, NINV (3-State)	A	SOL
74F862	24	10-Bit Bus Transceiver, INV (3-State)	A	SOL

DEVICE	NO. OF PINS	DESCRIPTION	AVAILABILITY	
			DIP	SMD
74F863	24	9-Bit Bus Transceiver, NINV (3-State)	A	SOL
74F864	24	9-Bit Bus Transceiver, INV (3-State)	A	SOL
74F1240	20	Octal Inverter Buffer (3-State), Light Load 74F240	A	SOL
74F1241	20	Octal Buffer (3-State), Light Load 74F241	A	SOL
74F1243	14	Quad Transceiver (3-State), Light Load 74F243	A	SOL
74F1244	20	Octal Buffer (3-State), Light Load 74F244	A	SOL
74F1245	20	Octal Bus Transceiver (3-State), Light Load 74F245	A	SOL
74F1604	28	Dual Octal Latch	A	SOL
74F1762	40	4-MBit Memory Address Controller	A	PLCC
74F1763	48	1-MBit Intelligent DRAM Controller	A	PLCC
74F1764	48	1-MBit DRAM Dual Ported Controller with Latch	A	PLCC
74F1764-1	48	1-MBit DRAM Dual Ported Controller with Latch	A	PLCC
74F1765	48	1-MBit DRAM Dual Ported Controller without Latch	A	PLCC
74F1765-1	48	1-MBit DRAM Dual Ported Controller without Latch	A	PLCC
74F1766	48	Burst Mode DRAM Controller	A	PLCC
74F1779	16	8-Bit Up/Down Counter, Common I/O (3-State), Extended Function of 74F779	A	SOL
74F1804	20	Hex 2-Input NAND Driver (Center Power Pin 74F804)	A	SOL
74F1805	20	Hex 2-Input NOR Driver (Center Power Pin 74F805)	A	SOL
74F1808	20	Hex 2-Input AND Driver (Center Power Pin 74F808)	A	SOL
74F1832	20	Hex 2-Input OR Driver (Center Power Pin 74F832)	A	SOL
74F2952	24	Octal Transceiver, NINV (3-State)	A	SOL/PLCC
74F2953	24	Octal Transceiver, INV (3-State)	A	SOL/PLCC
74F3037	16	Quad 2-Input 30Ω Line Drive, NINV	A	SOL
I74F3037	16	Quad 2-Input 30Ω Line Drive, NINV (Industrial)	A	SOL
74F3038	16	Quad 2-Input 30Ω Line Drive, NINV (OC)	A	SOL
74F3040	16	Dual 4-Input 30Ω Line Drive, NINV	A	SOL
74F3893	20	Quad Futurebus Backplane Transceiver (3-State + OC)	A	PLCC
74F5074	14	Synchronizing Dual D-Type Flip-Flop	A	SO
74F5300	8	LED Driver		SO
74F8960	28	Octal Latched Bidirectional Futurebus Transceiver, INV (OC)	A	PLCC
74F8961	28	Octal Latched Bidirectional Futurebus Transceiver, NINV (OC)	A	SOL/PLCC
74F30240	24	Octal 30Ω Transmission Line/Backplane Driver, INV (OC)	A	SOL
74F30244	24	Octal 30Ω Transmission Line/Backplane Driver, NINV (OC)	A	SOL
74F50109	16	Synchronizing Dual D-Type Flip-Flop	A	SO
74F50728	14	Synchronizing Cascaded Dual D-Type Flip-Flop	A	SO
74F50729	16	Synchronizing Dual D-Type Flip-Flop with Edge Triggered Set & Reset	A	SO

Discontinued Products

DISCONTINUED PRODUCTS

74F13
74F83
74F151
74F160A
74F162A
74F168
74F190
74F192
74F251
74F257
74F258
74F352
74F412
74F432
74F547
74F548
74F563
74F568
74F582
74F583
74F588
74F605
74F622
74F654
74F657A
74F732
74F755
74F764
74F765
74F881
74F882
74F1242
74F1760
74F30245
74F30640

Function Selection Guide

GATES

FUNCTION		DEVICE NUMBER
Inverters	Hex Inverter	74F04
	Hex Inverter, Schmitt Trigger	74F14
NAND	Quad 2-Input	74F00
	Triple 3-Input	74F10
	Dual 4-Input	74F20
	8-Input	74F30
	Quad 2-Input, Schmitt Trigger	74F132
	13-Input	74F133
AND	Quad 2-Input	74F08
	Triple 3-Input	74F11
NOR	Quad 2-Input	74F02
	Triple 3-Input	74F27
	Dual 5-Input	74F260
OR	Quad 2-Input	74F32
Exclusive-OR	Quad 2-Input	74F86
Combination Gates	Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-Invert	74F51
	4-2-3-2 Input AND-OR	74F64

GATES

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	RESET	METASTABLE IMMUNITY
Dual D	74F74	↑	Low	Low	
Dual D	74F5074	↑	Low	Low	Yes
Dual D	74F50728	↑	Low	Low	Yes
Dual D	74F50729	↑	High	High	Yes
Dual $\overline{JK}$	74F109	↑	Low	Low	
Dual $\overline{JK}$	74F50109	↑	Low	Low	Yes
Dual JK	74F112/I74F112	↓	Low	Low	
Dual JK	74F113	↓	Low	Low	
Dual JK	74F114	↓	Low	Low	

MULTIPLE FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	RESET	OUTPUT
Quad D	74F173	↑	High	NINV
Quad D with Master Reset	74F175/I74F175	↑	Low	NINV INV
Quad D with Enable	74F379	↑		NINV INV
Hex D with Master Reset	74F174	↑	Low	NINV
Hex D with Enable	74F378	↑		NINV
Octal D	74F273	↑	Low	NINV
Octal D, 3-State	74F374	↑		NINV
Octal D, 3-State	74F534	↑		INV
Octal D with Enable	74F377	↑		NINV
Octal D, 3-State	74F564	↑		INV
Octal D, 3-State	74F574	↑		NINV

OTHER REGISTERS, REGISTER FILES

FUNCTION	DEVICE NUMBER	CLOCK EDGE	PARALLEL ENTRY	BITS
Quad 2 Port, NINV, INV	74F398	↑	2D (Mux)	4 × 2
Quad 2 Port, NINV	74F399	↑	2D (Mux)	4 × 2
Dual Octal, 3-State	74F604	↑	8D	8
Register File	74F670	↑	2D	4 × 4
10-Bit, NINV, 3-State	74F821	↑	2D	10
10-Bit, INV, 3-State	74F822	↑	2D	10
9-Bit, NINV, 3-State	74F823	↑	2D	9
9-Bit, INV, 3-State	74F824	↑	2D	9
8-Bit, NINV, 3-State	74F825	↑	2D	8
8-Bit, INV, 3-State	74F826	↑	2D	8

LATCHES

FUNCTION	DEVICE NUMBER	ENABLE LEVEL	RESET LEVEL	OUTPUT
Dual Addressable	74F256	1 (Low)	Low	NINV
Dual Octal Latch	74F1604	1 (Low)		NINV
Octal Transparent, 3-State	74F373	1 (High)		INV
Octal Transparent, 3-State (Broadside version of 74F373)	74F533	1 (High)		INV
Octal Transparent, 3-State (Broadside version of 74F373)	74F573	1 (High)		NINV
8-Bit Addressable	74F259	1 (High)	Low	NINV
8-Bit Interface, 3-State	74F845	1 (High)	Low	NINV
8-Bit Interface, 3-State	74F846	1 (High)	Low	INV
9-Bit Interface, 3-State	74F843	1 (High)	Low	NINV
9-Bit Interface, 3-State	74F844	1 (High)	Low	INV
10-Bit Interface, 3-State	74F841	1 (High)		NINV
10-Bit Interface, 3-State	74F842	1 (High)		INV

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ENABLE LEVEL	SELECT INPUTS	OUTPUT
Dual 4-Input	74F153	2 (Low)	2 (High)	NINV
Dual 4-Input, 3-State	74F253		2 (High)	NINV
Dual 4-Input, 3-State	74F353		2 (High)	INV
Quad 2-Input	74F157/157A	1 (Low)	1 (High)	NINV
Quad 2-Input	74F158/158A	1 (Low)	1 (High)	INV
Quad 2-Input, 3-State	74F257A		1 (High)	NINV
Quad 2-Input, 3-State	74F258A		1 (High)	INV
Quad 2-Input	74F298		1 (High)	INV
Quad 3-Input	74F712A/712-1		2 (High)	NINV
Quad 3-Input	74F723A/723-1	1 (High)	2 (High)	NINV
Quad 4-Input	74F725A/725-1		2 (High)	NINV
Quint 2-Input	74F711A/711-1		1 (High)	NINV
8-Input	74F151A	1 (Low)	3 (High)	NINV, INV
8-Input, 3-State	74F251A		3 (High)	NINV, INV

Function Selection Guide

DECODER/MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE LEVEL	OUTPUT
Dual 1-of-4	74F139	2 + 2	1 (Low) + 1 (Low)	4 (Low) + 4 (Low)
Dual 1-of-4	74F539	2 + 2	1 (Low) + 1 (Low)	4 (High) + 4 (High)
1-of-8	74F138	3	2 (Low), 1 (High)	8 (Low)
1-of-8	74F538	3	2 (Low), 1 (High)	8 (High)
1-of-10	74F537	4	1 (Low), 1 (High)	10 (High)
1-of-16	74F154	4	2 (Low)	16 (Low)

BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Dual 4-Input NAND Transmission Line Driver	74F3040	INV
Dual 4-Input NAND Buffer	74F40	INV
Quad 2-Input NAND Buffer	74F37	INV
Quad 2-Input NAND Buffer, OC	74F38	INV
Quad 2-Input NAND Transmission Line Driver	74F3037/I74F3037	INV
Quad 2-Input Transmission Line Driver	74F3038	NINV
Quad Futurebus Backplane Transceiver, OC + 3-State	74F3893	NINV
Hex Inverter Buffer/Driver, OC	74F06/A	INV
Hex Inverter Buffer/Driver, OC	74F07/A	INV
Hex 2-Input NAND Driver, OC (Corner V_{CC} and GND)	74F804	INV
Hex 2-Input NAND Driver, OC (Corner V_{CC} and GND)	74F1804	INV
Hex 2-Input NOR Driver, OC (Corner V_{CC} and GND)	74F805	INV
Hex 2-Input NOR Driver, OC (Corner V_{CC} and GND)	74F1805	INV
Hex 2-Input AND Driver, OC (Corner V_{CC} and GND)	74F808	INV
Hex 2-Input AND Driver, OC (Corner V_{CC} and GND)	74F1808	INV
Hex 2-Input OR Driver, OC (Corner V_{CC} and GND)	74F832	INV
Hex 2-Input OR Driver, OC (Corner V_{CC} and GND)	74F1832	INV
Octal Inverter Buffer, OC	74F756	INV
Octal Buffer, OC	74F757	NINV
Octal Buffer, OC	74F760	NINV
Octal 30Ω Transmission Line/Backplane Driver, OC	74F30240	INV
Octal 30Ω Transmission Line/Backplane Driver, OC	74F30244	NINV
Octal Transceiver, OC	74F621	NINV
Octal Transceiver, OC	74F623	NINV
Octal Transceiver, OC	74F641	NINV
Octal Transceiver, OC	74F642	INV
Octal Transceiver/Register, OC	74F647	NINV
Octal Transceiver/Register, OC	74F649	INV
Octal Transceiver/Register, OC + 3-State	74F653	INV
Pi-Bus Transceiver (Octal Bidirectional Latched Transceiver), OC	74F776	NINV
Octal Latched Bidirectional Futurebus Transceiver, OC	74F8960	INV
Octal Latched Bidirectional Futurebus Transceiver, OC	74F8961	NINV

SHIFT REGISTERS

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK EDGE
Serial-In/Parallel-Out	74F164	8	D_{sa}, D_{sb}		↑
Serial-In/Parallel-Out Output Latch, 3-State	74F595	8	D_S		↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F195	4	J, K	4D	↑
Serial-In/Parallel-In/Parallel-Out, Shift Right	74F199	8	J, K	8D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F598	8	D_{s0}, D_{s1}	8 I/O	↑
Serial-In/Parallel-In/Serial-Out	74F674	16	SI/O	SI/O, 16D	↓
Serial-In/Parallel-In/Serial-Out	74F676	16	SI	16D	↑
Serial-In/Parallel-In/Serial-Out, 10/9 Bit	74F847	10/9	D_S	10D	↑
Serial-In/Parallel-In/Parallel-Out, Shift Right, 3-State	74F395	4	D_S	4D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F322	8	D_0, D_1	8 I/O	↑
Serial-In/Parallel-In/Parallel-Out	74F194	4	D_{sr}, D_{sl}	4D	↑
Serial-In/Parallel-In/Parallel-Out, Shift Right	74F199	8	J, K		↑
Serial-In/Parallel-In/Serial-Out	74F166	8	D_S		↑
Serial-In/Parallel-In/Parallel-Out, Bidirectional	74F198	8	D_{sr}, D_{sl}	8D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F299	8	D_{s0}, D_{s7}	8 I/O	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F323	8	D_{s0}, D_{s7}	8 I/O	↑
Parallel-In/Serial-In/Serial-Out, Multiplexed Inputs	74F539	8	D_s, D_{na}, D_{nb}	8D	↑
Parallel-In/Serial-In/Serial-Out, 2:1 Multiplexed Inputs	74F835	8	D_s, D_{na}, D_{nb}	8D	↑
Parallel-In/Serial-Out, Input Latch	74F597	8	D_S	8D	↑
Parallel-In/Parallel-Out, 3-State	74F350	4	SI/O	4Y	↑
Parallel-In/Parallel-Out, 3-State	74F604	16		A_0–A_7, B_0–B_7	↑
Parallel-In/Parallel-Out, True & Complement Output	74F398	8	S	I_{0a}–I_{0d}, I_{1a}–I_{1d}	↑
Parallel-In/Parallel-Out	74F399	8	S	I_{0a}–I_{0d}, I_{1a}–I_{1d}	↑

COUNTERS

FUNCTION	DEVICE NUMBER	MODULUS	PRESETTABLE	PARALLEL ENTRY	CLOCK EDGE
Synchronous (Asynchronous Reset)	74F161A	16	X	Synchronous	↑
Synchronous (Synchronous Reset)	74F163A	16	X	Synchronous	↑
Up/Down, Binary	74F169	16	X	Synchronous	↑
Up/Down, BCD Binary	74F191	16	X	Asynchronous	↑
Up/Down, BCD Binary	74F193	16	X	Asynchronous	↑
Bidirectional, Binary	74F269	256	X	Synchronous	↑
Up/Down, 3-State	74F569	16	X	Synchronous	↑
Up/Down	74F579	256	X	Synchronous (I/O)	↑
Up/Down, 3-State Multiplexed	74F779	256	X	Synchronous (I/O)	↑
Up/Down, 3-State Multiplexed	74F1779	256	X	Synchronous (I/O)	↑
Ripple Counter	74F393	10	X		↓

THREE-STATE BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Buffer	74F125	NINV
Quad Buffer	74F126	INV
Quad Bus Transceiver	74F242	INV
Quad Bus Transceiver	74F243	NINV
Quad Bus Transceiver	74F1243	NINV
Hex Buffer	74F365	NINV
Hex Inverter	74F366	INV
Hex Buffer, 4-Bit and 2-Bit	74F367	NINV
Hex Inverter, 4-Bit and 2-Bit	74F368	INV
Octal Buffer	74F240	INV
Octal Buffer	74F241	NINV
Octal Buffer	74F244/I74F244	NINV
Octal Buffer	74F1240	INV
Octal Buffer	74F1241	NINV
Octal Buffer	74F1244	NINV
Octal Buffer with Parity	74F455	INV
Octal Buffer with Parity	74F456	NINV
Octal Buffer with Parity	74F655A/I74F655A	INV
Octal Buffer with Parity	74F656A/I74F656A	NINV
Octal Driver	74F540	INV
Octal Driver	74F541	NINV
Octal Transceiver	74F245	NINV
Octal Transceiver	74F545	NINV
Octal Transceiver	74F620	INV
Octal Transceiver	74F640	INV
Octal Transceiver	74F1245	NINV
Octal Transceiver with Parity	74F657/I74F657	NINV
Octal Transceiver/Register	74F646/646A	NINV
Octal Transceiver/Register	74F648/648A	INV
Octal Transceiver/Register	74F651/651A	INV
Octal Transceiver/Register	74F652/652A	NINV
10-Bit Buffer	74F827	NINV
10-Bit Buffer	74F828	INV
10-Bit Transceiver	74F861	NINV
10-Bit Transceiver	74F862	INV
9-Bit Transceiver	74F863	NINV
9-Bit Transceiver	74F864	INV
Octal Registered Transceiver	74F543	NINV
Octal Registered Transceiver	74F544	INV
8-Bit Registered Transceiver	74F2952	NINV
8-Bit Registered Transceiver	74F2953	INV
Octal Registered Transceiver with Parity and Status Flags	74F552	INV
Octal Shift/Count Transceiver with Adder and Parity	74F807	INV

PRIORITY ENCODERS

FUNCTION	DEVICE NUMBER	ENABLE LEVEL	INPUT/OUTPUT LEVEL
8-to-3	74F148	Low	Active Low

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Bit Arithmetic Logic Unit	74F181
4-Bit Arithmetic Logic Unit	74F381
4-Bit ALU with Overflow Output for Two's Complement	74F382
4-Bit Binary Full Adder with Fast Carry	74F283
Look Ahead Carry Generator	74F182
Quad Serial Adder/Subtractor	74F285

COMPARATORS

FUNCTION	DEVICE NUMBER
4-Bit Identity Comparator	74F85
8-Bit Comparator	74F521
8-Bit Register Comparator	74F524

PARITY

FUNCTION	DEVICE NUMBER
9-Bit Odd/Even Parity Generator/Checker	74F280A/280B/I74F280B

SPECIAL FUNCTIONS

FUNCTION	DEVICE NUMBER
16 × 5 Asynchronous FIFO (3-State)	74F225
64-Bit RAM	74F189A/219A
Register Stack – 16 × 4 RAM 3-State Output Register	74F410
DRAM Dual-Ported Controller with Refresh	74F764-1
DRAM Dual-Ported Controller without Latch	74F765-1
4-Bit Asynchronous Bus Arbiter	74F786
1-MBit Memory Address Controller	74F1762
1-MBit Intelligent DRAM Controller	74F1763
1-MBit DRAM Dual-Ported Controller with Latch	74F1764
1-MBit DRAM Dual-Ported Controller without Latch	74F1765
Burst Mode DRAM Controller	74F1776
LED Driver	74F5300

Section 2
Quality and Reliability

Quality and reliability

SECTION 2

SUMMARY

The Signetics Company was founded in September, 1961 by a group of scientists and engineers who were among the pioneers in the development of integrated circuits. Signetics, acquired by Philips in 1975, was the first company in the world to be established for the sole purpose of designing, developing, manufacturing, and marketing ICs. Philips celebrated its 100th anniversary in 1991. On 1st January 1991, the Integrated Circuits and Discrete Semiconductor Business Units, formerly part of Philips Components, were merged into an autonomous product division (PD)—Philips Semiconductors as part of a major reorganization to focus Philips' semiconductor activities and to strengthen its standing in selected strategic markets. At the heart of this reorganization comes quality.

The Signetics approach to Quality Management has evolved with each evolution building upon the foundation laid. The emphasis in the 1960s and 1970s was quality by policy, documentation, and inspection. The emphasis in the 1980s was quality by employee involvement and process control. In the 1990s quality is achieved by emphasizing process and product Design For Manufacturability (DFM) and to customer requirements. (See Figure 1.) To ensure transformation, a formal Design Development Process (DDP) exists which requires the utilization of Cross-Functional Teams (CFTs) to assure that the customer Dimensions of Performance are met.

The modern Signetics Quality Journey (see Table 1) began in 1980. During the ensuing decade it achieved a 90-fold improvement in product electrical quality, 30-fold improvement in product visual and mechanical quality and a 20-fold improvement in product reliability. The great reduction in defect levels and a continued commitment to our customers made possible the following industry firsts:

- Ship-To-Stock Program
- Self-Qualification Program
- Zero Defects Warranty Policy

The Journey never ends—Signetics continues to strive for **EXCELLENCE** in all aspects of our business through company focus and initiatives aimed at achieving three performance level goals in 1994:

- Industry Leader in Customer Satisfaction
- With Products of Six Sigma Quality and Reliability
- And World Class Responsiveness to Customer Needs and Wants.

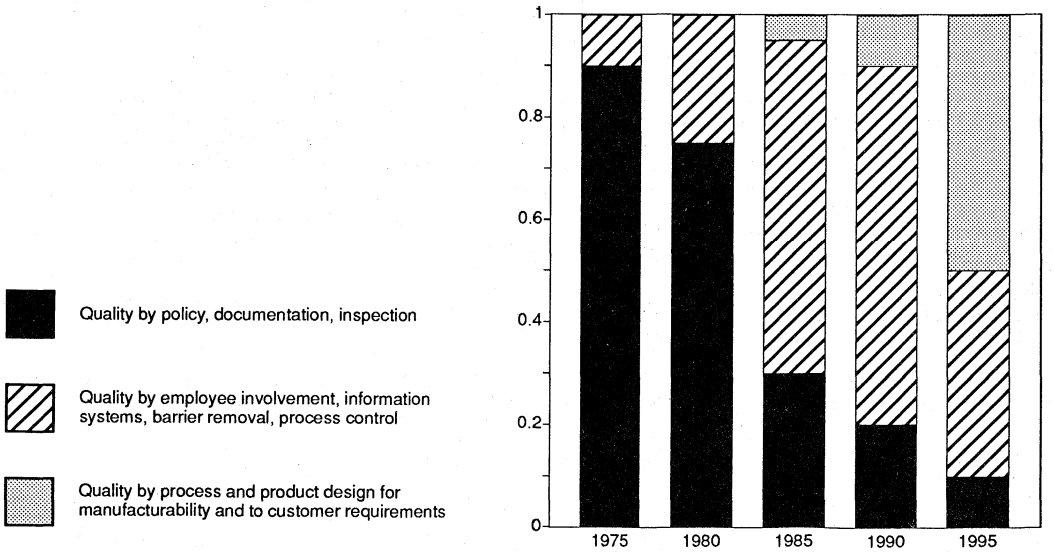


Figure 1. Evolution of Signetics Quality Management

SIGNETICS' QUALITY IMPROVEMENT PROCESS

In 1979, Signetics recognized that quality was becoming a major competitive issue, not only in the semiconductor business but also in other industries. Increases in the volume of products imported from the Far East (steel, automobiles, and consumer products) sent strong signals that new competitive forces were at work.

An investigation into a variety of quality programs was started. The company realized that quality improvement would require a contribution from all employees. Management commitment and participation, however, was recognized as the primary prerequisite for this program to work successfully. Resources required for the resolution of defects were under management control.

The "Signetics Quality Journey" from 1980 into the decade of the '90s is summarized in Table 1. In 1980 a program was developed which focused on quality management. Rearranging previous quality control philosophies, we developed a decentralized, distributed quality organization and simultaneously installed a Quality Improvement Process (QIP) based on the 14-Step improvement program advocated by Phil Crosby. The process was formally begun company-wide in 1981. Since then substantial progress has been made in every aspect of our operations. From incoming raw material conformance to improvements in clerical errors — every department and individual is involved and striving for Zero Defects. Zero Accept sampling plans and Zero Defects warranties are evidence of our ongoing commitment to and progress in quality. The Crosby 14 steps evolved into 9 elements as the foundation of the QIP. The QIP continued to expand, including more processes and disciplines as Signetics' vision cleared.

Today the Total Quality Management (TQM) model is applied to the QIP, as illustrated in Figure 2, having a far-reaching impact on all aspects of our business. The customer is at the start (driver) and end (goal) of the TQM model which requires a driver, system, measures and goal. The customer is the primary driver. Leadership is provided by Quality Improvement Teams (QITs) which ensure that customer interaction occurs and that the organization supports the mission, QI policy and customer direction. TQM requires a clear set of management principles which mandate systems and measurements consistent with stated objectives. TQM endorses and utilizes the seven major examination categories of the U.S.A. Malcolm Baldrige National Quality Award. Together, the examination categories address all major components of an integrated, prevention based system built around continuous improvement and customer satisfaction.

ZERO DEFECTS WARRANTY

In the '80s, American industry demanded increased product quality of its IC suppliers in order to meet growing international competitive pressure. As a result of this quality focus, it became clear that what once was thought to be unattainable— Zero Defects— is, in fact, achievable.

Signetics offers a Zero Defects Warranty which states that we will take back an entire lot if a single defective part is found. This precedent setting warranty implemented in 1985 effectively ended the IC industry's "war of the AQLs" (Acceptable Quality Levels). The ongoing efforts of IC suppliers to reduce PPM (Parts Per Million) defect levels is now a competitive customer service measure. This intense commitment to quality provides an advantage to today's electronics OEM. That advantage can be summed up in four words: ***Reduced Cost of Ownership.***

As IC customers look beyond purchase price to the total cost of doing business with a supplier, it is apparent that a quality-conscious supplier represents a viable cost reduction resource. Consistent high-quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures. Programs such as Self Qualification and Ship-To-Stock implemented in 1984 and Cycle Time Management (CTM) implemented in 1989 help reduce cost of ownership.

STATISTICAL PROCESS CONTROL (SPC)

Although application of statistics in our process development and manufacturing activities goes back to the early 1970's, the corporate-wide emphasis on Statistical Process Control (SPC) did not come until mid-1984.

A natural evolution of our quality improvement process made introduction of SPC and other related programs an inevitable event. SPC was, therefore, introduced under the QIP umbrella. The Crosby definition of Quality, "Conformance To Requirements (Specification)" was expanded to include "Conformance To Specified Targets". The measurement definition of "continuous improvement" was expanded to include "Continuous Reduction of Variability Around the Specified Target".

The objective of SPC is to institutionalize a systematic and scientific approach to business and manufacturing activities. This approach utilizes sound statistical theory. Managers are expected to be able to turn data into information and to make decisions solely on data (not perception).

The most critical and challenging aspect of implementing SPC is the establishment of a discipline within the operating areas so that decision making is fundamentally based on verifiable data and so that actions are documented. The other is the realization that statistical tools merely point out the problems but are not themselves solutions. The burden of action on the process is still on the shoulders of the person that implemented it. In order to implement SPC effectively, three steps are continually followed:

1. Documenting and understanding the process and using process flow charts and component diagrams.
2. Establishing data collection systems and using SPC tools to identify process problems and opportunities for improvement.
3. Acting on the process and establishing guidelines to monitor and maintain process control.

Repeating steps 1-3 again.

These fundamentals are the basis of establishing specifications and operating philosophy with respect to SPC. The management of SPC, be it policy, function deployment or ongoing continuous improvement is accomplished in a systematic way by following the four step Plan, Do, Check, Act – PDCA/Shewart/Deming Cycles of Learning.

Table 1. Signetics Quality Journey

		1980 – 1983	1984 – 1985	1986 – 1988	1989 – 1990	1991 – 1994
FOCUS		• Raw Material Quality • Product Quality • Individual Responsibility for Quality	• Supplier Partnerships • Manufacturing Excellence	• Customer Partnerships • In-process Quality Control • Product Reliability	• Cross Functional Operation • Better Management Practices • Cycle Time Management	• Customer Driven • Design Quality • Involve Everyone • Competitive & Functional Benchmarks
INITIATIVES	SUPPLIER	• No Waiver Policy • Audits • Certification Program	• Recognition • Ship-to-Stock (STS)	• SPC Implementation	• Measurement-TQRDC • Supplier Teams	• Cycle Time Management • Broaden to Equipment & Service
	INTERNAL	• Decentralized Q & R Function • Crosby 14 Steps & Absolutes • 33 QITs Formed • All Employees Sign ZD Pledge	• JIT Manufacturing • Zero Accept Sampling Plans • Repeat 14 Steps	• SPC Introduction • Early Failure C/A Program • 14 Steps to 9 Elements • Customer Workshop	• Design Development Cycle Time Reduction • Make Market Cycle Time Reduction • Inventory Reduction • Baldrige Assessment & Planning	• 6 Sigma Strategy • Responsiveness Strategy • Benchmarking – Design Methodology – Mfg. Excellence – Quality & Service • QIP Audits • ISO 9001 Certification • TQE Award
	CUSTOMER	• PPM Program	• ZD Warranty Policy • STS Program • Customer Process Change Notification • Self Qual Program	• Listening Post-TQRDC • Advocate Program • Lot Traceability	• SPC Communications • Customer Certifications • Electronic Data Interchange	• Customer Relationship Management Plan • Customer Survey • Quality Strategy Communications
GOAL		• Conformance to Requirements • Zero Defects	• Zero Defects to Customers	• Conformance to Customer Requirements • Continuous Improvement	• Total Customer Satisfaction • Cycle Time Entitlement	• Industry Leader in Customer Satisfaction • 6 Sigma Quality • World Class Responsiveness

Figure 2. Total Quality Management Model

CYCLE TIME MANAGEMENT (CTM)

Cycle Time Management efforts are focused on Design-Development Process and Make-Market Process Responsiveness. Both are aimed at reducing the cycle time of tasks from current performance (Baseline) to entitlement (Using Existing Resources) then to improved entitlement and theoretical limit.

Design-Development focuses on getting the right products and processes to production within the market window interval. Make-Market concentrates on getting product into the customers hands within Customer Lead Time Requirements. Cycle time management directly links to quality improvement in its requirement for task barrier identification at the root cause level and removal of those barriers (e.g. eliminating causes of rejects thereby eliminating rework or product sort). Also, the acceleration of results from reducing cycle time increases the frequency of events thereby increasing the cycles of learning required for quality improvement.

DESIGN FOR MANUFACTURABILITY (DFM) AND SIX SIGMA

A by-product of CTM application to the Design-Development Process (DDP) is the Signetics proprietary DDP manual introduced in January 1991 followed by Cross Functional Team (CFT) training. The DDP applies to all product, package and technology groups in Signetics. CFT's are used to drive the project from planning phase until all objectives of the new product contract are met. The requirements for SPC, DFM and meeting Six Sigma objectives are contained in the DDP manual. The CFTs are responsible for assuring that DFM occurs with an objective of Six Sigma. A Six Sigma design means that any desired characteristic of a part has a yield of 99.9997% or a defect rate of 3.4PPM (C_p of 2 or C_{pk} of 1.5)

QUALITY PERFORMANCE

Our Quality Improvement Process has influenced our entire production cycle - from the purchases of raw materials to the shipment of finished product. The involvement of all areas of the company has resulted in impressive quality improvements. A traditional quality gauge is final electrical and visual/mechanical product defect levels as measured upon first submittal results at outgoing Quality Assurance gates; Estimated Process Quality (EPQ). This is the PPM Level at our outgoing inspection for all accepted and rejected lots. (See Figures 3 and 4.) Current product shipments routinely record below 20PPM (Parts Per Million) electrical defect levels and 150PPM visual/mechanical defect levels. Since we utilize zero accept sampling on all finished product inspection, any lot with one or more rejects is rejected and 100 percent inspected.

The most meaningful measure of our quality is how we measure up to our customer's expectations. Many customers routinely send us incoming inspection data or ratings on our products and services. In 1991, Signetics also implemented a formal annual customer survey to solicit inputs on Signetics performance to the Dimension of Performance deemed relevant by the customer. Signetics is very appreciative of the recognition given by customers. Since 1986, Signetics has received over 70 formal commendation plaques from customers in recognition of Quality, Delivery and Service. Due to this type of performance, a number of our customers have eliminated expensive incoming inspection testing and have subscribed to the Ship-to-Stock Program. (See Figure 5.)

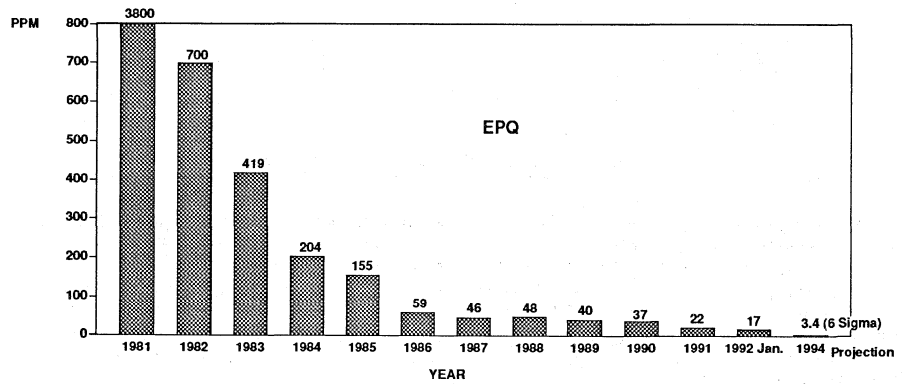


Figure 3. Electrical Product Quality Based on First Time Q.A. Submission Results

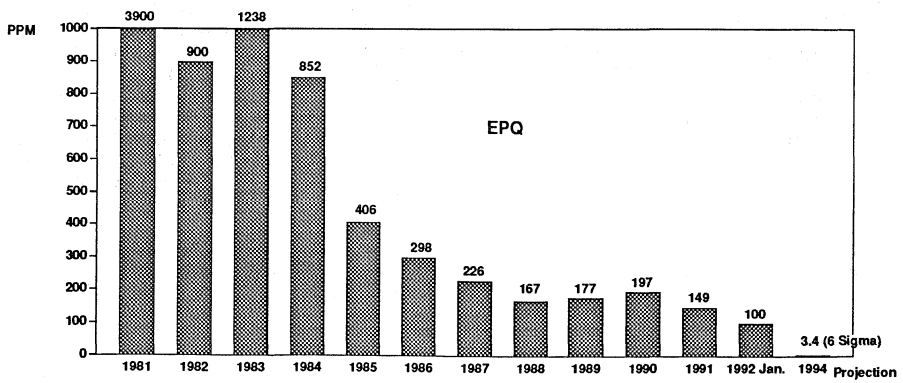
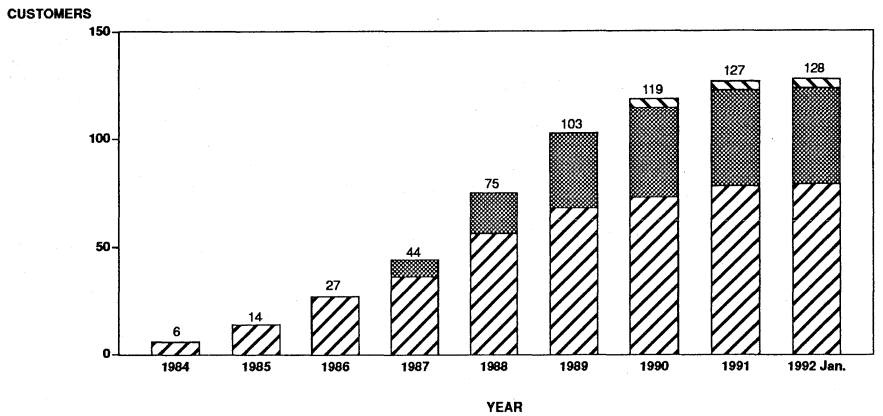


Figure 4. Visual/Mechanical Product Quality Based on First Time Q.A. Submission Results



	1984	1985	1986	1987	1988	1989	1990	1991	Jan. 1992
Asia Customers							4	4	4
Euro Customers				8	19	35	42	45	45
U.S. Customers	6	14	27	36	56	68	73	78	79

Figure 5. Signetics Ship-To-Stock Customer Growth

SHIP-TO-STOCK PROGRAM

Ship-to-Stock is a formal program developed at the request of our customers to help them reduce their costs by eliminating incoming test and inspection. Through close work with these customers in our quality improvement program, they became confident that our defect rates were so low that the redundancy of incoming inspections and testing was not only expensive, but unnecessary. They also saw that added component handling increased the potential of causing defects.

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into the customer's assembly line or inventory. This program was developed at the request of several major manufacturers after they had worked with us and had a chance to experience the data exchange and joint corrective action occurring as part of our quality improvement program.

Manufacturers using large volumes of ICs, those who are evaluating Just-in-Time delivery programs, or those who want to reduce or avoid high-cost incoming inspection are strongly encouraged to participate in this worthwhile program. Contact your local sales representative for further assistance and information on how to participate in this program.

RELIABILITY ASSURANCE PROGRAMS

Focus on Product Reliability

From 1981 to 1984, continuing improvements in process and material quality had a significant impact on product reliability.

Since 1984, the company has intensified its effort to markedly improve product reliability. Corporate Reliability Engineering, Group and Plant Reliability Units and Manufacturing Engineering work jointly on numerous improvement activities. These focused activities enhance the reliability of future products by providing improved methods for reliability assessment, increased understanding of failure physics, advanced analytical techniques, and aid in the development of material and processes.

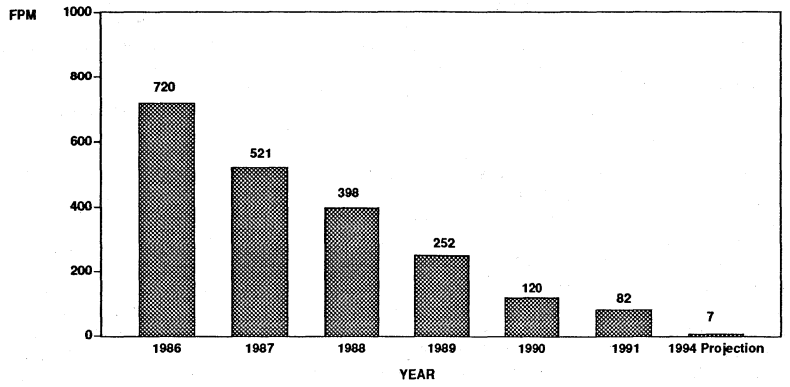


Figure 6. Signetics Early Failure Rate (EFR) Levels

EARLY FAILURE RATE (EFR) FOCUS

In 1986 Signetics intensified the focus on Early Life Reliability because of the significant impact EFR failures have on end system reliability performance. This program, which has now become a standard element in our reliability monitoring activities, provides quality engineering with statistically significant definition of low level process related defects. From these data, focused failure mechanism corrective actions can be developed. Average EFR levels on a broad cross section of processes, have been reduced from 720FPM to less than 100FPM since the corrective action effort was initiated in 1986 (reference Figure 6). Details of that activity are available upon request.

RELIABILITY MEASUREMENT PROGRAMS

Comprehensive product and process qualification programs have been developed to assure that our customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production on a regularly established basis (see Table 2).

Table 2. Reliability Assurance Programs

RELIABILITY FUNCTION	TYPICAL STRESS	FREQUENCY
New Process Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process (and facility) Each new assembly process (and facility)
New Product Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle Electrostatic Discharge Characterization	Each new product family
SURE III	High Temperature Operating Life Temperature-Humidity, Biased, Static Pressure Pot Temperature Cycle	Each fab process family, every four weeks
Product Monitor	Pressure Pot	Each plastic package type and technology family at each assembly plant, every week

DESCRIPTION OF STRESSES

High Temperature Operating Life

Static High Temperature Life (SHTL) stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. The voltage bias must be maintained until the devices are cooled down to room temperature from the elevated life test temperature. Dynamic High Temperature Life (DHTL) stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem. For this reason, SHTL has typically been used as the accelerated life stress for Logic products. DHTL is useful for products such as memory and micro-processor/controller where a large portion of the area can only be accessed by dynamic means.

HTSL-High Temperature Storage Life

This stress exposes the parts to elevated temperatures (150°C-175°C) with no applied bias. For plastic packages, 175°C is the high end of its safe temperature region without accelerating untypical failure mechanisms. This test is intended to accelerate potential mechanical package-related failure mechanisms such as Gold-Aluminum bond integrity and other process instabilities.

THBS-Temperature-Humidity, Biased, Static

The accelerated temperature and humidity bias is performed at 85°C and 85% relative humidity (85°C/ 85% RH). In general, the worst case bias condition is the one which minimizes the device power dissipations and maximizes the applied voltages. Higher power dissipations tend to lower the humidity level at the chip surface and lessen the corrosion susceptibility.

TMCL-Temperature-Cycling, Air to Air

The device is cycled between the specified upper and lower temperature without power in an air or Nitrogen environment. Normal temperature extremes are -65°C and +150°C with a minimum 10 minute dwell and 5 minute transition per MIL-STD-883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe. However, for large die the stress may be too severe and induce failures that would not be expected in a real application.

PPOT-Pressure Pot

This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127°C and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. The plastic encapsulant is not a moisture barrier and will saturate with moisture within 72 hours. Since the chip is not powered up the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination induced leakage problems, and general glassivation stability and integrity. It is also a good test for both package integrity (cracks in the package), and for die cracks (the moisture swells the plastic enough to stress the die; also the moisture causes leakage paths in the crack itself).

PRODUCT AND PROCESS QUALIFICATION PROGRAMS

Qualification activity is centered around new products and processes and changes in products and processes. The goal is to assure that the products can meet the qualification requirements prior to general release, and on an ongoing basis to demonstrate conformance to those requirements. The nature and extent of reliability stressing required depends on the type of change and the amount of applicable reliability data available.

A full qualification may include Early Failure Rate (EFR), Intrinsic Failure Rate (IFR), and Environmental Endurance Stressing. Such stress plans are reserved for introductions or changes that involve new or untested material or processes and, as such should be subjected to the maximum reliability interrogation. This normally entails a full range of biased and unbiased temperature and humidity stresses along with thermo-mechanical stresses.

For changes that are of limited scope, the full range of qualification stressing may not be warranted. In these instances, the nature and extent of the change is examined and only those stresses which provide a valuable measure of the change, or those which will detect potential weakness, are performed.

SELF-QUAL PROGRAM (SQP)

Self-Qual, initiated in 1984, is a joint program between Signetics and a customer that formally communicates the qualification activities for a new or changed product, process, or material. The Self Qual process provides our customer's engineering groups an opportunity to participate in the development of the qualification plan. During the qualification process, customers may audit the project, and can receive interim updates of qualification progress. Upon completion, formal detailed engineering reports are provided.

The major impact to the customer comes from the reduced workload on the component engineering and qualification groups. These engineering resources generally divide their time between routine qualification activity and problem resolution on critical components. By eliminating the need to perform qualification for one of the basic supplier changes the customer component engineer can spend more of his time resolving the critical product issues. In addition, the total amount of stress hardware needed to perform qualification life tests and other environmental evaluations can be reduced, saving the customer facility costs and reducing operating expense.

Self-Qual is a no-risk proposition for the customer. Each Self-Qual proposal provides a detailed description of what we are changing and why. It includes a detailed plan of what we intend to do to establish the reliability of the products affected. If the customer wishes to have product added to the plan or select some additional stresses, or prefers alternative stress conditions, Signetics will do everything possible to accommodate those requests. After that, if the customer is still uncomfortable with the recommended change, they are under no obligation to accept our data, and they may also perform their own qualification program. Customers who are interested in participating in this program should contact their local sales representative or the Corporate Reliability Engineering department directly.

SURE III RELIABILITY MONITORING PROGRAM

In order to implement an improvement program, a standard measure of performance was needed. The results from the SURE III Reliability Monitoring Program are used as basic ongoing measures of product reliability performance. This program samples all generic families of products manufactured and utilizes standardized stress methods and test procedures. A measurement philosophy was adopted based on the premise of continual improvement toward our performance standard of zero defects. We also increased our standard Pressure Pot stress conditions from 15 PSIG/121°C to 20 PSIG/127°C. This reduced stress duration from 168 hours to 72 hours, and increased high volume sampling, which increased sensitivity to low defect levels. Our standard monitoring program, SURE III, includes the stress conditions as described in Table 3. The continuous improvement results are shown in Figure 7 Signetics Reliability Index as Failure Per Million (FPM). The FPM value includes all rejects from all accelerated stresses divided by total units submitted to all stresses. This is a relative number used to manage continuous reliability improvement. It should not be interpreted as an expected failure rate. Figure 8 shows the continuous improvement in the SURE III 1000 Hour High-Temperature (T_J > 150°C) Operating Life Test FPM (includes early and intrinsic failure rates) for all technologies combined.

The 428 FPM for 1991 derates to 1 FIT at 45°C ambient temperature when assumptions of 0.7eV, 60% UCL and an 8°C junction rise above ambient are used. Admittedly the 1 FIT calculation for 1991 includes all technologies and unsubstantiated assumptions, but is a plausible number. Detailed FIT calculations by family do exist. Failure rate information is provided in the Signetics Product Reliability Summary Report available to all customers. In addition, the Signetics Reliability Handbook and the Signetics Process Technology and Manufacturing Facility Roadmap publications further define the rationale for methods used and the formation of process, product and package families.

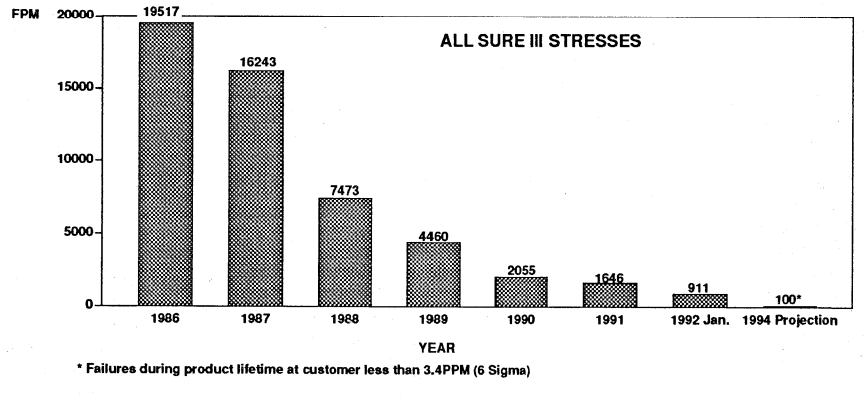


Figure 7. Signetics Reliability Index

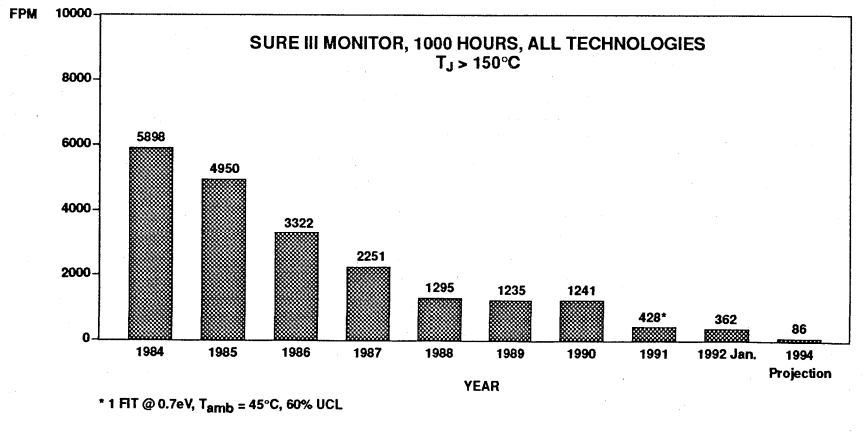


Figure 8. High-Temperature Operating Life Test FPM

Table 3. SURE III Reliability Monitoring Program

RELIABILITY FUNCTION	STRESS CONDITIONS	# UNITS
Static High Temperature Operating Life (SHTL)	Tj ≥ 150°C, T_{amb} = 125°C to 150°C, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours	135/150 Monthly
Temperature-Humidity, Biased, Static (THBS)	T_{amb} = 85°C ± 3°C, Humidity = 85% RH ± 5%, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours	100 Monthly
Temperature Cycling (TMCL)	T_{amb} = -65°C (+0°C -10°C) to +150°C (+10°C -0°C), Air-to-Air, Dwell time = 10 minutes minimum each extreme, Biased condition = None, Duration = 1000 cycles for plastic package, 300 cycles for ceramic package	100 Monthly
Pressure Pot	T_{amb} = 127°C ± 2°C, 20 PSIG ±0.5 PSIG (PPOT). 100% saturated steam, Biased condition = None, Duration = 72 hours	100 Weekly
		435/450 per Family

NOTE: V_{CC} = MAX is generally equal to V_{CC} = MAX as specified in data handbook

PRODUCT MONITOR

In addition to the SURE III program, each assembly plant performs Pressure Pot (20PSIG, 127°C, 72hours) reliability monitors on a weekly basis for each molded package type by pin count. The purpose of this program is to monitor the consistency of the assembly operations for such attributes as molding quality and die attach and wire bond integrity. This data is reported back to manufacturing operations and corporate and group reliability and quality assurance departments by electronic mail each week.

RELIABILITY EVALUATION

In addition to the product performance monitors encompassed in the SURE III program, Corporate and Group Reliability Engineering departments sustain a broad range of evaluation and qualification activities. Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.
- Devices or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE III program; however, more highly accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are included in some evaluation programs.

STRESS FACILITY QUALITY

Quality improvement has reached all functional areas of the company, and the reliability stress laboratories are no exception. Corporate Reliability Laboratory (CRL) is one of the many areas where the benefits of the quality improvement process pays repeated dividends.

CRL utilizes stress which accelerate failure rates hundreds to thousands of times, requiring precision and control to make reliability data meaningful. Stress loading schedules are maintained with absolute regularity and chambers are never off-line beyond scheduled loading plans. Board currents are recorded prior to and at each interval on biased stresses, and monitoring of in-oven currents is conducted daily.

Thermal modeling of the Temperature Cycling systems has been accomplished and all loads are carefully weighed to ensure that thermal ramps are consistent.

Pressure Pot and Biased Pressure Pot systems utilize microprocessor controllers, and are accurate to within 0.1 degree centigrade. Saturation is guaranteed via automatic timing circuits, and a host of fail-safe controls ensure that test groups are never damaged.

Electrostatic discharge (ESD) handling precautions are standard procedures in the laboratories, and the occurrences of devices lost, zapped, or overstressed have become almost non-existent.

MANUFACTURING FACILITIES

Signetics, as part of a multinational corporation, utilize manufacturing facilities for wafer fabrication, package assembly, and test in three states and six overseas countries as shown in Table 4. Wafer fabrication is performed in fabs which report to the Product Groups. Assembly operations in Korea and Thailand report to Assembly Manufacturing Operations (AMO). Assembly subcontractors are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Signetics' specifications and materials. We have on-site quality assurance personnel at each subcontractor site to audit assembly processes and procedures.

TYPICAL IC MANUFACTURING FLOW

The manufacturing process for integrated circuits begins with wafer fabrication. The wafers are then electrically sorted, assembled, and tested prior to customer shipment. Quality assurance inspections are utilized throughout the manufacturing process, with manufacturing being responsible for the process/product quality.

Table 4. Product Manufacturing

FACILITIES	DESIGNATION	LOCATION	PROCESS OR PACKAGE FAMILIES
Wafer Fabrication	Fab 01	Sunnyvale, California, USA	Bipolar, Linear, Junction Isolated and Quality Assurance
	Fab 21	Orem, Utah, USA	Bipolar Gold Doped, Schottky, Oxide Isolated, ECL, PLD and Quality Assurance
	Fab 22	Albuquerque, New Mexico, USA	NMOS, CMOS, ACMOS, BiCMOS, EPROM and Quality Assurance
	Fab 23	Albuquerque, New Mexico, USA	CMOS EPROM, Flash EPROM, BiCMOS, and Quality Assurance
	MOS #2	Nijmegen, The Netherlands	HC(T) CMOS Logic and Quality Assurance
Assembly	Alphatec (R)	Bangkok, Thailand	Ceramic DIP and Quality Assurance
	Anam (L)	Seoul, Korea	Plastic DIP, SO, PLCC, Metal Can and Quality Assurance
	ASAT (C)	Hong Kong	Plastic QFP, SO, and Quality Assurance
	HANA (M)	Bangkok, Thailand	Plastic DIP and Quality Assurance
	Hyundai (W)	Ichon, Kyungki, Korea	Plastic DIP, SO, PLCC, Ceramic DIP and Quality Assurance
	MEC (T)	Osaka, Japan	Plastic SO EIAJ, QFP and Quality Assurance
	Orem (P)	Orem, Utah, USA	Ceramic DIP, Flat Pack, QFP, PGA and Quality Assurance
	Pebei (B)	Kaosiung, Taiwan	Plastic DIP, SO, SSOP, PLCC, and Quality Assurance
	SigKor (K)	Seoul, Korea	Plastic DIP, SO, PLCC, and Quality Assurance
	Sig Thai (V)	Bangkok, Thailand	Plastic DIP, SO, and Quality Assurance
	Rohm (G)	Kyoto, Japan	Plastic QFP and Quality Assurance
Test	TA05	Sunnyvale, California, USA	Wafer Sort, Final Test and Quality Assurance
	SigKor	Seoul, Korea	Final Test and Quality Assurance
	SigThai	Bangkok, Thailand	Final Test and Quality Assurance
	Albuquerque	Albuquerque, New Mexico, USA	Wafer Test and Quality Assurance
	Orem	Orem, Utah, USA	Wafer Test, Military Final Test and Quality Assurance

Table 5. Package Construction

ITEMS	PLASTIC DIP	SO AND PLCC	CERAMIC DIP(CERDIP)	CERAMIC FLAT PACK
Lead Frame	Copper, 194 Alloy	Copper, 194 or PMC102	Alloy-42	Alloy-42
Lead Finish	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40) or Solder Plate (80/20)	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40)
Bond Area Finish	Silver Spot	Silver Spot	Silver Spot	Silver Spot
Die Attach	Silver Filled Polymide or Thermoplastic	Silver Filled Polymide or Thermoplastic	Silver Filled Glass	Silver Filled Glass
Bond Wire	Gold, 1.0-1.3 mils in Diameter	Gold, 1.0-1.3 mils in Diameter	Aluminum, 1.0-1.3 mils in Diameter	Aluminum, 1.0-1.3 mils in Diameter
Wire Bonding Die Lead Frame	Thermosonic Ball Stitch	Thermosonic Ball Stitch	Ultrasonic Stitch Stitch	Ultrasonic Stitch Stitch
Package Material	Novolac Epoxy	Novolac Epoxy	Ceramic	Ceramic

SPECIAL PROCESSING

SUPR II LEVEL B –

For our customers who require an infant mortality rate level less than that normally provided for our standard products (typically less than 1000PPM), we offer our Signetics Upgraded Product Reliability (SUPR) program.

Devices are burned-in per Signetics specification 850-227 schematics for a minimum of 21 hours at junction temperature between 155°C to 175°C. For a 1.0eV activation energy, 21 hours at 155°C is equivalent to 168 hours at 125°C.

Following burn-in, all devices are cooled down under bias and tested within 96 hours. All devices are tested before and after burn-in, yield calculated and compared to Percent Defective Allowed (PDA). If a lot fails PDA, it is investigated and good units submitted to a second burn-in. All "SUPR II B" devices carry a "B" marking.

The SUPR program was introduced in 1972 to improve quality and reliability and was expanded in 1975 to SUPR II A which included the burn-in option, SUPR II B. With the implementation of the Signetics Quality Improvement Process in 1980, standard product quality levels and guarantees caught up and passed SUPR II. All processing,

except for burn-in, is now standard. The Signetics standard warranty is Zero Defects.

"Evaluation of Early Failure Levels and The Effectiveness of Burn-In" is available upon request through your local sales office. This brochure is an aid for those users and purchasers of integrated circuits who need to make a decision regarding burn-in.

PUBLICATIONS

Signetics routinely publishes documents supporting the Quality and Reliability Improvement Process. The following significant documents are currently available.

IC Quality Series

Quality and Reliability Policy Manual (850-8000)

This manual is the starting point for understanding the policies of Signetics pursuant to constantly improving the high standards of quality and reliability in the manufacture of monolithic integrated circuits. Responsibilities and authority of organizations are defined along with governing specifications and operator instruction documents.

Signetics QIP Total Quality Management

This booklet describes the TQM model, patterned after the U.S.A. Malcom Baldrige National Quality Award criteria and how the model is applied to the Signetics Quality Improvement Process.

Supplier Partnership Guide

This booklet defines Signetics philosophy, policy and requirements for establishing strategic partnerships with raw material suppliers.

Product Symbol Formats

This publication provides a guide for determining standard product symbol format and content for decoding inventory and product in field usage since 1980. Since date code 8717, Signetics has symbolized the assembly start computer Lot ID on commercial products providing full traceability back to start of wafer fabrication.

Quality Attributes EDI System

This manual defines system requirements for Electronic Data Interchange (EDI) of Quality Attributes (pass/fail) Data.

Monthly Product Outgoing Quality Summary Reports

Estimated Process Quality (EPQ) in PPM for electrical, visual/ mechanical and hermeticity by part number or by family.

Statistical Process Control

This booklet introduces the Signetics SPC system including terminologies, philosophy, organization, training and implementation strategy and status.

Ship-To-Stock Program

This booklet defines the "joint program" requirements of Signetics and the customer to formally certify specific products to go directly into the assembly line or inventory with reduced or no incoming inspection thereby reducing cost of ownership.

Customer Return Immediate Service Program (CRISP)

This booklet defines the joint responsibilities of Signetics and the customer to assure that correlation samples are investigated and results reported per the Signetics 1-4-5 cycle time commitments.

IC Reliability Series

Signetics Reliability Handbook

This handbook is a detailed guide to Signetics Reliability Qualification and Monitoring activities. It includes reference sections that deal with the application and statistics of integrated circuit reliability issues.

Product Reliability Summary

Yearly, SURE III monitoring data is summarized and published for all product families in a Product Reliability Summary. Summaries like this one provide a detailed overview of product family performance and estimates the reliability of those products in use conditions.

Quarterly Reliability Update

Detailed results, by part number, package type, date code, assembly location, and by stress and test interval are routinely published in the Signetics Quarterly Reliability Update. The "Update" is available at the end of each quarter, and contains the results of reliability monitors which completed during the previous quarter, plus approximately 3 years of history for each product family.

SMD Reliability (The Reliability and Durability of Surface Mount Packages)

In support of Signetics' leadership in Surface Mount Device (SMD) technology, we have published in-depth studies and evaluations on the reliability and durability of SMD packages. The Surface Mount Reliability report covers evaluation of products after exposure to the unique environments created by various SMD soldering and cleaning processes.

Process Technology and Manufacturing Facility Roadmap

This document defines the various process technologies in production in Signetics manufacturing facilities, and defines in detail, the fab and assembly processes and locations qualified to produce all released products.

Thermal Characteristics of Integrated Circuit Packages

This is a comprehensive collection of thermal characterization data for all packages manufactured by Signetics. Thermal resistance data to *Case*, and to *Ambient* are provided. Details on airflow effects and die size are included.

SSQP – Signetics Self-Qual Program-Reports

In addition to the regular publications of reliability monitor results, a special program for the publication of qualification proposals and final engineering reports has been in place since January of 1984. Self-Qual Reports are available on all major process changes and introductions, thereby reducing customer cost of ownership.

Evaluation of Early Failure Levels and the Effectiveness of Burn-In

This report provides results of the Signetics Early Failure Rate (EFR) program implemented in 1986 to identify and eliminate root causes of infant mortality and to aid users of IC components faced with a decision regarding Burn-In of purchased integrated circuits.

DATA AVAILABILITY

The previously referenced documents are available to all our customers. Many are available in your local sales office, or from:

Corporate Quality System Group
Mail Stop #35
811 East Arques Avenue
P. O. Box 3409
Sunnyvale, CA 94088-3409, USA

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Section 3
Circuit Characteristics

FAST TTL Logic Series

Circuit Characteristics SECTION 3

INPUT STRUCTURES

There are three types of input structures used in FAST circuits: diffusion diode, PNP vertical transistor, and NPN transistor. Each of these are discussed below.

The diffusion diode input is most often used with FAST circuits. The input diode is labeled as D1 in Figure 1. There can be more than one if NAND logic is to be performed. In the oxide-isolated processes these are base-collector diffusions. Each input pin also has a Schottky clamp diode D2. This diode is standard for most TTL circuits, and is included to limit negative input voltage excursions that are generally the result of inductive undershoot.

The static diode input function of voltage versus current is shown in Figure 2. If the pin voltage is negative, most of the relatively high negative current flows through the clamp Schottky D2. At 0V the current flows from V_{CC} through R1 and D1 to the pin. Switching from a logic Low level to a logic High level occurs when the input pin voltage rises high enough to force the current from the D1 path to the Q3–Q2–Q1 path. This happens when the base voltage of transistor Q3 is at three base-emitter drops ($3V_{BE}$), and the pin is at $2V_{BE}$, which is the standard FAST threshold switching voltage. At this voltage the input current is very small, just the leakage currents of diodes D1, D3, and clamp diode D2. The current remains at this small, positive value until breakdown voltage is reached.

Transistor Q3 and resistor R2 provide a current gain by increasing the amount of current available to Q2 and Q1 when the pin voltage is high. R3 bleeds current off the base of Q2 to pull it low when the pin voltage is low. D3 speeds up this process during the High-to-Low pin transition. When the switching transients are over, D3 is reverse biased.

The current of Figure 2 is scaled for the case where the pin is required to pull down a single 10KΩ resistor R1 (20μA maximum in the High state and 0.6mA maximum in the Low state), which is defined as a standard FAST Unit Load (UL). For some parts, pin current can exceed a UL, especially in the logic Low state. This will happen if the pin must sink the current from more than one R1 resistor, or if the value of R1 is less than 10KΩ, which will be the case if the capacitance at the base of the transistor Q3 is too large for the required switching speed. In this event, the actual number of ULs is listed for each input in the specification sheet for the part. Note: UL, as defined here, is less than the normally defined Schottky TTL Unit Load. The correlation is one Schottky Unit Load – 1.67 ULs. This is an important point to remember for fan-in and fan-out calculations in systems that mix FAST with other TTL families.

The PNP vertical transistor has found wide acceptance in its various forms in low power Schottky logic because it provides a high-impedance input which is usually desirable. It was not used with early FAST circuits because the original oxide-isolated processes did not provide a fully suitable PNP vertical structure. It is now frequently the input of choice for new parts built with improved processes. The PNP transistor Q3 is fabricated with the P-type substrate as the grounded collector, the N-type Epi as the base, and the P-type normal base diffusion as the emitter. The process must be tailored to provide a suitable current gain for this vertical structure and must have provision to remove the considerable substrate current without an appreciable rise in substrate voltage. Referring to Figure 3, Q3 functions as an emitter follower for pin voltages low enough to provide an emitter-base forward bias. This occurs at an emitter voltage below the $3V_{BE}$ value provided by the D3–Q2–Q1 stack, and gives the desired $2V_{BE}$ pin threshold. At pin voltages above this value, Q3 turns off and the current through R1 is directed to Q2–Q1 through D3. The Schottky diode D2 speeds up the High to Low transition if the pin voltage falls more rapidly than the base of Q2; otherwise, D2 is off. The PNP input characteristics are shown in Figure 4. If the input voltage is negative with respect to ground, a large clamp current flows through D1. As the voltage rises, D1 turns off and the input current falls to the base current of Q3; for the usual values of R1, this is in the range of about 10μA. This decreases as the lead voltage rises. At threshold, Q3 turns off and the input current drops to a low value determined by the leakage of D1, D2, and Q3. The current remains at this low value until the onset of breakdown. Since all PNP inputs are protected with ESD structures, the breakdown current is set by this, and not the actual PNP device.

The NPN input is shown with two variations in Figures 5 and 6. It has limited use in standard TTL circuits, and is used in selected FAST devices, especially where its superior high-impedance input characteristics are useful. A typical plot of static input current versus input voltage is shown in Figure 7.

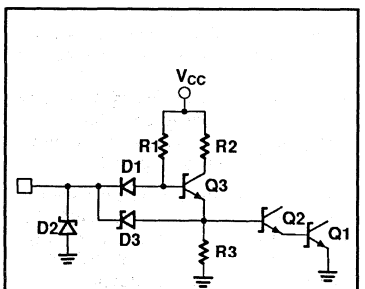


Figure 1. Diode Input

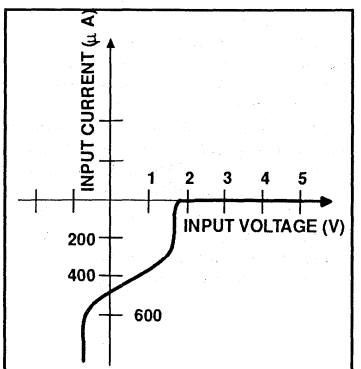


Figure 2. Static Diode Input Function of Voltage vs. Current

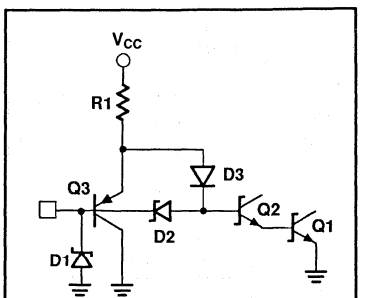


Figure 3. PNP Input

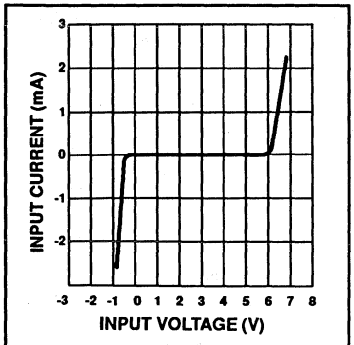


Figure 4. PNP Input Characteristics

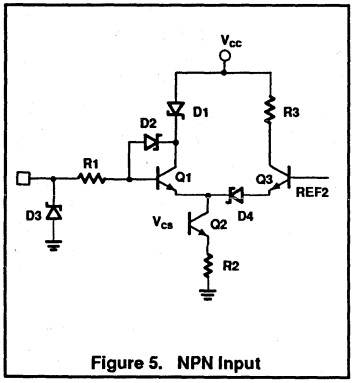


Figure 5. NPN Input

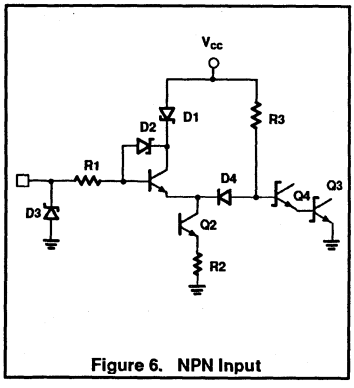


Figure 6. NPN Input

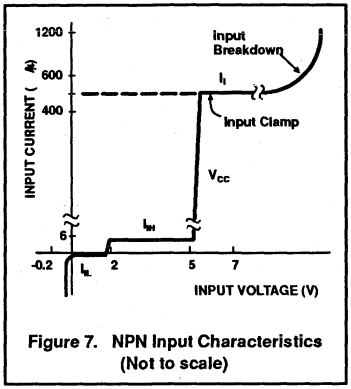


Figure 7. NPN Input Characteristics (Not to scale)

There are some significant differences between this function and that of the diffusion diode input shown in Figure 2, the most important being the much lower input current in the region from 0V to threshold and the controlled increase of input current above V_{CC}.

When the pin voltage is negative, the large negative clamp current is supplied through the clamp Schottky diode D3. For positive voltages, from 0V to the switching threshold of $2V_{BE}$, Q1 is off, and the input current I_{IL} is very small, just the leakage current of Q1, D2, and D3 with low reverse bias. As the input voltage rises above $2V_{BE}$ Q1 turns on, and the current that had been flowing through D4 now flows through Q1, blocking Schottky diode D1 to V_{CC}. The value of this current is determined by the current source transistor Q2 with its base connected to voltage reference V_{CS}, and by the size of the emitter resistor R2. The current is nearly constant within the normal operating range of input voltages and has a typical value of 0.1mA to 1.0mA. The pin must supply only a small fraction of this bias current, the ratio of Q1 collector current to base current being the bipolar β factor. Typically, I_{IH} base input current is less than 20μA in the voltage range from 0V to V_{CC}. This value is the specification for a standard FAST NPN Unit Load. As in the diode input case, its larger currents are needed to reduce delay times or to provide tor multiple-input transistors connected to the same pin, the specification sheet tor the particular device will identify the input pins which have NPN ULs larger than one, and will list their values.

In normal operation, the pin voltage will be limited in the negative direction by the diode clamp D3, and will be less than V_{CC} in the positive direction. The actual input voltage may exceed V_{CC} tor three reasons: there may be inductive overshoot in badly terminated systems; the V_{CC} pin may be floating or grounded; or the input pin may be forced high by electrostatic discharge or incoming inspection testing.

For the inductive overshoot case, when the pin voltage exceeds V_{CC} part of the Q1 collector current begins to flow from the pin through limiting resistor R1 and Schottky diode D2. The current from V_{CC} through D1 decreases by exactly this amount, since Q2 is a constant current source. As the voltage continues to rise, D1 becomes reverse biased and prevents high currents flowing from the pin into V_{CC}. All the Q2 current flows into the pin through the R1–D2–Q1–Q2–R2 path to ground. As stated before, this current is typically small, in the range of 0.1mA to 1.0mA, and nearly independent of pin voltage, as shown by the I_I plateau in Figure 7. I_I provides a clamping action to ground for pin voltages in excess of V_{CC} which is usually desirable to reduce overshoot.

For the case where V_{CC} is grounded or floating, the input current is nearly zero for positive voltages between zero and approximately 7V. The conducting path through R1–D2–Q1 is available, but the current source Q2 will be shut off because, without V_{CC} drive, the Q2 base reference V_{CS} will be at 0V. This is the specified standard setup for incoming inspection. For the incoming inspection testing case where V_{CC} is connected to a 5V source, the response is shown in Figure 7. The current remains on the Q2-limited plateau until the pin voltage is high enough to cause non-destructive collector-emitter reach-through of Q2. At this point, input current increases as the pin voltage rises and R1 functions to limit this current and prevent damage to Q2.

The electrostatic discharge case is similar to the incoming inspection case except that Q2 may be off if the V_{CC} pad is floating, in which case it breaks down at a slightly higher voltage. The NPN input produces

reach-through at a relatively low voltage compared with the diode input. The effect of this non-destructive reach-through is to greatly increase the ability of the device to survive electrostatic discharge. The discharge current is passed through the chip at a relatively low power dissipation, and this is shared by elements R1, D2, Q1, Q2 and R2, so that none of them dissipate enough power to do damage. By way of contrast, with a diode input, the clamp Schottky diode breaks down at high voltage with high dissipation in a localized area, and may suffer damage.

Another advantage of the NPN input is its ability to interface on the chip to either a conventional TTL interior design, or to the increasingly popular current-mode interior logic. The conventional TTL interface is shown in Figure 6. In this case the Q2 current source is designed to provide sufficient current to insure that in the Low state, with current flowing through the R3–D4–Q2 path, the base-emitter stack of Q3–Q4 is shut off. The $2V_{BE}$ input threshold is set by the forward drops of Q1, D4, Q4 and Q3.

The current-mode logic interface is shown in Figure 5. The output voltage is the drop across R3, and is referenced to V_{CC} (or some on-chip regulated voltage lower than V_{CC}) as is required for current-mode logic. For this case, voltage reference REF2 is normally fixed at $2V_{BE}$ + 1 Schottky drop to provide a pin threshold voltage of $2V_{BE}$. In fact, REF2 can be tailored to set the switching threshold voltage to any desirable level; it can be set to something other than an integral number of base emitter drops, or it can be designed to reduce the sometimes undesirable temperature variations of input threshold.

INPUT CONSIDERATIONS

Static Input Current

A comparison of input current for various input voltage ranges for each of the three types of inputs is shown in Figure 8.

The majority of FAST devices available to date have diode inputs and supply current to their drivers that may be as large as 600μA at V_{IN} of 0.5V for a single unit load input. If a driver cannot sink the necessary current for a particular number of loads, the system designer must either add a buffer circuit designed to drive with higher current, or switch to devices that have high-impedance inputs. These are available on many Signetics FAST designs, and are specified to have input current less than 20μA over the full switching range from 0V to V_{CC}. Typical input current for the NPN structure at room temperature is less than 1μA below switching threshold voltage and 3μA above threshold. Typical PNP input current is less than 10μA below threshold voltage and 1μA above threshold.

Input Capacitance

Input capacitance, measured using a small-signal variation about a static DC operating point, is usually the least for the NPN. When one includes the added capacitance of the elements common to each input, such as the pin, pad, bond wire, and clamp Schottky diode, the percentage difference for total static input capacitance for any of the three types of inputs is not very large.

Dynamic Input Current

In many applications the total current an input pin draws during a switching transition is a more important consideration than its input capacitance. This dynamic input current is often larger than the value of static capacitance would predict because each of the three types of input structure normally includes some sort of speed-up mechanism, usually a "kicker" Schottky diode, connected to an internal node of the circuit. The kickers deliver current, related in a non linear way to input edge-rates. High-dynamic input current does not always equate to fast circuit switching. NPN inputs are usually faster than diode or PNP inputs, but in general have the lowest total dynamic current. The percentage differences for dynamic current tend to be larger than the respective differences for static capacitance.

Switching Threshold Voltage

The FAST input switching threshold voltage is set quite high for TTL at two base-emitter junction forward-bias drops. FAST input structures have enough gain that the voltage range in which they switch from one state to the other, as shown by a static DC transfer function curve, is completed within about 100mV of the $2V_{BE}$ threshold. For a typical part at room temperature, V_{BE} is about 800mV, and the switching threshold is nominally at 1.6V; the static transfer range uncertainty of about 100mV gives a nominal threshold for solid Lows and Highs of about 1.55V and 1.65V respectively. The FAST threshold voltage was chosen higher than other TTL families to give a larger noise margin with respect to ground, and to be more nearly centered in the region where a FAST output driver stage switches with maximum edge rates, which occurs between about 0.6V and 2.6V.

Because the FAST threshold is set by the base-emitter junction voltage, it is dependent on junction temperature and current density. V_{BE} increases by about 1.2mV for each degree Celsius drop in junction temperature; current density changes by about a decade for a 60mV change in V_{BE} The total variation due to processing differences, temperature, and current density is about 150mV per junction, or 300mV total change in input threshold to give limits of 1.25V Low and 1.95V High. The FAST V_{IL} and V_{IH} limits are 0.8V and 2.0V respectively, a tight spec for V_{IH}.

HYSTERESIS CONSIDERATIONS

Hysteresis has frequently been added to the inputs of TTL circuits in the past. The purpose is to increase noise immunity, which is accomplished by adjusting threshold voltages in a direction to reinforce an input level once a critical value has been reached. The procedure works well for slow circuits where the likelihood of slow, noisy inputs is high. It does not accomplish what is intended for FAST parts. There are several reasons: FAST threshold is already high and well centered so noise problems are automatically minimized. Inductive ground bounce, which is discussed at length later, causes problems with fast edge rates that completely swamp the typical benefits of hysteresis. It thus becomes a further complication in an already complicated picture and is more apt to hurt noise margins than to help. Because of this, the two major suppliers of FAST have eliminated hysteresis circuits except those specifically designed as Schmidt triggers; the 'F13, 'F14, and 'F132.

INPUT VOLTAGE RANGE	INPUT CURRENT		
	DIODE	PNP	NPN
Below Ground	Schottky Clamp	Schottky Clamp	Schottky Clamp
Ground to V_T	High (to 600μA)	Low (to 20μA)	Leakage
V_T to V_{CC}	Leakage	Leakage	Low (to 20μA)
Above V_{CC}	Leakage	Leakage	Clamp 100 to 1000μA

Figure 8. Input Current for Input Voltage Ranges

ELECTROSTATIC DISCHARGE (ESD) CONSIDERATIONS

It is universally true that no bipolar integrated circuit process can provide devices with such high breakdown voltages that they are able to withstand ESD without some structure punching through or breaking down. The necessary condition for survival when this occurs is that the energy dissipation in any volume of the chip must be kept low enough so that neither the silicon nor the interconnecting metal can melt. This can be accomplished in two ways: the breakdown voltage should be as low as practical, consistent with normal circuit operation, and the energy should be dissipated in as large a volume as is possible. Circuit components that are particularly sensitive to charge damage must be protected by structures that are less fragile. All Signetics FAST parts are designed with these requirements in mind, and although, as a rule of thumb, a sophisticated oxide-isolated process used to fabricate these parts tends to be more ESD damage-prone than a junction-isolated process, FAST is about as rugged as other TTL families in general. If FAST parts are handled with the same care afforded any other high-technology parts, they will not be damaged.

ESD sources usually fit into one of two categories: people or other objects that have accumulated static charge and touch the parts; or, they generate their own charge, as is the case when a circuit makes sliding contact with an insulator. In the first instance, static voltages tend to be high, over 10,000V, and discharge is usually limited by relatively high series resistance. In the second case, voltages are lower, around 200V, but there is very little series resistance to limit discharge current. Both possibilities are simulated with discharge models that are used in the majority of the test setups, and parts are designed in a way to improve survival for both ESD conditions.

Experience has shown that inputs of TTL circuits are much more likely to suffer ESD damage than outputs. Since negative voltages are discharged through clamp ground diodes with low chip dissipation, only voltages positive with respect to substrate ground are apt to produce input damage.

Circuits with diode inputs have a positive voltage breakdown in the relatively high range of from 15V to 25V. Schottky diodes connected to an input pin usually break down before junction diodes, and if they are stressed beyond their limits the Schottky diodes usually sustain damage in the corners. A diffusion guard-ring around the diode increases the uniformity of the breakdown, and as a result maximizes the dissipation volume at break-down and increases the ability of the device to survive ESD. All Signetics FAST circuits have guard-rings on Schottky diodes that connect to input or output pins.

NPN inputs are designed to have low holdoff voltage for positive voltages in excess of V_{CC}. Under static discharge the input structure forward biases, and the current-source transistor conducts the ESD current to substrate with a relatively low collector-emitter reach-through voltage. The input current for normal operation is low enough that a series limiting resistor can be added; this limits ESD current, especially for the case where the ESD source has no appreciable series resistance itself.

As processes improve, it is often possible to improve ESD protection. Most new releases and many parts that have been recently redesigned onto new processes have specific ESD structures included which protect up to 2000V for the standard resistance limited case – the human body model.

FLOATING INPUTS

FAST inputs should not be allowed to float. All unused inputs, even those on unused gates, should be tied to a voltage source of relatively low impedance that will get them out of the logic picture and out of trouble. For a Low input this can be ground, or the output of a permanently low driver. For a High input this can be V_{CC}, protected by a series resistor if circuit damaging voltage spikes are possible in the system, or a permanently high driver.

Properly tied High or Low inputs will not pick up enough spurious noise to cause problems. If they are allowed to float, the results can be disastrous. Floating diode inputs usually pull to within a few Mv of $3V_{BE}$ above ground, a V_{BE} above threshold. The input voltage will fall about 1V per 0.1mA of current that is capacitively coupled from an adjacent Low-going pin. Since pin-to-pin input capacitance is in the order of one pF for an IC in a PC environment, an adjacent pin falling at 1.0V/ns couples in about 1.0mA of current, enough to switch the input to a Low state for as long as the current lasts. The normal FAST circuit response will be to switch or oscillate. The problem is even worse for high-impedance low-capacitance NPN or PNP inputs. In this case the static voltage to which they float is determined in part by leakage, and is not predictable.

To reiterate, FAST inputs must not be allowed to float. To do so is to invite serious system problems.

OUTPUT CONSIDERATIONS

The purpose of the output stage is to supply current to a load to force it to a High state or to sink current from the load to force it to a Low state. The speed at which the load can be switched from one state to the other depends on how much supply current or sink current is available from the output driver. There must be an amount in excess of that which is required to maintain the static load voltage, and it is the excess current that is available to charge or discharge the load capacitance. Most FAST circuits are designed to fit into one of those categories, based on output drive capability; the normal output stage, the buffer driver which can supply approximately twice as much current, and the high current drivers designed to drive low-impedance terminations.

Both normal drivers and buffers may be 3-State, which means that, in addition to Low and High states, they can be forced to a high-impedance OFF state as a third possible choice. This allows multiple components to be connected to a bus simultaneously, with only the single-selected device providing actual drive capability.

The basic components of an output stage are shown in Figure 9.

The pull-down drive-components sink load currents to force a Low state at the output pin; the pull-up driver components supply current to force a High state. The control components turn on the selected driver and turn off the nonselected driver in response to the logic input signal. For 3-State parts, the control components turn off both drivers if the 3-State control signal is active. The output Schottky clamp is included to suppress inductive undershoots, and is a part of every FAST circuit. The load requires a static current to keep it in either a logic High or Low state. The drivers must also charge and discharge the load capacitance C_L, which is generally one of the major factors that influence switching speed.

Since to a large extent, they function independently of each other, the pull-up driver, pull-down driver and control blocks are discussed independently.

PULL-UP DRIVERS

Open-Collector

The simplest pull-up driver consists of no more than a fixed pull-up resistor tied to V_{CC}. For this case, the control stage interacts only with the pull-down driver. In the Low state, this must sink the current from both the pull-up resistor and load. In the High state, the pull-up resistor must supply all of the load current. Most often, the pull-up resistor is not physically a part of the integrated circuit chip itself, but is added externally. In this case the only circuit element connected to the output pad (in addition to the ever-present Schottky clamp) is the collector of the pull-down driver transistor, hence the name "Open-Collector." Parts with this output stage can be tied together for bus applications. If any of the connected pull-down stages is active, it will pull the bus Low; only if all of them are off can the external resistor pull the bus High. This action provides a "wired" logical function that is free in the sense that no additional components are required to achieve it. Some Open-Collector FAST parts also have 3-State inputs that serve to disable output pull-down stages regardless of the action of the normal logic function.

The Open-Collector output voltage depends on the load, the value of the pull-up resistor, and the voltage to which this is connected. If the resistor value is Low, the output will rise to nearly the full value of the pull-up source voltage; in particular, the Open-Collector output can rise to V_{CC}, a voltage higher than that obtainable with a standard Darlington totem-pole pull-up.

High-drive Open-Collector parts are ideal as drivers for terminated transmission lines. In this application the line is terminated at the receiving end with a resistor network that provides the proper impedance and an equivalent source voltage of about 3V. The circuit pull-down drive sinks the termination current through the line at relatively low chip power dissipation when it is on. When it is turned off, the line pulls the output high, charging the stray capacitance from an impedance equal to the line characteristic impedance. Since the current is supplied by the line, the chip power dissipation falls. Very fast rise times approaching 1ns can be obtained with this scheme. Rise times, in general, for open-collector outputs are determined by the R_c product of the pull-up resistor and the stray capacitance, and are limited only be the ability of the chip to pull the load Low.

Signetics has a new family of parts designed specifically for driving heavy loads in terminated or unterminated environments. The majority of these are Open-Collector functions. They are discussed in detail later.

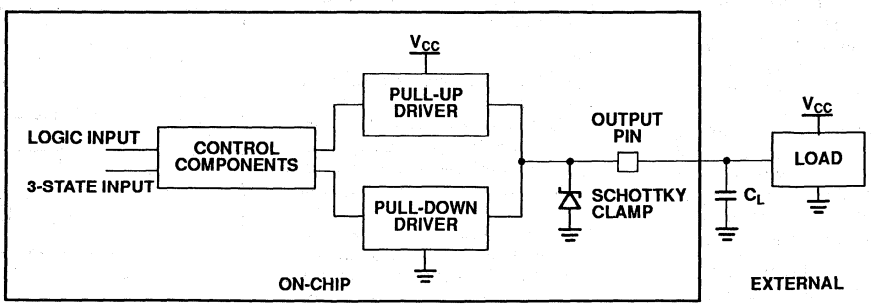


Figure 9. Output Stage Basic Components

Standard Darlington

Most FAST pull-up drivers use dual transistors, connected as shown in Figure 10, with the emitter of the first device Q_b delivering current to the base of the driver Q_a. This configuration is called a Darlington circuit and provides a composite current gain nearly as large as the product of the current gains of Q_b and Q_a.

The major advantage of the Darlington pull-up, as compared to the Open-Collector, is that the pin is actively pulled high by the emitter-follower action of Q_a which is capable of supplying large currents to quickly charge output capacitance. Despite the large output current that is available, the drive requirements of Q_b are low, so that the voltage drop across R_c is small, and the pad will pull up to a voltage nearly as high as V_{CC} $-2V_{BE}$.

For the case where the output pin voltage is High, the phase-splitter transistor Q_c is off, and the base of Q_b is pulled high by resistor R_C. The current which flows through R_C is just sufficient to provide base drive to Q_b. The base voltage of Q_b will be just slightly below V_{CC}, and the output pin voltage will be less than this by the sum of the V_{BE} drops of Q_b and Q_a, both of which are on. Most of the base current for Q_a and the current through pull-down resistor R_b is supplied from V_{CC} through R_a and Q_b. Q_b has a Schottky clamp to prevent saturation when the current through R_a is large. Resistor R_a limits the amount of current flowing from V_{CC} through Q_a to a value small enough that Q_a will not be damaged if the output pin is accidentally grounded for a short period of time. This short circuit output current is called I_{OS}, and its value is approximately the maximum current available to charge the output capacitance at the beginning of a Low-to-High transition. The minimum current available when the pin has reached the minimum guaranteed high voltage V_{OH} is called output high current (I_{OH}). and is specified to be either 1mA or 3mA, depending on the type of driver. The maximum output voltage that the pull-up driver can achieve occurs at maximum V_{CC} and at high temperatures with corresponding low values of transistor V_{BE} and high current gain. Conversely, the minimum high voltage occurs at low V_{CC} and low temperatures.

In the Low state, the pull-down driver Q_d is on and the pin voltage is the Q_d saturation voltage V_{SAT}. Q_c is on and its collector resistor R_c is pulled down to V_{BE} + V_{SAT}; the V_{BE} of Q_d, V_{SAT} of Q_c. Q_b is also on, with its emitter at V_{SAT}, and the current through R_b is low. The base-emitter voltage of Q_a is nearly zero and Q_a is off.

The rate at which the pull-up driver can force a Low-to-High transition depends on a number of factors. The first, and obvious, consideration is that the control components must turn off the pull-down driver very quickly. During the short time that both pull-up and pull-down are on, there is a large feed-through current spike that is wasted as far as switching the load is concerned; it also increases chip power dissipation and produces undesirable voltage spikes in V_{CC} and ground. Assuming the pull-down is off, the Low-to-High transition speed is governed by: 1) the rate at which R_c can pull-up the base of Q_b; 2) the amount of pin current required to drive the load and charge the load capacitance; 3) the value of R_a; 4) the physical size and current gain of Q_a; and 5) the amount of Q_a base drive current that is lost through R_b to ground. The amount of R_b drive current lost can be reduced by connecting R_b to the output pin instead of ground, and this is done in a number of FAST parts. For this case, the static current through R_b with the pin high is less than if R_b is grounded, but switching feed-through current spike for a High-to-Low transition may be increased because R_b cannot effectively pull-down the base of Q_a until after the pin voltage falls.

The pin can be driven above its maximum high value by an external pull-up or by positive reflections from a transmission line. When this happens, Q_a and Q_b do not have sufficient base-emitter drive to keep them on. If the pin voltage rises significantly above

V_{CC} Q_a will begin to leak current into V_{CC}. For the case where R_b is tied to the pin instead of ground, the reverse transistor action of Q_a allows a high pin-to-V_{CC} current. This is not usually a problem in normal operation, but should be avoided in system applications where the V_{CC} pin may be intentionally grounded.

3-State

For all 3-State FAST parts, the leakage paths to a grounded V_{CC} pin are blocked with Schottky diodes. A typical 3-State pull-up is shown in Figure 11. S_a is the series Schottky blocking diode. 3-State Schottkys S_{t1} and S_{t2} serve to simultaneously turn off the pull-up and pull-down drivers. The 3-State control is active when it is pulled low to within V_{SAT} of ground. In this state it sinks all the available drive current for Q_b and Q_c and pulls their bases down to (V_{SAT} + $V_{Schottky}$) which is essentially one V_{BE}. The voltage drop across R_c is large and 3-State power dissipation is typically high. Q_a and Q_b are off for normal TTL voltage ranges of the output pin; a negative undershoot large enough to drive the pin about one V_{BE} below ground will allow them to turn on and supply current from V_{CC}; this action aids the clamping Schottky diode in preventing the pin voltage from falling lower.

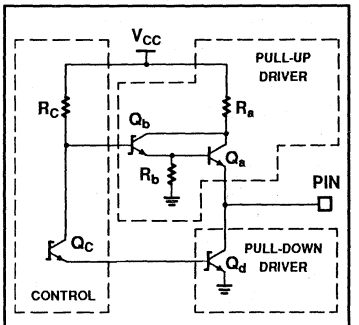


Figure 10. Basic Darlington Pull-Up

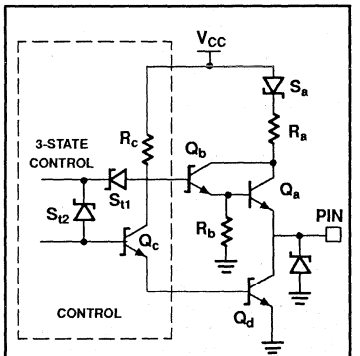


Figure 11. Basic 3-State Pull-Up

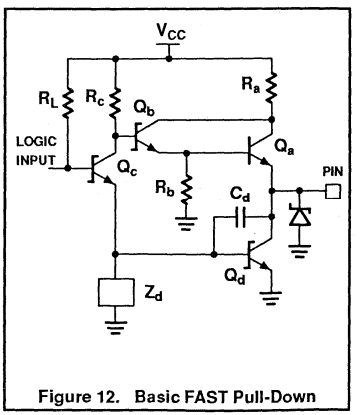


Figure 12. Basic FAST Pull-Down

PULL-DOWN DRIVERS

The basic FAST pull-down driver is shown in Figure 12. Q_d is the pull-down driver transistor, a big Schottky-clamped device capable of sinking large currents. C_d is the stray base-collector capacitance of Q_d, and its unavoidable presence has an important effect on the performance of the pull-down driver Q_c is the Schottky-clamped phase splitter. It functions as a current-limited, low-impedance driver for Q_d when the logic input voltage V_{IN} is high, and as an inverting driver for pull-up Q_b by virtue of the current through R_c when V_{IN} is low and Q_c is off. Z_d is the pull-down impedance network which insures that Q_d is off when V_{IN} is low.

Switching to the logic Low state occurs when V_{IN} is larger than the V_{BE} drops of Q_c plus Q_d. both of which are initially on. Part of the total emitter current available from Q_c comes from R_c which has a voltage drop of $V_{CC} - V_{BE} - V_{SAT}$. The remainder of the Q_c emitter current is supplied through its base Schottky clamp or by other components not shown in Figure 12 but discussed in the section on control components. A portion of the total Q_c emitter current is lost in the pull-down network Z_d; the remainder is available as base current for pull-down driver Q_d. The amount of current Q_d can sink depends on its base drive, its current gain, and its collector voltage. This current is specified on a per-part basis in the data sheets at output low voltage (V_{OL}) of 0.5V. The current which Q_d can sink in the switching range with the pin voltage at 2.5V is called available current (I_{AVL}). and is usually at least 70mA for FAST. The manner in which this current varies as the pin voltage decreases from 2.5V to V_{OL} is not specified as a FAST family parameter, since it is critically dependent on circuit design for a particular part, but is included as a specification for selected parts, especially those tailored to drive transmission lines. Several innovative circuit improvements that increase I_{AVL} by increasing the drive current for Q_d are shown in Figures 19a and 19b. Speed-up Schottky diodes S_{s1} and S_{s2} have been added to the standard pull-down circuit as shown in Figure 13a. Both are reverse-biased and off in the High state, since R_c pulls the collector of Q_c nearly to V_{CC}. Both connect the collector of Q_c to nodes that need to be discharged during a High-to-Low transition. S_{s1} to the base of Q_a, S_{s2} to the pin. They will conduct if these node voltages are higher than $V_{BE} + V_{SAT} + V_{Schottky}$, or approximately $2V_{BE}$; they are quite effective above $2V_{BE}$. Other networks are available which function down to lower voltages; these are especially useful for transmission line drivers. Figure 13b shows a dynamic kicker that gives an impulse of current which is especially useful in discharging high capacitive loads.

The network of elements labeled Z_d in Figure 12 is the pull-down impedance which insures that Q_d is off when the value of V_{IN} falls below $2V_{BE}$. When the voltage at the base of Q_d is being pulled high by Q_c or low by Z_d, the output pin voltage responds by moving in the opposite direction. This produces a change in voltage across C_d, which is the sum of the base voltage change and the collector voltage change, so the amount of charge required by C_d is magnified by a factor which is larger than unity.

This well-known Miller-effect causes the apparent value of C_d, as perceived by the drivers, to be a factor of about five times larger than the already large physical junction capacitance, all of which means that the drivers Q_c and Z_d need to supply or sink much more current during an output transition than is necessary to maintain static conditions. When static conditions do exist internally in the circuit, noise voltage spikes on the output pin, V_{CC} or ground can momentarily force the base of Q_d in the direction to produce a serious output glitch, and the drivers must respond quickly to counter this coupled noise.

The simplest Z_d element is a resistor R_{Z1} tied to ground, as shown in Figure 14. It will pull the base of Q_d all the way down to 0V if V_{IN} is less than one V_{BE}. This provides good immunity to coupled noise, but slows down the High-to-Low pad transition somewhat because the base of Q_d must rise a full V_{BE} before the output can begin to change. The value of R_{Z1} needs to be relatively large to prevent a serious loss of base drive current when Q_d is on, which makes it easier to capacitively couple voltage spikes to the base of Q_d and, in part, nullifies the good noise immunity the full V_{BE} swing provides.

The addition of a series Schottky diode solves most of the problems. This is shown in Figure 15. The Q_d base voltage cannot pull below a Schottky drop, so the switching speed is unimpaired. The value of R_{Z2} can be less than R_{Z1} for the same current when the base is high, so the effect of coupled charge is less and the noise margin is acceptable.

The circuit of Figure 16 is standard with many TTL families. It pulls the base of Q_d down even less than does $R_{Z2} - S_{d2}$, but it has a relatively high dynamic impedance and is somewhat noise sensitive. It has the advantage that it tends to "square up" the input voltage-to-output voltage transfer function, hence its popular name "squaring circuit." It is frequently used in simple gates where the shape of the transfer function may be important. For more complicated circuits, where there are one or more stages of logic with gain between input and output pins, the squaring ability is pretty much lost; in fact, it is likely that high-gain, multiple-logic level FAST circuits will oscillate if the input voltage is held at near threshold for any length of time.

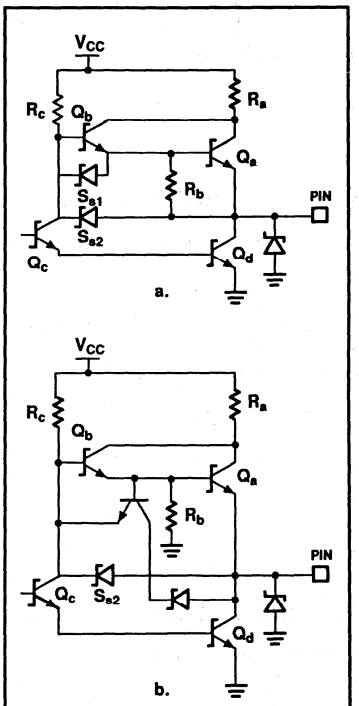


Figure 13.

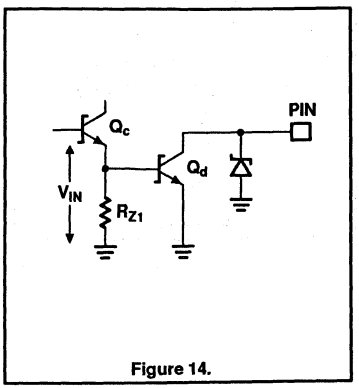


Figure 14.

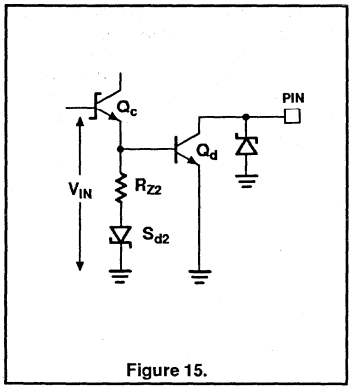


Figure 15.

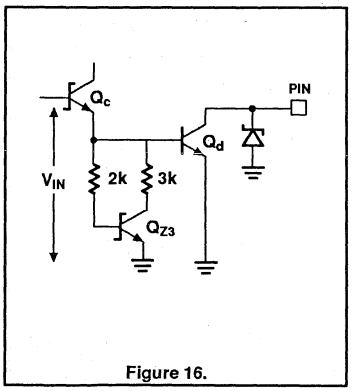


Figure 16.

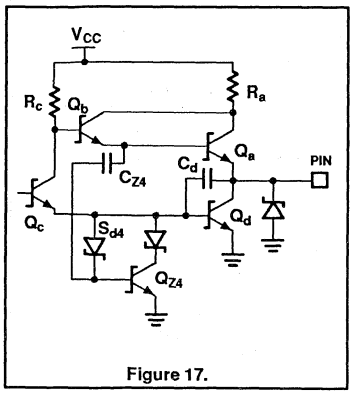


Figure 17.

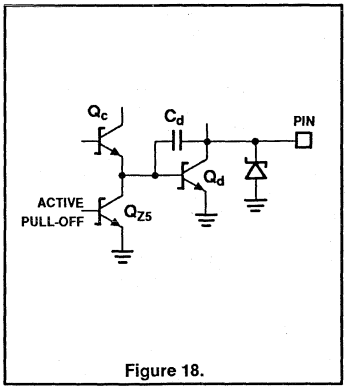


Figure 18.

Figure 17 shows a popular dynamic circuit that is used in conjunction with a resistor or squaring circuit pull-down, and which insures that C_d cannot couple enough charge to the base of Q_d to slow down a Low-to-High transition. In operation, as the emitter of Q_b rises, charge is coupled through C_{Z4} into the base of Q_{Z4} which turns on and shunts the Miller current flowing through C_d to ground. When the transition is finished, the current through C_{Z4} stops and Q_{Z4} turns off. When the High-to-Low transition of Q_b occurs, C_{Z4} discharges through S_{d4}. Because Q_{Z4} reduces the problems associated with Miller current, the circuit is called a "Miller Killer."

Figure 18 shows an active pull-down for the base of Q_d. The drive for Q_{Z5} (not shown) must be generated from the same signal that drives the base of Q_c. When Q_c is on, Q_{Z5} must be off, and when Q_c is off, Q_{Z5} turns on to hold the base of Q_d low. The impedance is very low, eliminating the capacitive-coupling noise problem.

CONTROL COMPONENTS

This section covers 3-State control drivers, special 3-State problems, and V_{CC} turn-on current and 3-State glitches during power-up.

3-State Control Drivers

The normal TTL 3-State scheme is shown in Figure 11 . The 3-State control voltage in the OFF state is high enough that S_{t1} and S_{t2} are reverse-biased; in the active state the control voltage is low, usually V_{SAT}, so that the Q_a–Q_b base emitter stack is off, as is the Q_c–Q_d stack In the 3-State mode, R_c is dissipating maximum power. Blocking Schottky diode S_a. prevents current from flowing backwards through Q_a if the V_{CC} pin is grounded; the output pin high voltage can be about 4.5V before there is any significant 3-State leakage current. The only exception to this general rule with FAST is for the diode input transceiver function, where the same pin acts as an input or an output. In this case, the pin supplies one or more normal FAST unit loads of current if it is Low, and tends to pull to $2V_{BE}$ if it is floating. NPN and PNP input transceivers have normal low 3-State leakage.

There are several innovative improvements to the basic 3-State circuit, as shown in Figure 19. The addition of inverter $Q_{c2} - R_{c2}$ with a blocking Schottky S_{c2} allows the addition of feedback diodes S_{s1} and S_{s2} to increase I_{AVL}; S_{c2} cannot be included in series with R_{c1} because its forward voltage drop would lower V_{OH}. 3-State power is not increased, since only one R_{c1} is pulled low. The current through Q_{c2} is available as added base drive to Q_d. So nothing is wasted. An additional transistor may be paralleled with Q_{c1} and Q_{c2} to control an active pull-down version of impedance Z_d which, discussed in a previous section, eliminates the Miller turn-on problem.

I_{CC} Considerations

There is no formal family specification that limits the amount of V_{CC} current a FAST circuit may draw during turn-on as V_{CC} rises from zero to 4.5V. However, for most new designs, and especially for circuits that have high I_{CC} requirements, an effort has ben made to limit maximum turn-on I_{CC} to 110% of I_{CCmax}. This precaution prevents an undesirable system situation where the V_{CC} power supply is large enough to drive the devices, but can't power them up. The major component of turn-on current is V_{CC} to ground feed-through of output stages. Unless specific steps are taken to prevent it, the pull-up Darlington turns on if V_{CC} is greater than $2V_{BE}$, and remains on until the on-chip voltage is high enough to set the phase splitter solidly in one or the other of its two states. The solution is to incorporate extra circuit components that will set the phase splitter at voltages nearly as low as $2V_{BE}$, or turn off the top device with a separate 3-State type structure which activates at low V_{CC}

voltages and becomes inoperative when V_{CC} is high.

The amount of current that can be fed from an output pin back into a grounded V_{CC} pin, or through the chip to ground for an open V_{CC} pin, depends on the design. Generally, 3-State feedback current is specifically limited to low values which are leakage or break-down related. Other parts have medium to high current. Those with Darlington pull-downs connected to the output pin conduct the most.

Some 3-State parts, especially selected buffer functions, have additional circuit elements to insure that as they power on they source or sink no appreciable output current, provided that the 3-State control pins are in the active state as V_{CC} rises. This means that V_{CC} can be turned on or off at will in the system to conserve power, and bus voltages will not be affected. Parts with this capability are identified in the specific data sheets.

GROUND VOLTAGE AND OTHER NOISE PROBLEMS

Ground Voltage As a Serious Problem

Excessive ground noise voltage in a system usually produces serious degradation of switching speed. It may also produce unwanted glitches on outputs, or spurious clocks which cause flip-flops to lose data, or relaxation oscillations that completely disrupt a system. It is, without doubt, one of the major causes of logic systems failure... difficult to accommodate, and difficult to eliminate.

The problem is not unique with FAST, but is greatly aggravated by the high transition rates and large currents for which FAST is designed. Because of this, FAST can optimally replace other TTL families only in systems that have been carefully designed at the PC board level. Well planned layout is vital, and multi-layer boards with ground and V_{CC} planes are often necessary. Great care must be taken to insure adequate bypassing for V_{CC}. The problems are not trivial, but they can be solved satisfactorily to yield systems whose performance is not exceeded in the TTL world.

Sources of Ground Noise

Ground lead inductance is the source of most ground noise voltage; it causes a voltage drop proportional to the rate at which the current through it changes.

Inductance is a measure of the amount of energy stored in the magnetic field associated with a current. Low values of inductance imply low energy, which means low voltage required to affect a change in current. As a general rule, inductance decreases as current is allowed to spread out in space, and current interactions decrease. The inductance of a thin wire far removed from the return current path is high; that of a large conductor coaxially encircled by the return path is low. Inductance tends to increase faster than linearly with conductor length, but only approximately logarithmically with decreasing cross-section dimensions. From a logic system viewpoint, ground planes are better than ground traces; wide lines are better than narrow lines; close spacing to planes is good; loops that allow magnetic flux linkages are bad; wire lengths of fractions of inches count; and sockets with long pins add significant inductance to a PC card.

Ground noise voltage is increased by feed-through current spikes. These occur when both top and bottom devices of the output totem-pole driver are on simultaneously, and heavy currents are allowed to flow directly from V_{CC} to ground. They can be minimized in one of two ways: drive the devices such that one is turned off before the other can turn on, or more commonly, drive them together, but very fast, so the feed-through current can flow for only a short time.

Although most ground noise results from ground inductance, resistance also contributes. Static ground offsets unrelated to rates of current change occur, and add to the total ground voltage. Generally speaking, those measures which reduce ground inductance also reduce ground resistance.

Estimating The Magnitude of Ground Noise

The accurate modeling of ground noise related problems in logic design is a complex procedure that requires numerical analysis to determine system currents and voltages as a function of time. This can only be accomplished in a satisfactory manner it one has reasonable electrical models, especially for input stages and output drivers of the integrated circuits used in the system. These data are available on request for many of the FAST logic functions. Signetics is prepared to assist customers in solving the sometimes formidable problems associated with large system simulation.

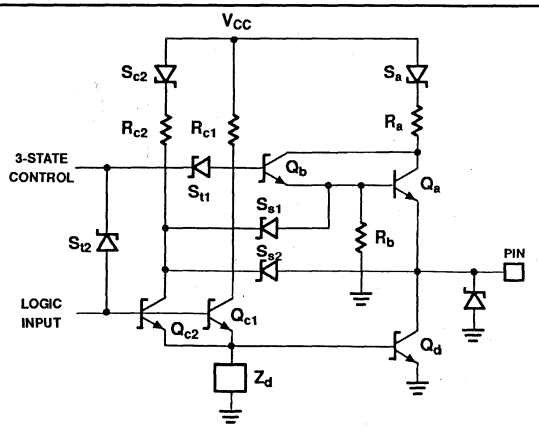


Figure 19. Improved 3-State Circuit

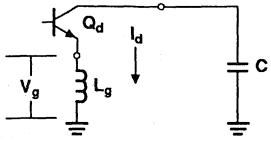


Figure 20.

The following discussion derives the minimum peak-value of ground noise that will occur as an integrated circuit discharges a capacitor through ground lead inductance. It points out the minimum problems that will exist. In the real world, the peak ground voltage will always be larger than the simple derivation predicts.

The load capacitor C and its discharge path are shown in Figure 20. The capacitor has been previously charged to a positive voltage, and is discharging through pull-down transistor Q_d and lead ground inductance L_g. As the current changes, it develops a ground voltage V_g across L_g that is equal to the product of L_g times the rate at which it changes.

The discharge current I_d will vary with time: starting from zero, it will increase to a maximum value, and then eventually return to zero. There are an infinite number of ways I_d can vary, depending on how the transistor allows charge to flow at any instant in time, but each of the possible current-versus-time discharge curves must define the same area, equal in value to the total charge Q that is removed from the capacitor as its voltage falls by an amount V.

The voltage drop V_g across the inductor at any instant in time will be determined by the slope of the current-versus-time curve, that is, by the rate at which current is changing. The unique curve that has the required area and minimum slope is triangular, as shown in Figure 21. The ground voltage for this case is a square wave as shown in Figure 22. It will be positive while the current is increasing, and negative when the current is decreasing.

The equations of interest in estimating V_g are:

$$\text{Charge} = Q = CV = I_{MAX} T/2 = \text{triangle area}$$

$$\text{Ground voltage} = V^g = (\text{triangle slope})(L) = \frac{2 I_{MAX} L}{T}$$

Combining the two equations to eliminate I_{MAX} gives:

$$V_g = \frac{4CVL}{T^2}$$

This lower limit of peak ground voltage will always be exceeded in the real world, where ground voltages are usually spikes, not square waves. If a spike is large enough and long enough, the chip will erroneously recognize it as a valid input, and respond either by glitching, slowing down, clocking incorrectly, or oscillating.

An example using values typical for a FAST circuit in a 16-pin DIP illustrates the potential for trouble. If the circuit discharges one standard FAST load of 50pF in 2ns with a voltage change of 3V through a ground inductance of 10nH, the minimum ground voltage will be:

$$V_g = \frac{4 \times 50 \times 10^{-12} \times 3 \times 10 \times 10^{-9}}{(2 \times 10^{-9})^2} = 1.5V$$

This value is high, and suggests that if transition times are not to be seriously degraded, inductances must be kept as small as possible, and loads must be minimized.

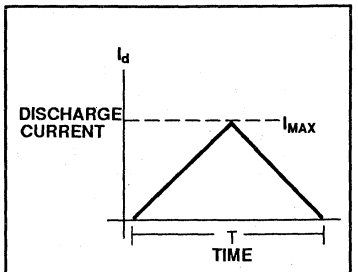


Figure 21.

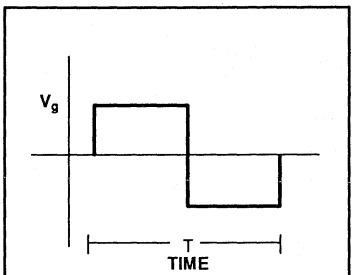


Figure 22.

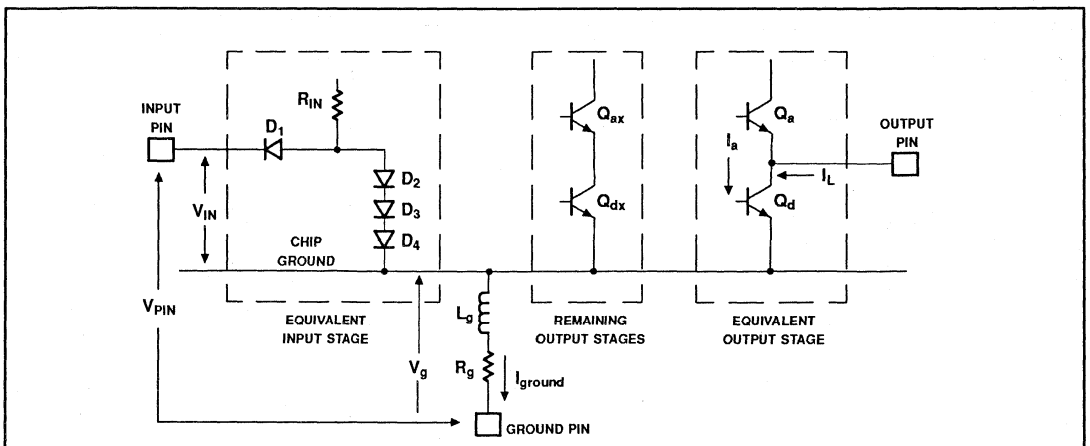


Figure 23. Equivalent Input and Output Stage

Effects of Ground Noise on Input Stages

FAST TTL input voltages are referenced to system ground as illustrated in Figure 23 which shows an equivalent input and output stage. The equivalent input circuit is represented by R_{IN} and the four diodes D1 through D4. These components establish an input switching threshold voltage of $2V_{BE}$ relative to chip ground. The on-chip voltage V_{IN} must be different from this value by a margin large enough to guarantee a static Low or High with sufficient overdrive to insure switching speed. The on-chip voltage V_{IN} that is actually available is the difference between the input pin voltage V_{PIN} and the total ground voltage noise V_g. V_g is the sum of the steady state voltage due to ground current flowing through R_g, and the inductive voltage drop across L_g. The inductive voltage is usually the larger of the two, and since it depends on current changes, it will have both positive and negative polarities for each switching cycle. This means that either Low or High input voltages which are too close to switching threshold will allow the noise margin to be exceeded, and if the ground voltage noise persists long enough, the input will switch erroneously. The result of this depends on the chip function. Combinatorial logic usually slows down or produces output glitches. Latches and flip-flops may be clocked inadvertently, and stored data will be lost. Complex circuits that have multiple outputs may oscillate, particularly if one polarity of ground noise results in a rapid change of ground current that produces the opposite polarity ground noise.

Ground noise adds a dimension of difficulty in measuring input threshold voltage. FAST parts are guaranteed to have input thresholds between the limits 0.6V and 2.0V. A typical method of verifying this is to determine the voltage at which the input actually switches. This requires some care, since the true threshold voltage is masked by any noise voltage contributed by the test system or ground inductance. For accurate results, the input pin voltage should approach the switching threshold slowly and smoothly. At threshold the input will switch. Sensing this point is easy for those circuits where an output also switches, glitches, or oscillates. It is much harder to sense this point for those circuits where an input change produces no output change, for example, with flip-flops which change state only when clocked. The input switch point for these devices can be inferred by measuring the input current as a function of input voltage. Clocking the part may produce enough ground noise to distort the measurement, even if the output doesn't switch.

Effects of Ground Noise on Output Stages

The most obvious effect that ground noise has on output stages is to directly change the voltage available to force discharge current through the pull-down device. If the only source of ground voltage is from the particular output of interest, the ground and output pin inductances will always slow down a High-to-Low transition. They produce a voltage in opposition to the output pin voltage at the beginning of the discharge when currents tend to be high and voltage changes rapidly. As discharge continues, the available drive decreases, and currents increase less rapidly. Eventually the current begins to fall, and the ground voltage reverses polarity, which tends to limit the rate at which the current decreases. If currents have been high, and the inductances are large, there may be substantial undershoot at the end of the switching cycle which can drive the output pin below ground.

If multiple outputs are switching simultaneously, the total ground noise needs to be considered to determine the result for a particular output. For this case, it can happen that ground noise will, in fact, speed up an output; on the other hand, it may introduce delays that are much larger than those possible with single output switching. This behavior makes it difficult to predict, except on a case by case basis, what the actual effects of multiple output switching will be. Curves of delay versus multiple switching have been published, but these serve only as rough guides to indicate potential problems, and need to be backed up with actual analysis for any particular application.

In addition to the direct influence on discharge voltage, excessive ground noise can affect the operation of the control components, and alter both rise and fall times by driving pull-up or pull-down stages incorrectly. One example of this can be understood with reference to Figure 24. The scenario is that the output pin is Low, but on the verge of switching High, with V_{IN} falling and Q_c ready to turn off. A problem occurs if, at the instant before the pull-up transistor Q_a turns on to pull the output pin high, the voltage from output pin to chip ground falls. This can happen as a result of inductive undershoot driving the output pin down, or by a rise in ground voltage caused by currents completely unrelated to the output of interest. The low output-pin-to-chip-ground voltage pulls down the emitter of Q_c through Schottky clamp diode S_d, and if V_{IN} is not low enough to counteract this, Q_c will not turn off. The net result is that R_c cannot rise, and the transition is delayed until the noise voltage from output to ground disappears.

V_{CC} Noise As an Additional Problem

Inductance in the V_{CC} lead produces noise in the on-chip V_{CC} voltage that is entirely analogous to ground voltage. The effects of V_{CC} noise can be nearly as harmful as those produced by ground noise, the only significant difference being the fact that TTL input voltages are referenced to ground instead of V_{CC}. If multiple outputs are switching simultaneously, the total ground noise needs to be considered to determine the result for a particular output. For this case, it can happen that ground noise will, in fact, speed up an output; on the other hand, it may introduce delays that are much larger than those possible with single output switching. This behavior makes it difficult to predict, except on a case by case basis, what the actual effects of multiple output switching will be. Curves of delay versus multiple switching have been published, but these serve only as rough guides to indicate potential problems, and need to be backed up with actual analysis for any particular application.

The first symptom of excessive V_{CC} inductive voltage drop is a change in the edge rate for a Low-to-High transition. This will decrease if the on-chip V_{CC} falls, and increase if it rises. If the ground to V_{CC} voltage falls below a minimum value, internal circuit delays or glitches can occur, and functions with flip-flops or other storage elements may lose data. As is the case with excessive ground noise, FAST circuits may break into relaxation oscillation.

Because V_{CC} to ground voltage must remain above a minimum value to avoid logic errors and glitches, it is absolutely vital that V_{CC} to ground bypassing is adequate. This requires low inductance V_{CC} and ground PC traces, and low inductance bypass capacitors. FAST parts are guaranteed to function properly for low V_{CC} of 4.5V. This means that pin voltages must not fall below this value for any appreciable time: fractions of nanoseconds. V_{CC} system voltage should be close to the maximum guaranteed value for safe system design.

Designing To Reduce the Effects of Ground Noise

The typical 1.5V minimum value for ground noise, calculated in the preceding example, points out the possibility of noise-related problems when only one standard 50pF load is being driven by an output stage. Simultaneous switching of more than one such load obviously increases the risk of trouble, and raises the question of how an octal part can work at all. Fortunately, the real world, with careful PC layout, is not usually so grim.

The standard 50pF load is a lot of capacitance, chosen so one can estimate the chip response for a single output switching under conditions that approach worst case. On a modern PC board a wire trace that has 50pF stray capacitance is several feet long and looks like a resistive delay line instead of a lumped capacitor.

Traces on a PC card must be short to behave like lumped capacitance for an output stage. For this case, a major contributor to driver current is the load presented by the input stages of the driven circuits, and the associated stray capacitance As previously mentioned, the input current for FAST parts is related to edge rates, and is generally larger than the measured static value of input capacitance would predict. Because of this, the useful fan-out of FAST circuits may be more dependent on ground noise of drivers with heavy capacitive loads than on the amount of current available to a static DC load, which is the guaranteed data sheet value.

Most of Signetics' FAST parts are available in surface mount packages, and these have lower ground inductance than the standard DIP parts.

Inductance of output signal pins reduces the rate at which associated ground current can change, and this reduces ground noise voltage without a corresponding reduction of static output voltage. This inductance may be intentionally increased by adding trace length on the PC board; one needs to be careful, and anticipate the increase in output ringing during switching transitions

In summary, there are many potential problems that one can anticipate in logic systems with fast edge rates. Some of these are dependent on the available components and their respective packages, and the system designer must be certain that the demands made of them are not more than they can handle. A second major consideration is the system layout, especially from the standpoint of ground, V_{CC}, and signal lead inductance. If one is careful with PC design and layout, and chooses components wisely, FAST systems deliver performance second to none in the TTL world.

Heavy Current Drivers

Signetics has a new family of parts defined that are capable of driving currents much larger than those achieved with standard FAST parts.

The parts presently available are:

F3037	Quad 2-input NAND
F3038	Quad 2-input NAND, Open-Collector
F3040	Dual 4-input NAND
F30240	Octal Line Driver, Open-Collector
F30244	Octal Line Driver, Open-Collector
F30245	Octal Transceiver, Open-Collector
F30640	Octal Transceiver, Open-Collector

Others are in the planning stage.

The drivers are husky enough to assure incident wave-switching driving transmission lines with impedance levels as low as 30Ω. They are the best choice available for applications that need the ultimate in speed and drive capability.

All the parts use multiple center ground and V_{CC} pins. Special precautions have been taken to insure minimum feed-through current during switching, and this, coupled with the low V_{CC} and ground inductance, results in minimum V_{CC} and ground noise, and allows maximum edge-rate and speed.

The parts are available on several different packages, including ceramic. Because the power dissipation is application dependent, the user needs to choose a package and an environment carefully to be sure the maximum temperature ratings are not exceeded. These maximum ratings are part of the individual data sheets.

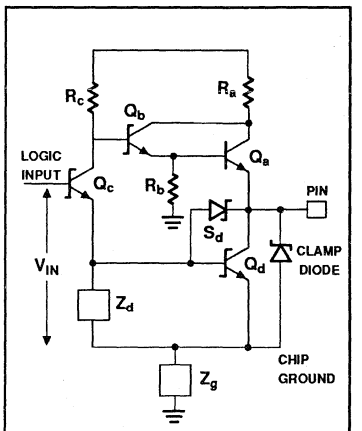


Figure 24.

Section 4
FAST User's Guide

FAST TTL Logic Series

CONTENTS

Data Sheet Specification Guide

SECTION 4
FAST USER'S GUIDE

INTRODUCTION

Signetics' FAST data sheets have been configured for quick usability. They are self-contained and should require minimum reference to other sections for amplifying information.

All references to military products have been deleted from this manual, specifically to reflect recent government requirements imposed via Revision C of MIL-STD-883, including the general provisions of Paragraph 1.2. Specifications for military-grade FAST products are included in the Military Products Data Manual available from the nearest Signetics Sales Office or Sales Representative.

TYPICAL PROPAGATION DELAY AND SUPPLY CURRENT

The typical propagation delays listed at the top of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part.

In the case of clocked product, this is sometimes the maximum frequency of operation. In any event, this number is under the operation conditions of V_{CC} = 5.0V and T_A = 25°C.

The typical I_{CC} current shown in that same specification block is the average current (in the case of gates, this will be the average of the I_{CCH} and I_{CCL} currents) at V_{CC} = 5.0V and T_A = 25°C. It represents the total current through the individual functions.

LOGIC SYMBOLS

There are two types of logic symbols. The conventional one, "Logic Symbol," explicitly shows the internal logic (except for complex logic). The other is "Logic Symbol (IEEE/IEC)" as developed by the IEC and IEEE. The International Electrotechnical Commission (IEC) has developed a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC3 is preparing a new document (Publication 17-12) that will consolidate the original work started in the mid-1960s and published in 1972 (Publication 117-15), and the amendments and supplements that have followed. Similarly, for the USA, IEEE Committee SCC11 has revised the publication IEEE Std 91/ANSI Y32.14-1973.

The updated version IEEE Standard Graphic Symbols for Logic Functions ANSI/IEEE Std 91-1984 (revision of ANSI/IEEE Std-1973) ANSI 732.14-1973 can be ordered through:

IEEE Service Center
445 Hoes Lane
Piscataway, New Jersey
Phone: (201) 981-0060

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it. There is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than -0.5V is applied to the output pin, after the voltage is removed, the part will not have been shorted.

Input and output voltage specifications in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction.

Absolute Maximum Ratings imply that any transient voltages, currents, and temperatures will not exceed the maximum ratings. Absolute Maximum Ratings are shown in Table 1.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has dual purposes. It sets environmental conditions (operating free-air temperature), and it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in these tables. Signetics feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment. If V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltage guaranteed by the DC Electrical Characteristics table. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs test the part for functionality in a "truth table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the part has assumed its final and correct output state. Thus, V_{IH} and V_{IL} should never be used in testing the functionality of any FAST part type. For these types of tests, input voltages of +4.5V and 0.0V should be used for the High and Low states, respectively.

TABLE 1. ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply Voltage		-0.5 to +7.0	V
V_{IN}	Input Voltage		-0.5 to +7.0	V
I_{IN}	Input Current		-30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Standard outputs	40	mA
		3-State outputs	48	mA
		All Buffer outputs	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" Highs and Lows during functional testing is done primarily to reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several feet. The situation in a system on a PC board is less severe than in a noisy production environment. Typical recommended operating conditions are shown in Table 2.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Signetics during their testing operations conducted under the conditions set forth in the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with V_{CC} = +4.7V, V_{IH} = 0.8V across the temperature range of 0°C to +70°C, and with an output current of I_{OH} = -1.0mA.

In this table, one sees the heritage of the original junction isolated Schottky family — V_{OL} = 0.5V at I_{OL} = 20mA. This gives the user a guaranteed worst case Low-state noise immunity of 0.3V. In the High state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the High state than in the Low state, more noise immunity is a useful state of affairs. Because the impedance of an output in the High state is generally much higher than in the Low state, more noise immunity in the High state is needed. This is because the noise source couples noise onto the output connection of the device. That output tries to pull the noise source down by sinking the energy to ground or to V_{CC} depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low-impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective as shunting the noise energy to V_{CC}, so than an extra 0.4V of noise immunity in the High state compensates for the higher impedance. The result is a nice balance of sink-and-drive current capabilities with the optimum amount of noise immunity in both states.

V_{OH} and V_{OL} values may vary depending on whether 5% or 10% V_{CC} swings are specified. The type of output structure, standard: 3-State, or buffer will also affect the value of V_{OH} and V_{OL}. Generally, as the output current and V_{CC} variation increase, the guaranteed minimum V_{OH} decreases and the maximum V_{OL} increases. Signetics specifies and tests V_{OH} and V_{OL} for both 5% and 10% V_{CC} swing.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at a guaranteed minimum input breakdown voltage. The test conditions for I_I vary according to the type of input structure being tested. Diode inputs are tested with the V_{CC} = MAX and 7.0V at the input. It is necessary to turn off V_{CC} for the NPN input test to measure leakage. Otherwise, the current source is on and the leakage is undetectable. When I_I is being measured on transceiver I/O pins, both V_{CC} and the input voltage is 5.5V. The reduced input voltage is necessary because of the output structure connected to the input structure. Output structures break down faster than input structures and it is impossible to test the input without testing the output also.

I_{IH} for both Diode and NPN input structures is less than 20µA typically. I_{IL} is less than 20µA for NPN inputs and less than 600µA for Diode inputs. If multiple structures are tied together in the design, then the input current values also multiply. The fan-out for the devices with NPN inputs is 30 times greater than those with Diode inputs. This means the output current sinking ability of the device driving the input to the Low state could be 30 times less when driving NPN devices. For transceiver I/O pins, the outputs are in the high-impedance state when the inputs are tested. Therefore, a maximum of 50µA extra leakage is allowed and combined with the I_{IH} and I_{IL} values. These tests are called I_{IH} + I_{OZH} and I_{IL} + I_{OZL} to more accurately describe the true measurement being made.

I_{OZH} is tested only on Open Collector outputs as a leakage test with setup conditions that would put the output in the High state if it were not in the 3-State high impedance condition. I_{OZL} is similar except the setup condition is for the Low state.

I_{OH} is tested only on Open Collector outputs as leakage test for the lower output transistor structure. Both V_{CC} and V_{OH} are at the same value so that there is not a current path to or from V_{CC} that would mask the leakage path.

Short circuit output current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that specification has totally changed. Originally, I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground, the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally induced malfunctions could occur after several seconds of sustained test.

TABLE 2. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min.	Norm.	Max.	
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage	Open Collector			4.5	V
I_{OH}	High-level output current	Standard			-1	mA
		3-State			-3	mA
		Buffer			-15	mA
I_{OL}	Low-level output current	Standard			20	mA
		3-State			24	mA
		Buffer			64	mA
T_A	Operating free-air temperature range		0		70	°C

Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the Low state. When the output is switched High, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to the new state of V_{OH}. At the instant the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. We now reach the critical point in our discussion. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0μF of line capacitance tied to the output, a load that is unrealistically high by several order of magnitude.

The effect of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious – *as long as that current is limited to a short duration.* If the hard short is allowed to remain, the full I_{OS} current will flow through the output state and may cause functional failure or damage to the structure. As test induced failure may occur if the I_{OS} test time is excessive. As long as the condition is brief, typically 50ms or less with ATE equipment, the local heating does not reach the point where damage or functional failures may occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging the capacitance. The Signetics data sheet limits for I_{OS} reflect the conditions that the part will see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment of test methods ground an output for too long a time, causing functional failure or damage. DC electrical characteristics are shown in Table 3.

AC ELECTRICAL CHARACTERISTICS

The AC Electrical Characteristics table contains the guaranteed limits when tested under the conditions set forth in the AC Test Circuits and Waveforms section. In some cases, the test conditions are further defined by the AC setup requirements (see Table 5) — this is generally the case with counters and flip-flops where setup and hold times are involved.

All of the AC Characteristics are guaranteed with 50pF load capacitance. The reason for choosing 50pF over 15pF as load capacitance is that it allows more leeway in dealing with stray capacitance, and also loads the device during rising or falling output transitions, which more closely resembles the loading to be expected in average applications, thus giving the designer more useful delay figures.

Although the 50pF load capacitance will increase the propagation delay by an average of about 1ns for FAST devices, it will increase several nanoseconds for standard Schottky devices.

The load resistor of 500Ω is conveniently specified as both a pull-up and pull-down load resistor.

FAST products are being released in the surface mounted SO package as a commercial option. Because of the reduced inductance inherent in this package, minimum propagation delays are being derated by 0.2ns. This is reflected by a note at the bottom of Table 4.

TABLE 3. DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]	LIMITS			UNIT	V_{CC}[4]
					Min.	Typ.[2]	Max.		
V_{IH}	High-level input voltage			Recognized as a High signal over recommended V_{CC} and T_A range	2.0			V	
V_{IL}	Low-level input voltage			Recognized as a Low signal over recommended V_{CC} and T_A range			0.8	V	
V_{IK} (V_{CD})	Input clamp diode voltage			I_{IN} = -18mA			0.8	V	
V_{OH}	High-level output voltage	Standard[5]	±10% V_{CC}	I_{OH} = -1mA	2.5	3.4		V	MIN
			±5% V_{CC}		2.7	3.4		V	MIN
		3-State	±10% V_{CC}	I_{OH} = -3mA	2.4	3.3		V	MIN
			±5% V_{CC}		2.7	3.3		V	MIN
		Buffers	±10% V_{CC}	I_{OH} = -15mA	2.0	3.2		V	MIN
			±5% V_{CC}		2.0	3.1		V	MIN
V_{OL}	Low-level output voltage	Standard[5]	±10% V_{CC}	I_{OL} = 20mA		0.30	0.5	V	MIN
			±5% V_{CC}			0.30	0.5	V	MIN
		3-State	±10% V_{CC}	I_{OL} = 24mA	2.4	0.35	0.5	V	MIN
			±5% V_{CC}		2.7	0.35	0.5	V	MIN
		Buffers	±10% V_{CC}	I_{OL} = 48mA	2.0	0.38	0.55	V	MIN
			±5% V_{CC}	I_{OL} = 64mA	2.0	0.42	0.55	V	MIN
I_I	High-level current breakdown test	Diode inputs		V_{IN} = 7.0V			100	µA	MAX
		NPN inputs		V_{IN} = 7.0V			100	µA	0.0V
		Transceiver I/O pins		V_{IN} = 5.5V			1.0	mA	5.5V
I_{IH}	High-level input current			V_{IH} = 2.7V (20µA × n High U.L.)			n(20)	µA	MAX
I_{IL}	Low-level input current	Diode inputs		V_{IL} = 0.5V (-0.6mA × n Low U.L.)			n(-0.6)	mA	MAX
		NPN inputs		V_{IL} = 0.5V (-20µA × n Low U.L.)			n(-20)	µA	0.0V
I_{IH} + I_{OZH}	High-level input current (I/O pins)			V_{IH} = 2.7V (20µA × n High U.L.)			n(20)+50	µA	MAX
I_{IL} + I_{OZH}	Low-level input current (I/O pins)	Diode inputs		V_{IL} = 0.5V (-0.6mA × n Low U.L.)			n(-0.6)	mA	MAX
		NPN inputs		V_{IL} = 0.5V (-20µA × n Low U.L.)			n(-20)-50	µA	MAX
I_{OZH}	3-State, High-level OFF current			V_{OUT} = 2.7V			50	µA	MAX
I_{OZL}	3-State, Low-level OFF current			V_{OUT} = 0.5V			-50	µA	MAX
I_{OH}	Open Collector output leakage			V_{OH} = 4.5V			250	µA	MAX
I_{OS}	Output short-circuit current	Standard[5], 3-State		V_{OUT} = 0V	-60		-150	mA	MAX
		Buffer driver			-100		-225	mA	MAX
I_{CEX}	Output High leakage current			V_{OUT} = 5.5V, not tested on NPN transceivers and Open Collector outputs			250	µA	MAX
I_{ZZ}	Bus drainage test			V_{OUT} = 5.5V, 3-State			500	µA	0.0V

NOTES:

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to V_{CC} = 5V, T_A = 25°C.
4. MIN and MAX refer to the values listed in the data sheet table of recommended operating conditions.
5. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.
6. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

TABLE 4. AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A=+25°C, V_{CC}=5V, C_L=50pF, R_L=500Ω			T_A=0°C to +70°C, V_{CC}=5V±10%, C_L=50pF, R_L=500Ω		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	13.0 8.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	12.0 8.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.5 6.0	ns ns
f_{MAX}	Maximum clock frequency	74F374	Waveform 1	100			70		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.5 7.5	2.0 2.0	12.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 6.5	ns ns

TABLE 5. AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A=+25°C, V_{CC}=5V, C_L=50pF, R_L=500Ω			T_A=0°C to +70°C, V_{CC}=5V±10%, C_L=50pF, R_L=500Ω		
				Min.	Typ.	Max.	Min.	Max.	
t_s (H) t_s (L)	Set-up time D_n to E	74F373	Waveform 4	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time D_n to E		Waveform 4	3.0 3.0			3.0 3.0		ns
t_w (H)	E Pulse width, High		Waveform 1	6.0			6.0		ns
t_s (H) t_s (L)	Set-up time D_n to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time D_n to CP		Waveform 5	2.0 2.0			2.0 2.0		ns
t_w (H) t_w (L)	CP Pulse width, High or Low		Waveform 1	7.0 6.0			7.0 6.0		ns

TEST CIRCUITS AND WAVEFORMS

The 500Ω load resistor, R_L to ground, as described in Figure 1, acts as a ballast to slightly load the totem-pole pull-up and limit the quiescent High-state voltage to about +3.5V. Otherwise, an output would rise quickly to about +3.5V, but then continue to rise slowly up to about +4.4V. On the subsequent High-to-Low transition, the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the Low state. Perhaps more importantly, the 500Ω load to ground can be a high frequency, passive probe for a sampling scope, which costs much less than the equivalent, high impedance probe. Alternately, the 500Ω load to ground can be simply a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Figure 2, Test Circuit for 3-State outputs, shows a second 500Ω resistor from the device output to switch. For most measurements this switch is open; it is closed for measuring a device with Open Collector outputs and for measuring one set of the enable/disable parameters (Low-to-OFF and OFF-to-Low) of a 3-State output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establish a quiescent High level of +3.5V, which correlates with the High-level discussed in the preceding paragraph.

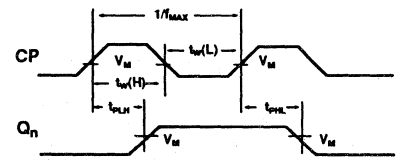
As shown in Figure 3, AC Waveforms for FAST 74F373 and 74F374, the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the quiescent level (i.e., Low for t_{PLH}[2] or High for t_{PHL}[2]).

Since the rising or falling waveform is RC-controlled, 0.3V of change is more linear and is less susceptible to external influences.

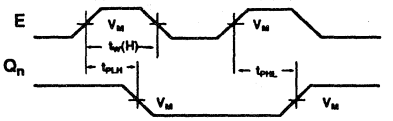
More importantly, from the system designer's point of view, 0.3V is adequate to ensure that a device output has turned OFF. It also gives system designers more realistic delay times to use in calculating minimum cycle times.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.5ns, and signal swing of 0V to +3.0V, 1.0MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters

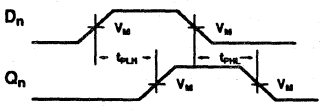
AC WAVEFORMS



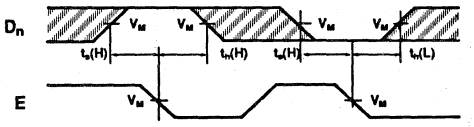
Waveform 1. Propagation Delay Clock to Output, Clock Pulse Widths, and Maximum Clock Frequency



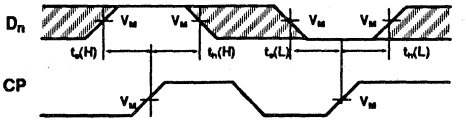
Waveform 2. Propagation Delay, Enable to Outputs and Enable Pulse Width



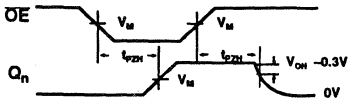
Waveform 3. Propagation Delay, Data to Outputs



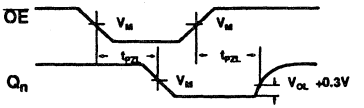
Waveform 4. Data Setup and Hold Times



Waveform 5. Data Setup and Hold Times

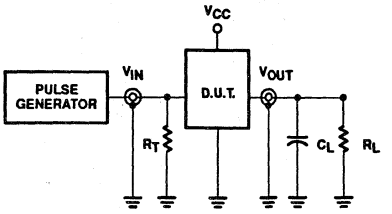


Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level



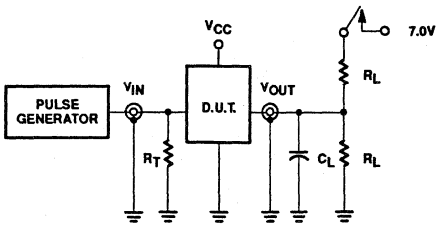
Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, VM = 1.5V. The shaded areas indicate when the input is permitted to change for predictable output performance.



DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 1. Test Circuit for Totem-Pole Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 2. Test Circuit for 3-State Outputs

DC SYMBOLS AND DEFINITIONS

Voltages – All voltages are referenced to ground. Negative voltage limits are specified as absolute values (i.e., -10V is greater than -1.0V)

V_{CC} **Supply voltage:** The range of power supply voltage over which the device is guaranteed to operate within the specified range.

V_{IKMAX} **Input clamp diode voltage:** The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.

V_{IH} **High-level input voltage:** The range of input voltages recognized by the device as a logic High.

V_{IHMIN} **High-level Minimum Input voltage:** This value is the guaranteed input High threshold for the device. The minimum allowed input High in a logic system.

V_{IL} **Low-level input voltage:** The range of input voltages recognized by the device as a logic Low.

V_{ILMAX} **Low-level Maximum Input voltage:** This value is the guaranteed input Low threshold for the device. The maximum allowed input Low in a logic system.

V_M **Measurement voltage:** The reference voltage level on AC waveforms for determining AC performance. Usually specified as 1.5V for the FAST family.

V_{OHMIN} **High-level output voltage:** The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OLMAX} **High-level output voltage:** The maximum guaranteed Low voltage at an output terminal sinking the specified load current I_{OL}.

V_{T+} **Positive-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T-} (Min).

V_{T-} **Negative-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T+} (Max).

Currents – Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply current:** The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst-case operation unless specified.

I_I **Input leakage current:** The current flowing into an input when the maximum allowed voltage is applied to the input.

I_{IH} **High-level input current:** The current flowing into an input when a specified High level voltage is applied to that input.

I_{IL} **Low-level input current:** The current flowing out of an input when a specified Low-level voltage is applied to that input.

I_O **Output current:** The output current that is approximately one half of the short-circuit output current (I_{OS}).

I_{OH} **High-level output current:** The leakage current flowing into a turned-off Open Collector output with a specified High-level output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the High-level state.

I_{OH1} **High-level output current:** The current necessary to guarantee the Low to High transition in a 30Ω transmission line on the incident wave.

I_{OL} **Low-level output current:** The current flowing into an output which is the Low-level state.

I_{OL1} **Low-level output current:** The current necessary to guarantee the High to Low transition in a 30W transmission line on the incident wave.

I_{OS} **Short-circuit output current:** The current flowing out of an output which is in the High-level state when that output is short-circuited to ground.

I_{OZH} **OFF-state output current High:** The current flowing into a disabled 3-state output with a specified High level output voltage applied.

I_{OZL} **OFF-state output current High:** The current flowing out of a disabled 3-state output with a specified Low level output voltage applied.

AC SYMBOLS AND DEFINITIONS

f_{MAX} **Maximum clock frequency:** The maximum input frequency at a clock input for predictable performance. Above this frequency the device may cease to function.

t_{PLH} **Propagation delay time:** The time between specified reference points on the input and the output waveforms with the output changing from the defined Low-level to High-level.

t_{PHL} **Propagation delay time:** The time between specified reference points on the input and the output waveforms with the output changing from the defined High-level to Low-level.

t_{PHZ} **Output disable time from High level to a 3-State output:** The delay time between the specified reference points on the input on the input and output voltage waveforms with the 3-State output changing from the High-level to a high impedance "OFF" state.

t_{PLZ} **Output disable time from Low level to a 3-State output:** The delay time between the specified reference points on the input on the input and output voltage waveforms with the 3-State output changing from the Low-level to a high impedance "OFF" state.

t_{PZH} **Output enable time to a Low level of a 3-State output:** The delay time between the specified reference points on the input on the input and output voltage waveforms with the 3-State output changing from a high impedance "OFF" state to a High-level.

t_{PZL} **Output enable time to a Low level of a 3-State output:** The delay time between the specified reference points on the input on the input and output voltage waveforms with the 3-State output changing from a high impedance "OFF" state to a Low-level.

t_s **Setup time:** The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_h **Setup time:** The interval immediately following the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_w **Pulse width:** The time between the reference point on the leading and trailing edges of a pulse.

t_{REC} **Recovering time:** The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_{TLH} **Transition time, Low to High:** The time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low to High.

t_{THL} **Transition time, High to Low:** The time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High to Low.

t_r, t_f **Clock input and rise and fall times:** 10% and 90% value.

Design Considerations

INTRODUCTION

The properties of high-speed FAST logic circuits dictate that care be taken in the design and layout of a system.

Some general design considerations are included in this section. This is not intended to be a thorough guideline for designing FAST systems, but a reference for some of the constraints and techniques to be considered when designing a high-speed system.

HANDLING PRECAUTIONS

As described in the circuit characteristics section, FAST devices are susceptible to damage from electrostatic discharge (ESD).

- Signetics FAST devices are shipped in conducting foam or anti-static tubes and foil-lined boxes to minimize ESD during shipment and unloading.
- Before opening the shipment of FAST devices, make sure that the individual is grounded and all handling means (such as tools, fixtures and benches) are grounded.
- After removal from the shipping material, the leads of the FAST devices should always be grounded. In other words, FAST devices should be placed leads-down on a grounded surface, since ungrounded leads will attract static charge.
- Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn on-off, do not exceed absolute maximum ratings.
- After assembly on PC boards, ensure that ESD is minimized during handling, storage or maintenance.
- FAST inputs should never be left floating on a PC board. This precaution applies to any TTL family. As a temporary measure, a resistor with a resistance greater than 10kΩ should be soldered on the input. The resistor will limit accidental damage if the PC board is removed and brought into contact with static-generating material.

INPUT CLAMPING

FAST circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative DC voltages or long duration, negative pulses. Certain FAST part types with the NPN base input structure also provide clamping of positive overshoots.

UNUSED INPUTS

Proper design rules dictate that all unused inputs on TTL devices be tied either High or Low. This is especially important with FAST logic.

Electrically open inputs can degrade AC noise immunity as well as the switching speed of the device. Small geometries make FAST more susceptible to damage by ESD than other TTL families. Tying inputs to V_{CC} or GND, directly or through a resistor, protects the device from in-circuit electrostatic damage. Additionally, while most unconnected TTL float High, FAST devices with NPN inputs float Low. FAST devices do not require an input resistor to tie the input High. Inputs can be connected directly to V_{CC} as well as ground.

Possible ways of handling unused inputs are:

1. Unused active-High NAND or AND inputs to V_{CC}. The inputs should be maintained at a voltage greater than 2.7V, but should not exceed the absolute maximum rating.
2. Connect unused active-High NOR or OR inputs to ground.
3. Tie unused active-High NAND or AND inputs to a used input of the same gate, provided that the High-level fan-out of the driving circuit is not impaired.
4. Connect the unused active-High NAND or AND inputs to the output of an unused gate that is forced High.

MIXING FAMILIES WITH OTHER TTL FAMILIES

Mixing the slower TTL families such as 74 and 74LS with the higher speed families such as 74F is possible but must be done with caution. Each family of TTL devices has unique input and output characteristics optimized to achieve the desired speed or power features.

The unique speed/power characteristics of FAST devices are achieved partially by the internal fast rise and fall times, as well as those at input and output modes. These fast transitions can cause noise of various types in a system. Power and ground line noise are generated by the faster transitions of the current in the output load capacitance. Signal line noise can also be generated by the fast output transitions.

The noise generated by 74F devices can be minimized in systems designed with shorter signal lines, good ground planes, well-bypassed power distribution networks, layouts that minimize adjacent signal lines that run parallel, and improved impedance matching in signal lines to reduce transmission line type reflections.

INPUT-OUTPUT LOADING AND FAN-OUT TABLE

For convenience in system design, the input-output loading and fan-out characteristics of each circuit are specified in terms of unit load and actual load value. One FAST Unit Load (U.L.) in the High state is defined as 20μA; thus both the input leakage current, I_I, and output High current-sourcing capability, I_{OH}, are normalized to 20μA.

Similarly, one FAST Unit Load (U.L.) in the Low state is defined as 0.6mA and both the input Low current, I_{IL}, and input Low current-sinking capability, I_{OL}, are normalized to 0.6mA.

For added convenience, the actual load value in amperes is listed in the column adjacent to U.L.

On some FAST devices, high-impedance NPN base input structure has been utilized. With this structure, the Low level input current, I_{IL}, has been reduced to 20μA. This characteristic is 30 times lower than the requirement of devices using the conventional input structure. This feature improves fan-out in the Low state and can help reduce part count in system design by eliminating buffers in some applications.

CLOCK PULSE REQUIREMENTS

All FAST clock inputs are buffered to increase their tolerance of slow positive-clock edges and heavy ground noise. Nevertheless, the rise time on positive-edge-triggered devices should be less than the nominal clock-to-output delay measured between 0.8 to 2.0V levels of the clock driver for added safety margin against heavy ground noise. Not only a fast rising, clean clock pulse is required, but the path between the clock drive and clock input of the device should be well-shielded from electromagnetic noise.

TABLE 1. LOADING COMPARISONS

DRIVING DEVICE FAMILY	I_{OL} (MIN.)	DRIVEN DEVICE FAMILY						
		74F	74F(NPN)	74LS	74	74S	8200/9300	82S00
		I_{IL} (MAX.)						
		0.6mA	20μA	0.4mA	1.6mA	2.0mA	1.6mA	0.4mA
		MAXIMUM NUMBER OF LOADS DRIVEN						
74F	20mA	33	1,000	50	12.5	10	12	50
74F(NPN)	64mA	106	3,200	160	40	32	40	160
74LS	8mA	13	400	20	5	4	5	20
74LS Buffer	24mA	40	1,200	60	15	12	15	60
74	16mA	26	800	40	10	8	10	40
74 Buffer	40mA	78	2,400	120	30	24	30	120
74S	20mA	33	1,000	50	12.5	10	12	50
74S Buffer	60mA	100	3,000	150	37.5	30	37	150

INPUT LOADING AND OUTPUT DRIVE COMPARISON

The logic levels of all TTL products are fully compatible with each other. However, the input loading and the output drive characteristics of each family are different and must be taken into consideration when mixing them in a system, Table 1 shows the relative drive capabilities of each family for commercial temperature and voltage ranges.

FAST OUTPUTS TIED TOGETHER

The only FAST outputs that are designed to be tied together are Open Collector and 3-State outputs. Standard FAST outputs should not be tied together unless their logic levels will always be the same; either High or Low. When connecting Open Collector or 3-State outputs together, some general guidelines must be observed.

Open Collector Outputs

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices devices must have a pull-up resistor(s) added between the OR-tie connector and V_{CC} to establish an active-High level. Only special high voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of the pull-up resistor is determined as follows.

$$R(Min) = \frac{V_{CC}(Max) - V_{OL}}{I_{OL} - N_2(I_{IL})}$$

$$R(Max) = \frac{V_{CC}(Min) - V_{OL}}{N_1(I_{OH}) - N_2(I_{IH})}$$

where:

I_{OL} = Minimum I_{OL} guarantee or OR tie elements.

$N_2(I_{IL})$ = Cumulative maximum input Low current for all inputs tied to OR-tie connection.

$N_1(I_{OH})$ = Cumulative maximum output High leakage current for all outputs tied to OR-tie connection.

$N_1(I_{IH})$ = Cumulative maximum input High leakage current for all outputs tied to OR-tie connection.

If a resistor divider network is used to provide the High level, the R(Max) must be decreased enough to provide the required [V_{OH}/R(pull-down)] current.

3-State Outputs

3-State outputs are designed to be tied together, but are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-State output should be active at any time. This generally requires that the output enable signals be non-overlapping. When TTL decoders are used to enable 3-State outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally guarantee when the address is changing.

Since most 3-State output enable signals are active-Low, shift register or edge-triggered storage registers provide good output enable buffers. Shift registers with one circulating Low bit, such as the 'F164 or 'F194, are ideal for sequential enable signals. The 'F174 or 'F273 can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from Low-to-High faster than from High-to-Low, the selection of one device at a time is assured.

GND

Good system design starts with a well thought out ground layout. Try to use ground plane if possible. This will save headaches later on. If ground strip is used, try to reduce ground path in order to minimize ground inductance. This prevents crosstalk problems. Quite often, jumper wire is used for connecting to ground at the breadboarding stage, but a solid ground must be used even at the breadboarding stage.

V_{CC}

Typical dynamic impedance of un-bypassed V_{CC} runs from 50Ω to 100Ω, depending on V_{CC} and GND configuration. This is why a sudden current demand, due to an IC output switching, can cause momentary reduction in V_{CC} unless a bypass (decoupling) capacitor is located near V_{CC}.

Not only is there a sudden current demand due to output switching transient, there is also a heavy current demand by the buffer driver. Assuming the buffer output sees a 50Ω dynamic load and the buffer Low-to-High transition is 2.5V, the current demand is 50mA per buffer. If it is an octal buffer, the current demand could be 0.4mA per package in 3ns time!

The next step is to figure out the capacitance requirement for each bypass capacitor. Using the previously mentioned octal buffer and assuming the V_{CC} droop is 0.1V, then C is:

$$C = 0.4A \times 3 \times 10^{-9}\ sec/0.1V$$
$$= 12 \times 10F^{9}$$

This formula is derived as follows:

$cQ = CV$

By differentiation:

$\Delta Q/\Delta t = C\Delta V/\Delta t$

since

$\Delta Q/\Delta t = i$

the equation becomes:

$i = C\Delta V/\Delta t$

hence

$C = i\Delta t/\Delta V$

Select the C bypass ≥0.02μF and try to use a high quality RF capacitor. Place one bypass capacitor for each buffer and one bypass capacitor every two other types of IC packages. Make sure that the leads are cut as short as possible.

In addition, place bypass capacitors on a board to care of board-level current transients.

CROSS-TALK

The best way to handle cross-talk is to prevent it from occurring in the first place; quick fixes are troublesome and costly. To prevent cross-talk, maximize spacing between signal lines and minimize spacing between signal lines and ground lines.

Preferably, place ground lines between signals. For added precaution, add a ground trace alongside either the potential corss-talker or the cross-listener.

For back-plane or wire-wrap, use twisted pair for sensitive functions such as clocks, asynchronous set or reset, or asynchronous parallel load. In flat cable, make every other conductor ground.

For multilayer PC boards, run signal lines in adjacent planes perpendicular to prevent magnetic coupling, and limit capacitive coupling. Use power shield (V_{CC} or ground plane) in between signal planes.

Since any voltage change, noise or otherwise, arriving at the unterminated end of transmission lines double in amplitude, even a partially terminated line reduces the amplitude of the signal (noise or otherwise) appearing at the end of the line; therefore, using a terminating resistor whose value is equal to the line characteristic impedance will help reduce cross-talk.

Section 5
Military Information

FAST TTL Logic Series

Military Information

SECTION 5

Effective January 1, 1985, this section has been superseded by the 1990 Military Products Data Manual, Volume 2, and the Suplement to Military Products Data Manual Volume 1, 1992. Information regarding this manual can be obtained from the Military Marketing Group at (408) 991-2722.

MILITARY STANDARD PRODUCTS

The Signetics Military product line offerings include Class B vendor standard products, as well as products qualified to standard military drawings. These products are designed to offer our customers the optimum of quality, reliability, delivery and cost. The benefits of these products provide our customers:

- Industry-wide standardization;
- Fewer custom specifications;
- Cost savings associated with larger lots;
- Better lead times by reducing specification negotiation time and allowing off-the-shelf procurement; and,
- Industry standard marking.

SIGNETICS CLASS B STANDARD PRODUCT (RB)

Signetics Class B standard product is offered for use when a DESC Drawing product is not available, or when program requirements allow the use of vendor standard product.

Class B standard product conforms to MIL-STD-883, general provisions Paragraph 1.2.1 (and its sub-paragraphs), except where noted (see the "Product Non-compliance" section of the Military Data Manual or Data Book). No other claims, express or implied, are made of equivalence to JAN product or to MIL-M-38510. Signetics compliant product also conforms with JEDEC Publication 101, except for marking content. Electrical test requirements are as stated in the most current *Signetics Military Data Manual* only.

- 100% final electrical tests include all Data Manual parameter limits, test conditions, and temperatures applicable to Subgroups 1, 2, 3, 7, and 9 of MIL-STD-883, Method 5004 for digital products, or to Subgroups 1, 2, 3, 4, and 9 for Linear products.
- Group A sample electrical inspection tests include all final electrical subgroups as well as all other Data Manual parameters with specified minimum or maximum limits.
- End point electrical tests used for QCI inspection sampling (Groups C and D) are those Data Manual parameter limits, test conditions, and temperatures applicable to Group A Subgroups 1, 2, and 3 per MIL-STD-883, Method 5005, or to Subgroup 1 for Linear products.

Data Manual parameters which have no specified minimum or maximum limits (typical performance only) are not tested. Parameters which have limits specified at 25°C only are tested only at that temperature. Detailed parameter assignment to subgroups and other test detail are contained in documented Signetics Internal Product Electrical specifications and are available upon request. Actual test program symbolics are available for customer review at the factory, but are considered proprietary and will not be copied or otherwise distributed outside of Signetics.

QCI Groups A and B testing are performed on all products and packages per MIL-M-38510 and MIL-STD-883, Method 5005. Signetics utilizes inline Group A and alternate Group B for all lines. QCI Groups C and D are routinely performed on all compliant families and package types.

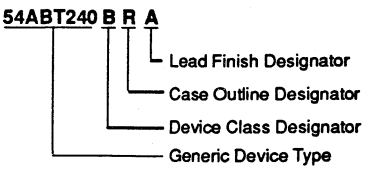
Waivers, deviations, or exceptions of an kind deemed necessary in the course of the contracts must be issued in accordance with DOD-STD-480. Should Signetics have knowledge of the need for waivers at the time of response to quote (RFQ) or order entry, that information will be transmitted prior to order entry.

Package types which do not have case outlines letters assigned in MIL-M-38510, Appendix C, will be assigned case outline letters per JEDEC Publication 101.

The Signetics standard Product Assurance Plan documentation is available for customer review at the factory, and is considered proprietary.

This category of product conforms to quality level B-2 of MIL-HDBK-217 (π_Q = 6.5).

For Class B Standard Product, the part number is listed as follows:



Section 6
74F Series Data Sheets

FAST TTL Logic Series

CONTENTS

* *Please see the Discontinued Product List in Section 1, page 8.*

Contents (Continued)

** Please see the Discontinued Product List in Section 1, page 8.*

Contents (Continued)

** Please see the Discontinued Product List in Section 1, page 8.*

Contents (Continued)

* *Please see the Discontinued Product List in Section 1, page 8.*

Contents (Continued)

** Please see the Discontinued Product List in Section 1, page 8.*

Quad 2-input NAND gate — 74F00

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F00	3.4ns	4.4mA

ORDERING INFORMATION

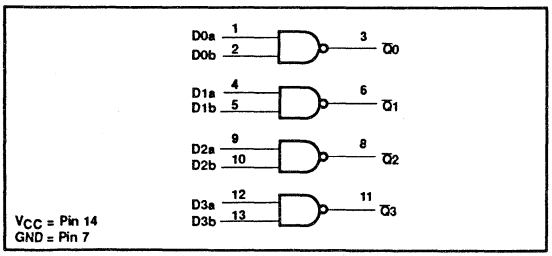
DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F00N	I74F00N
14–pin plastic SO	N74F00D	I74F00D

INPUT AND OUTPUT LOADNG AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$n	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

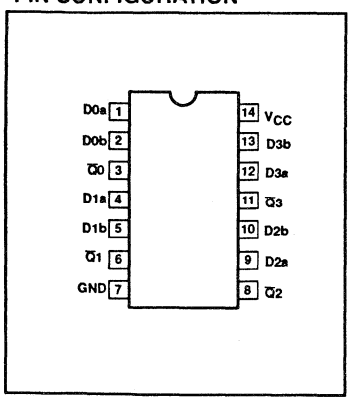


FUNCTION TABLE

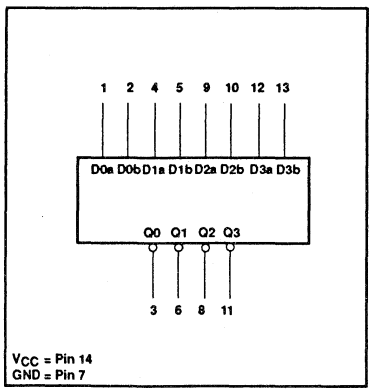
INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}$n
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
1. H = High voltage level
2. L = Low voltage level

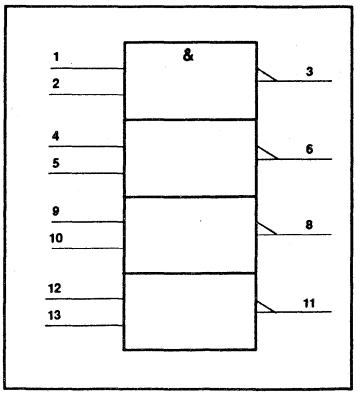
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.9	2.8	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		6.8	10.2	mA

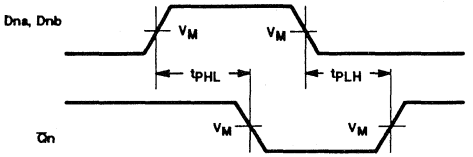
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	2.0 1.5	6.5 6.0	ns

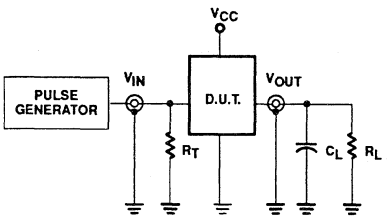
AC WAVEFORMS



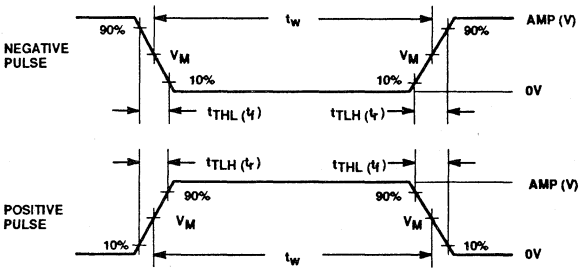
Waveform 1. Propagation delay for inverting outputs

Note: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORM



Test circuit for totem-pole outputs



DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Quad 2-input NOR gate — 74F02

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F02	3.4ns	4.4mA

ORDERING INFORMATION

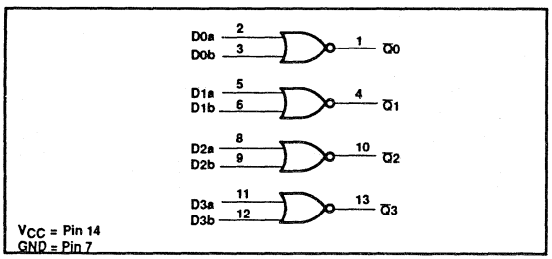
DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F02N	I74F02N
14–pin plastic SO	N74F02D	I74F02D

INPUT AND OUTPUT LOADNG AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}n$	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

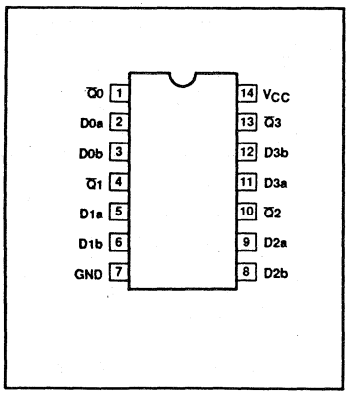


FUNCTION TABLE

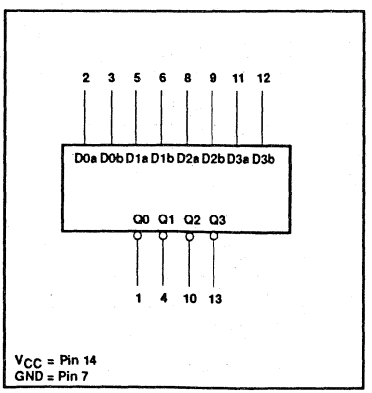
INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}n$
L	L	H
L	H	L
H	L	L
H	H	L

NOTES:
1. H = High voltage level
2. L = Low voltage level

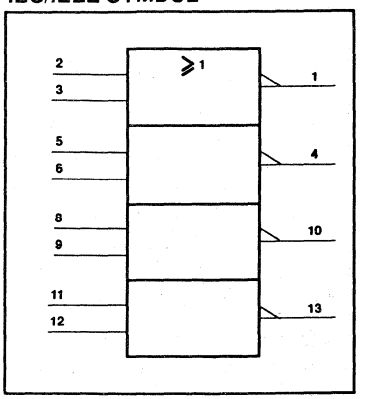
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]	I_{CCH}	V_{CC} = MAX			3.0	5.6	mA
		I_{CCL}	V_{CC} = MAX			7.0	13.0	mA

NOTES:

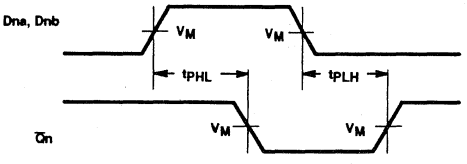
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	2.5 2.0	4.4 3.2	5.5 4.3	2.5 2.0	6.5 5.3	2.5 1.5	7.0 6.0	ns

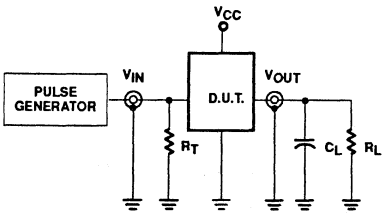
AC WAVEFORMS



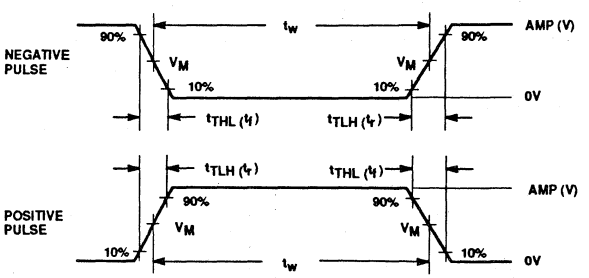
Waveform 1. Propagation delay for inverting outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORM



Test circuit for totem-pole outputs



Input pulse definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Hex inverter — 74F04

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F04	3.5ns	6.9mA

ORDERING INFORMATION

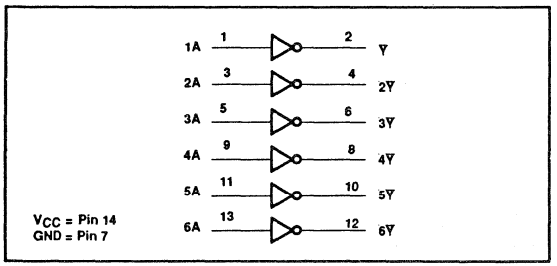
DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F04N	I74F04N
14–pin plastic SO	N74F04D	I74F04D

INPUT AND OUTPUT LOADNG AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA	Data inputs	1.0/1.0	20µA/0.6mA
nȲ	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

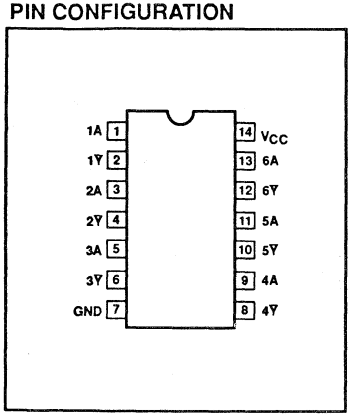


FUNCTION TABLE

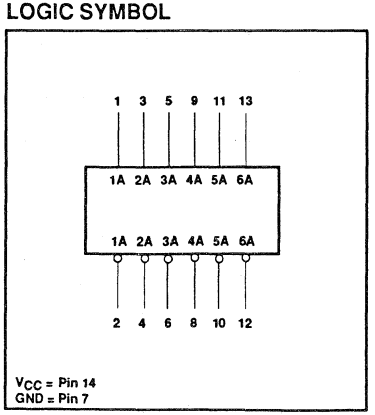
INPUTS	OUTPUT
A	Ȳ
L	H
H	L

NOTES:
1. H = High voltage level
2. L = Low voltage level

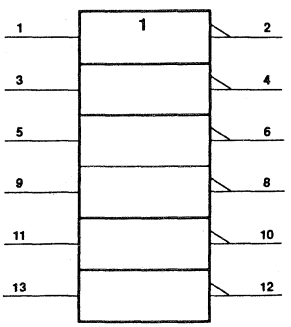
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		2.8	4.2	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		10.2	15.3	mA

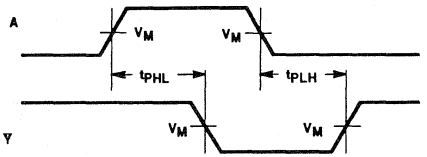
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A to $\overline{Y}$	Waveform 1	2.4 1.5	3.7 3.2	5.0 4.3	2.4 1.5	6.0 5.3	1.5 1.1	8.0 6.5	ns

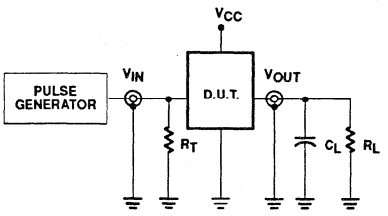
AC WAVEFORMS



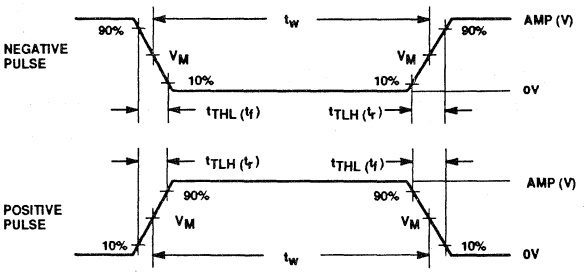
Waveform 1. Propagation delay for inverting outputs

Note to AC Waveforms
1. For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Inverter/buffer drivers — 74F06, 74F06A, 74F07, 74F07A

74F06 Hex inverter buffer/driver (Open Collector), 74F06A Hex inverter buffer/driver (Open Collector)
74F07 Hex buffer/driver (Open Collector), 74F07A Hex buffer/driver (Open Collector)

FEATURES FOR 74F06, 74F07

- Open Collector output drive 64mA
- High speed
- 12V output termination voltage
- Symmetrical propagation delays

FEATURES FOR 74F06A, 74F07A

- Open Collector output drive 48mA
- High speed
- 30V output termination voltage
- Replaces 7406 and 7407
- Improved performance upgrade for 7406 and 7407
- Reduced I_{OH} leakage @ 30V

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F06	3.5ns	30mA
74F06A	9.0ns	30mA
74F07	4.5ns	32mA
74F07A	10.0ns	32mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
14–pin plastic DIP	N74F06N, N74F06AN
14–pin plastic SO	N74F07D, N74F07AD

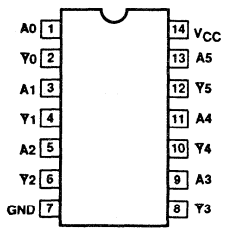
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/ LOW
An	Data inputs ('F06, 'F07)	1.0/1.0	20µA/0.6mA
An	Data inputs ('F06A, 'F07A)	1.0/0.7	20µA/0.4mA
$\overline{Y}$n	Data outputs ('F06)	OC/106.7	OC/64mA
$\overline{Y}$n	Data outputs ('F06A)	OC/80	OC/48mA
Yn	Data outputs ('F07)	OC/106.7	OC/64mA
Yn	Data outputs ('F07A)	OC/80	OC/48mA

NOTES:
7. One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.
8. OC = Open Collector

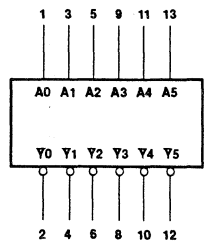
PIN CONFIGURATION

74F06/74F06A



LOGIC SYMBOL

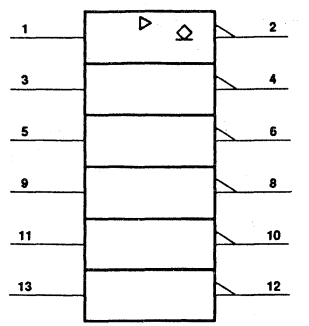
74F06/74F06A



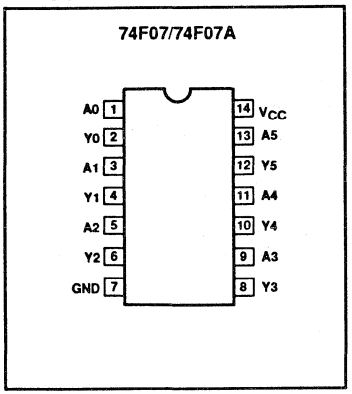
V_{CC} = Pin 14
GND = Pin 7

IEC/IEEE SYMBOL

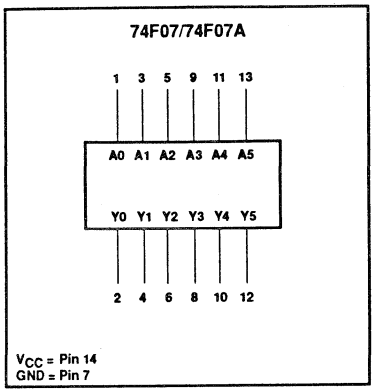
74F06/74F06A



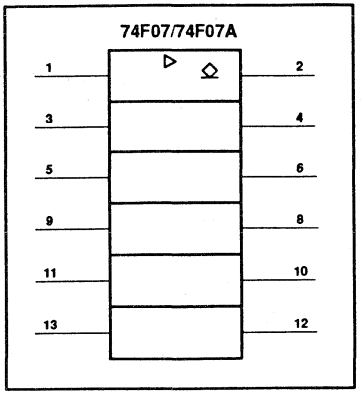
PIN CONFIGURATION



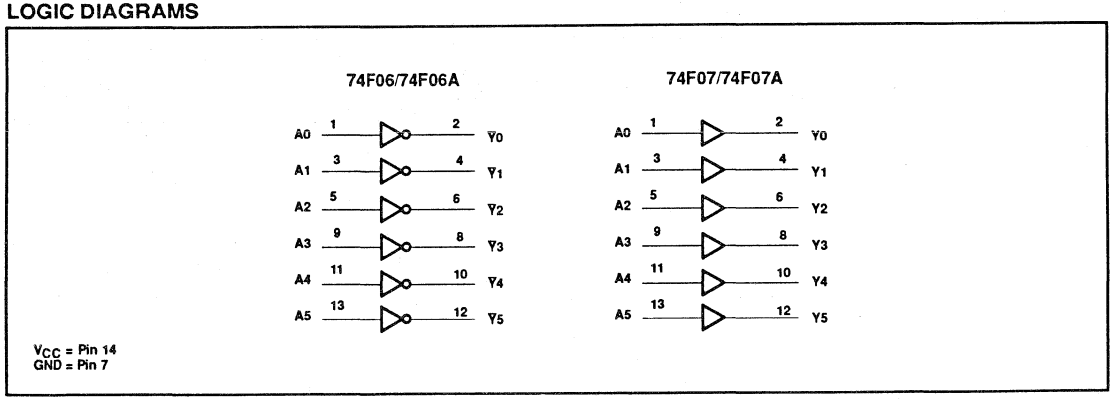
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAMS



FUNCTION TABLE

INPUTS	OUTPUTS	
	'F06, 'F06A	'F07, 'F07A
An	$\overline{Y}n$	Yn
L	H	L
H	L	H

NOTES:
1. H = High voltage level
2. L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	'F06, 'F07	–0.5 to 12	V
		'F06A, 'F07A	–0.5 to 30	V
I_{OUT}	Current applied to output in Low output state	'F06, 'F07	128	mA
		'F06A, 'F07A	96	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
V_{OH}	High–level output voltage	'F06, 'F07			12	V
		'F06A, 'F07A			30	V
I_{OL}	Low–level output current	'F06, 'F07			64	mA
		'F06A, 'F07A			48	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High–level output current	'F06, 'F07	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = MAX,					250	µA
		'F06A, 'F07A	V_{IH} = MIN					100	µA
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10% V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5% V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	'F06, 'F07	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
		'F06A, 'F07A						–0.4	mA
I_{CC}	Supply current (total)	74F06, I_{CCH}	V_{CC} = MAX				5.0	8.0	mA
		74F06A I_{CCL}					30	43	mA
		74F07, I_{CCH}					10	14	mA
		74F07A I_{CCL}					32	45	mA

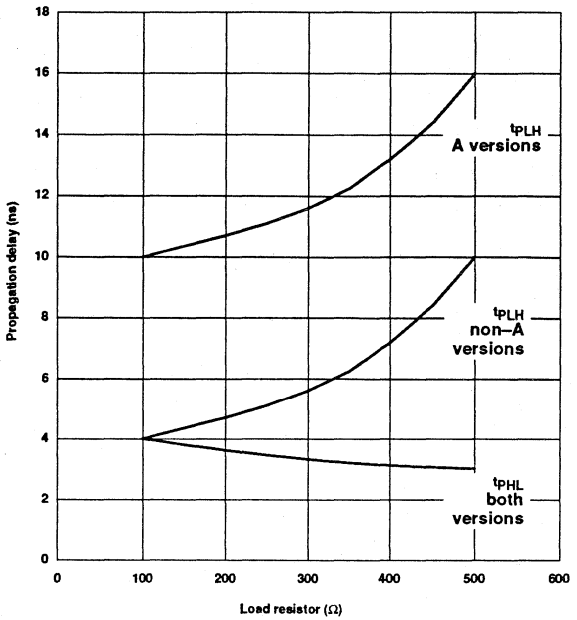
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

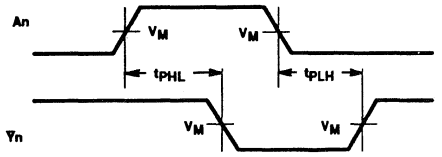
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 100Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 100Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}$n	'F06	Waveform 1	2.0 1.5	3.5 3.0	6.0 5.5	1.5 1.0	6.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}$n	'F06A	Waveform 1	5.0 2.0	9.0 4.0	11.0 6.0	4.0 2.0	15.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Yn	'F07	Waveform 2	2.0 3.0	4.0 5.0	6.0 7.0	2.0 2.5	6.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay An to Yn	'F07A	Waveform 2	6.0 5.0	10.5 7.5	13.0 10.0	5.0 4.0	17.0 13.0	ns

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

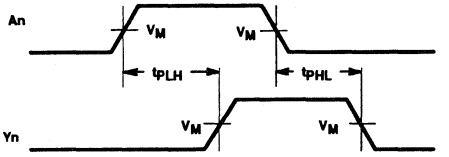


NOTE:
When using Open–Collector parts, the value of the pull–up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull–up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull–up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

AC WAVEFORMS



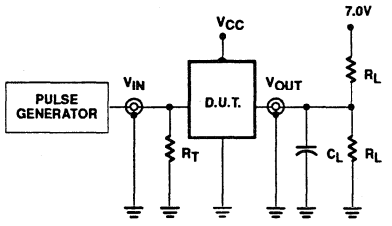
Waveform 1. Propagation delay for inverting outputs



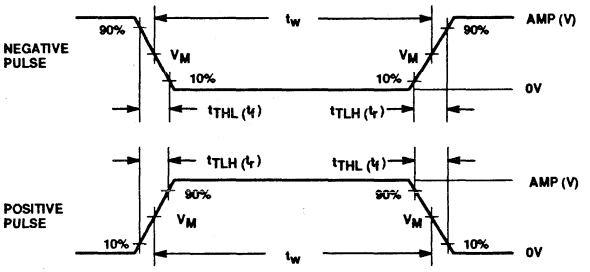
Waveform 2. Propagation delay for non–inverting outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for Open Collector outputs



DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0328
ECN No.	94536
Date of issue	September 19, 1988
Status	Product Specification
FAST Products	

FAST 74F08 Gate

Quad Two-Input AND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F08	4.1 ns	7.1 mA

FUNCTION TABLE

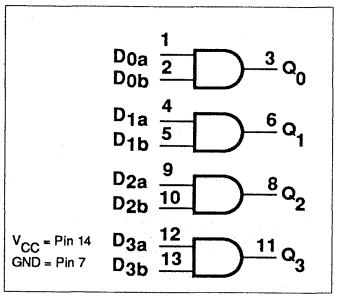
INPUTS		OUTPUT
D_{na}	D_{nb}	Q_n
L	L	L
L	H	L
H	L	L
H	H	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F08N
14-Pin Plastic SO	N74F08D

LOGIC DIAGRAM

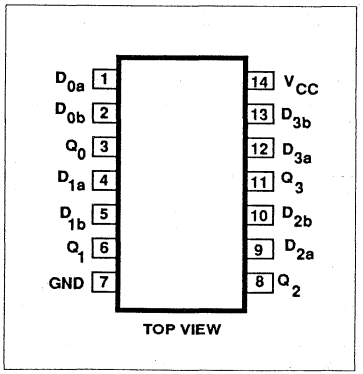


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

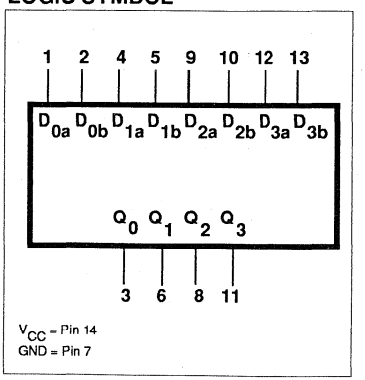
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20µA/0.6mA
Q_n	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

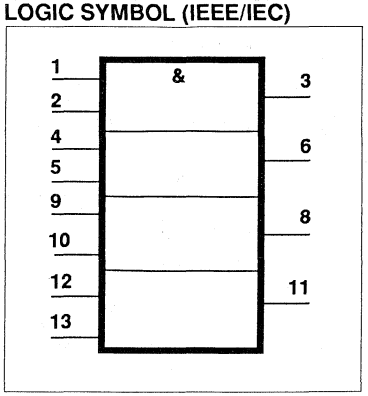
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=4.5V		5.5	8.3	mA
		I_{CCL}		V_{IN}=GND		8.6	12.9	mA

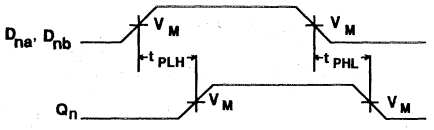
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1	3.0 2.5	4.2 4.0	5.6 5.3	3.0 2.5	6.6 6.3	ns

AC WAVEFORMS

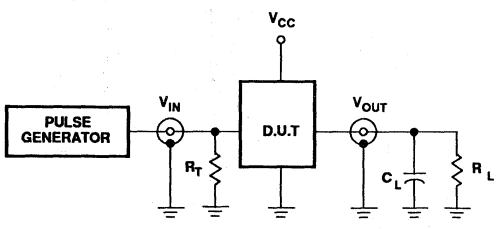


Waveform 1.

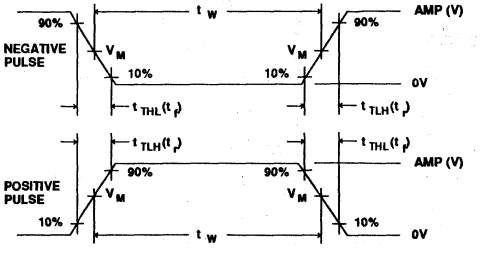
For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0329
ECN No.	97683
Date of issue	September 20, 1989
Status	Product Specification
FAST Products	

FAST 74F10, 74F11 Gates

74F10 Triple 3-Input NAND Gate
74F11 Triple 3-Input AND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F10	3.5ns	3.3mA
74F11	4.2ns	5.3mA

ORDERING INFORMATION

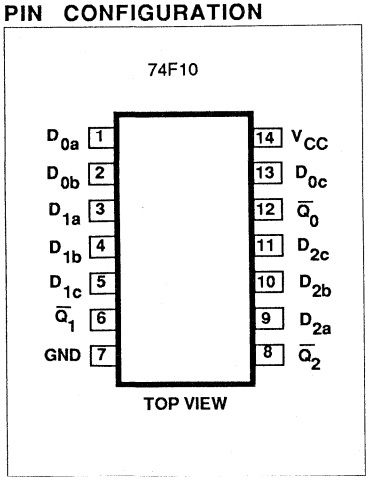
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F10N, N74F11N
14-Pin Plastic SO	N74F10D, N74F11D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

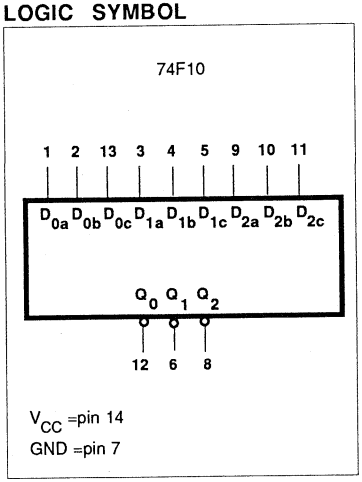
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data output ('F10)	50/33	1.0mA/20mA
Q_n	Data output ('F11)	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

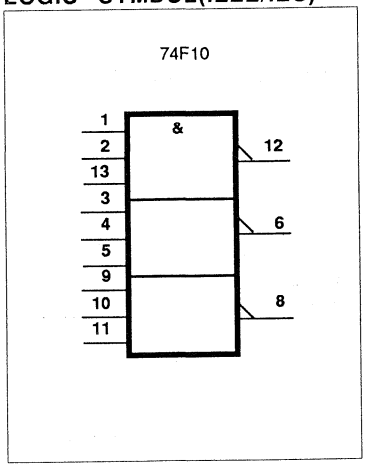
PIN CONFIGURATION



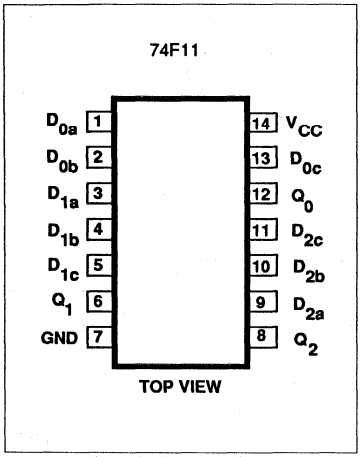
LOGIC SYMBOL



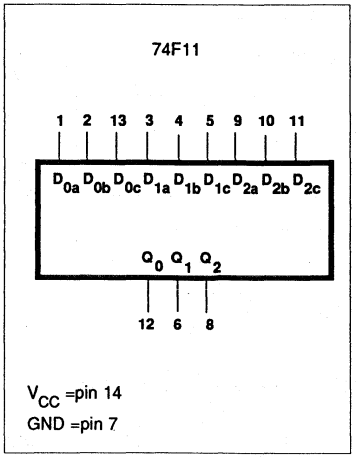
LOGIC SYMBOL(IEEE/IEC)



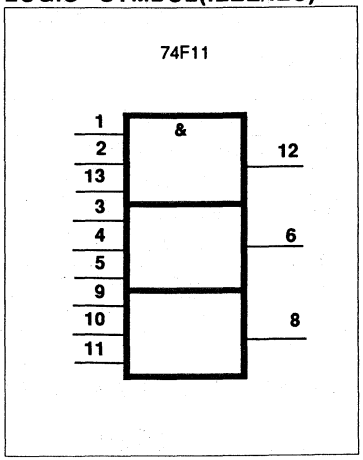
PIN CONFIGURATION



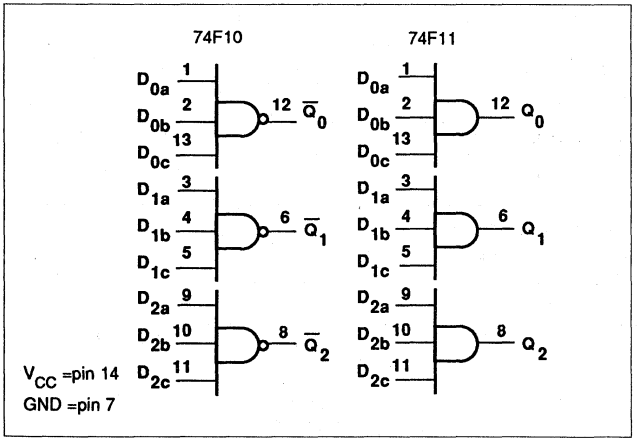
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	
			74F10	74F11
D_{na}	D_{nb}	D_{nc}	$\overline{Q}_n$	Q_n
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to + 7.0	V
V_{IN}	Input voltage	-0.5 to + 7.0	V
I_{IN}	Input current	-30 to + 5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to + 70	°C
T_{STG}	Storage temperature	-65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	'F10	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		1.8	2.1	mA
			I_{CCL}		V_{IN}=4.5V		6.0	7.7	mA
		'F11	I_{CCH}		V_{IN}=4.5V		4.7	6.2	mA
			I_{CCL}		V_{IN}=GND		7.2	9.7	mA

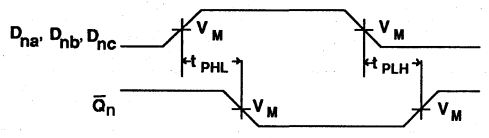
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

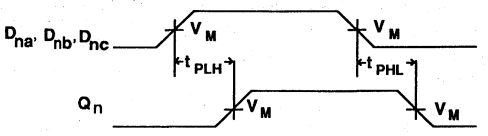
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to $\overline{Q}_n$	74F10	Waveform 1	2.4 1.5	3.7 3.2	5.0 4.3	2.4 1.5	6.0 5.3	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	74F11	Waveform 2	3.0 2.5	4.2 4.1	5.6 5.5	3.0 2.5	6.6 6.5	ns

AC WAVEFORMS



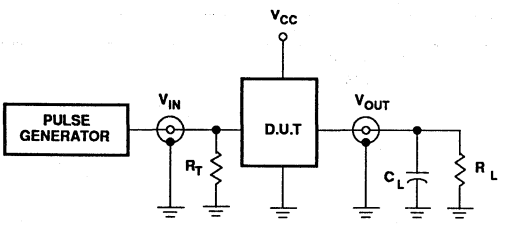
Waveform 1. For Inverting Outputs ('F10)



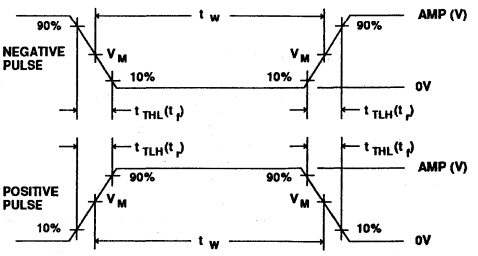
Waveform 2. For Non-Inverting Outputs ('F11)

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Hex inverter schmitt trigger — 74F14

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F14	5.0ns	18mA

DESCRIPTION

The 74F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter free output signals. In addition, they have greater noise margin than conventional inverters. Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem–pole output. The Schmitt trigger uses positive feedback to effectively speed–up slow input transitions, and provide different input threshold voltages for positive–going and negative–going input threshold (typically 800mV) is determined internally by resistor ratios and is insensitive to temperature and supply voltage variations.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F14N	I74F14N
14–pin plastic SO	N74F14D	I74F14D

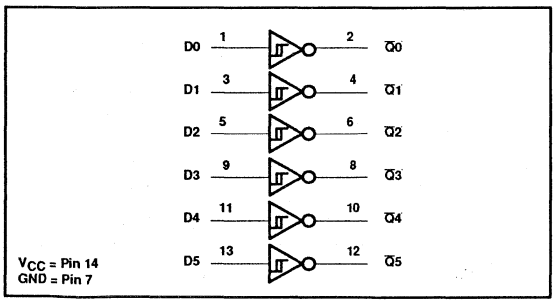
INPUT AND OUTPUT LOADNG AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$n	Data output	50/33	1.0mA/20mA

Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM



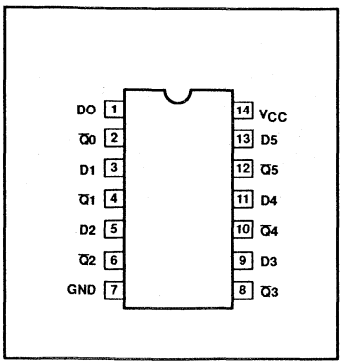
FUNCTION TABLE

INPUTS	OUTPUT
Dn	$\overline{Q}$n
L	H
H	L

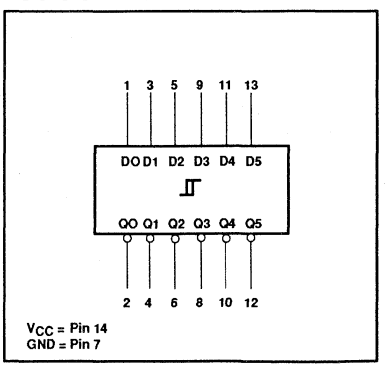
Notes to function table

1. H = High voltage level
2. L = Low voltage level

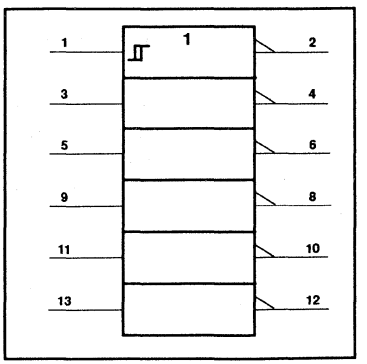
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

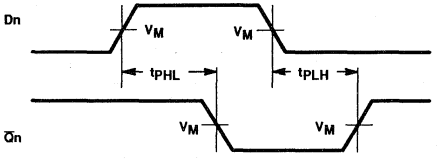
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{T+}	Positive–going threshold		V_{CC} = 5.0V		1.4	1.7	2.0	V
V_{T-}	Negative–going threshold		V_{CC} = 5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_I = V_{T-MIN},	±10%V_{CC}	2.5			V
			I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_I = V_{T+MAX},	±10%V_{CC}		0.30	0.50	V
			I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_{T+}	Input current at positive–going threshold		V_{CC} = 5.0V, V_I = V_{T+}			0		µA
I_{T-}	Input current at negative–going threshold		V_{CC} = 5.0V, V_I = V_{T-}			–175		µA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		13	22	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		23	32	mA

Notes to DC electrical characteristics
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	Waveform 1	4.0 3.5	6.5 5.0	8.5 6.5	4.0 3.5	9.5 7.0	3.0 3.5	10.5 9.0	ns

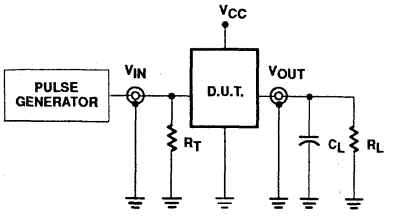
AC WAVEFORMS



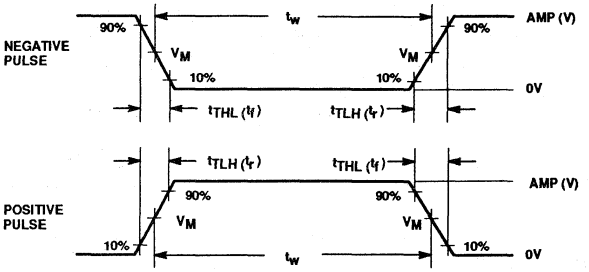
Waveform 1. Propagation delay for inverting outputs

Note to AC Waveforms
1. For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

NOTES

Philips Semiconductors-Signetics

Document No.	853-0332
ECN No.	95935
Date of issue	March 3, 1989
Status	Product Specification
FAST Products	

FAST 74F20 Gate

Dual 4-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F20	3.5 ns	2.2 mA

ORDERING INFORMATION

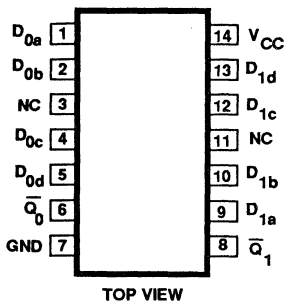
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F20N
14-Pin Plastic SO	N74F20D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

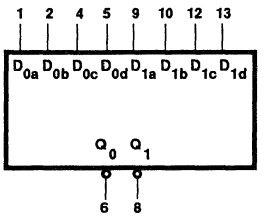
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



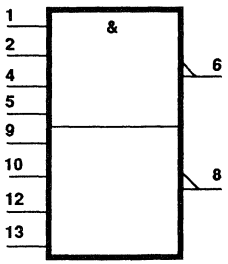
TOP VIEW

LOGIC SYMBOL

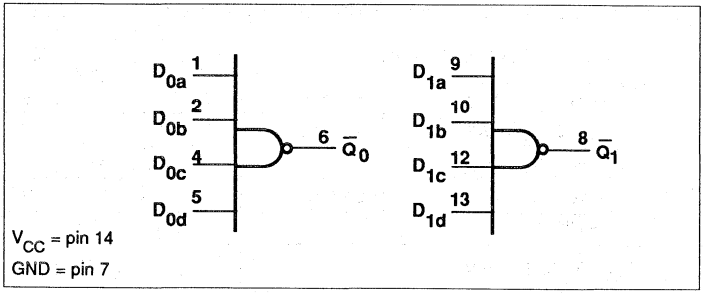


V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
D_{na}	D_{nb}	D_{nc}	D_{nd}	$\overline{Q}_n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

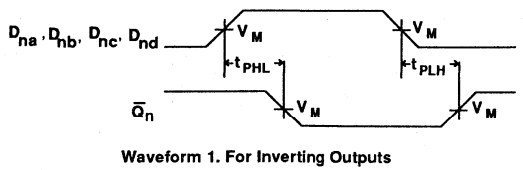
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		0.9	1.4	mA
		I_{CCL}		V_{IN}=4.5V		3.4	5.1	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to $\overline{Q}_n$	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	ns

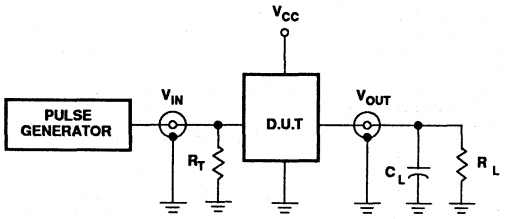
AC WAVEFORMS



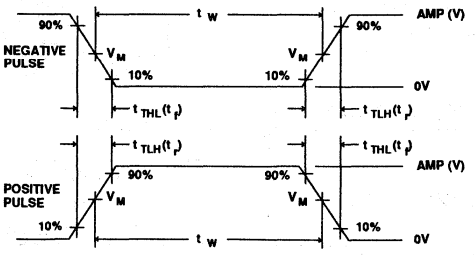
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Triple 3-input NOR gate — 74F27

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F27	3.0ns	6.5mA

ORDERING INFORMATION

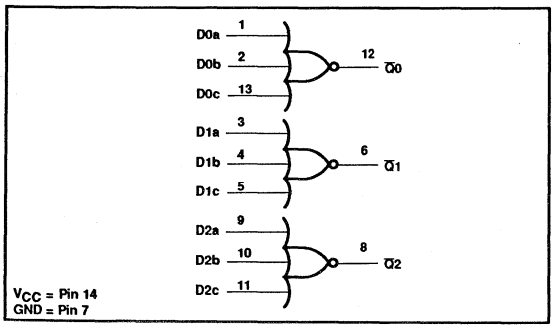
DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F27N	I74F27N
14–pin plastic SO	N74F27D	I74F27D

INPUT AND OUTPUT LOADNG AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
Dna, Dnb, Dnc	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}n$	Data output	50/33	1.0mA/20mA

Note to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

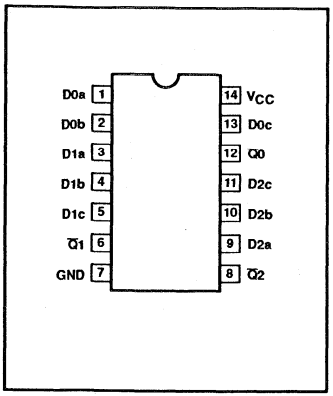


FUNCTION TABLE

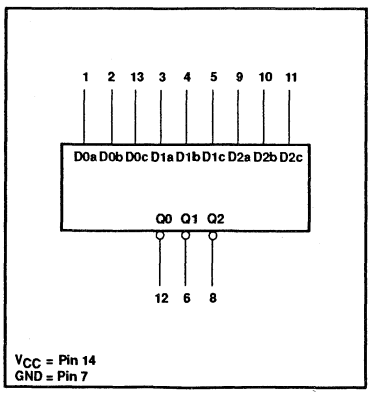
INPUTS			OUTPUT
Dna	Dnb	Dnc	$\overline{Q}n$
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

Notes to function table
1. H = High voltage level
2. L = Low voltage level

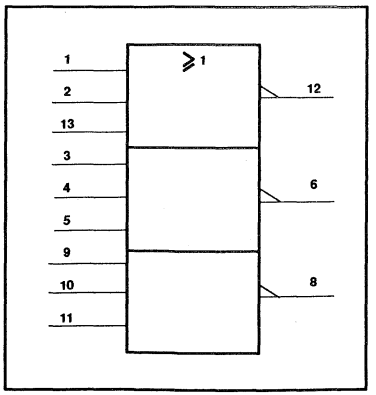
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		4.0	5.5	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		8.5	12.0	mA

Notes to DC electrical characteristics

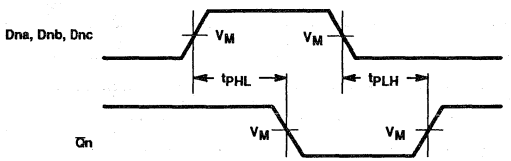
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to $\overline{Q}$n	Waveform 1	2.0 1.0	3.5 2.5	5.0 4.5	1.5 1.0	5.5 4.5	1.0 1.0	7.0 5.5	ns

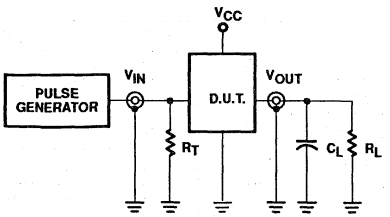
AC WAVEFORMS



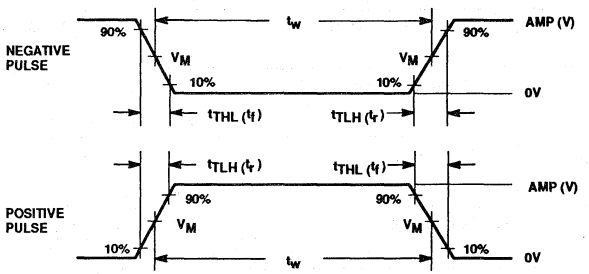
Waveform 1. Propagation delay for inverting outputs

Note to AC Waveforms
1. For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Document No.	853-0050
ECN No.	95941
Date of issue	March 3, 1989
Status	Product Specification
FAST Products	

FAST 74F30 Gate

8-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30	3.2 ns	1.7 mA

ORDERING INFORMATION

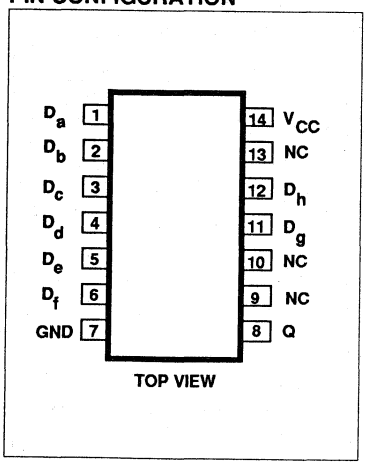
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F30N
14-Pin Plastic SO	N74F30D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

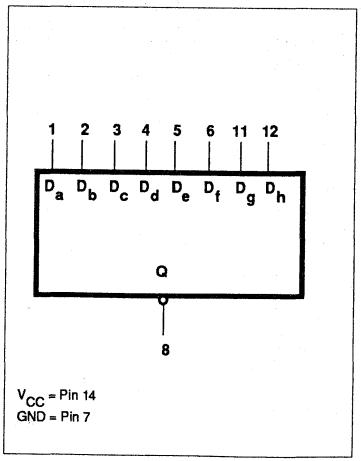
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

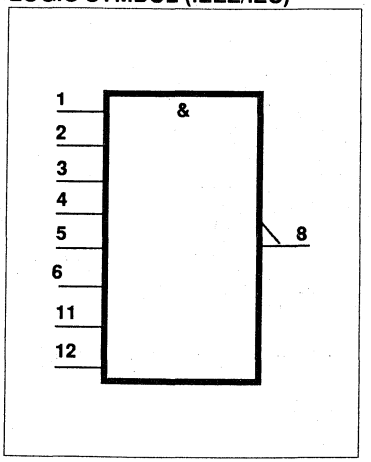
PIN CONFIGURATION



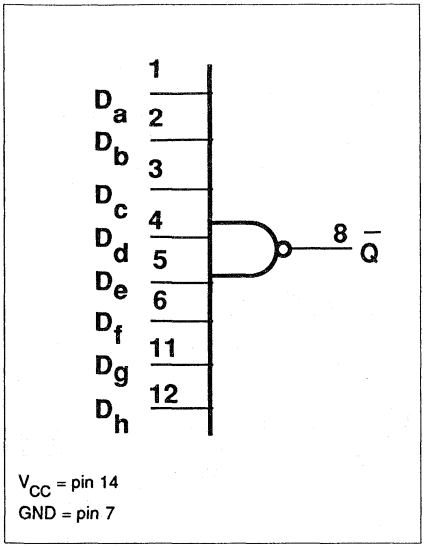
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS								OUTPUT
D_a	D_b	D_c	D_d	D_e	D_f	D_g	D_h	$\overline{Q}$
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		0.6	1.5	mA
		I_{CCL}		V_{IN}=4.5V		2.8	4.0	mA

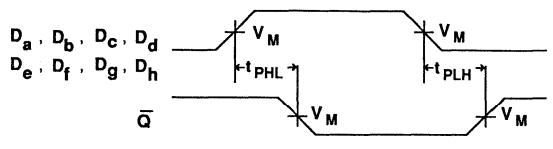
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_a, D_b, D_c, D_d, D_e, D_f, D_g, D_h to $\overline{Q}$	Waveform 1	1.5 1.0	3.5 3.0	5.0 4.5	1.5 1.0	5.5 5.0	ns

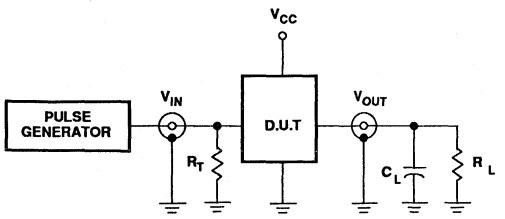
AC WAVEFORMS



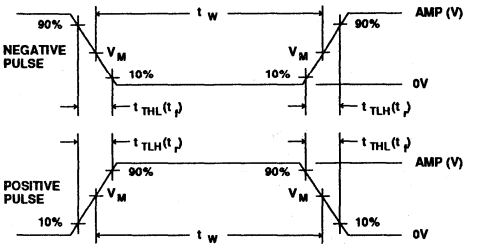
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Quad 2-input OR gate — 74F32

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F32	4.1ns	8.2mA

ORDERING INFORMATION

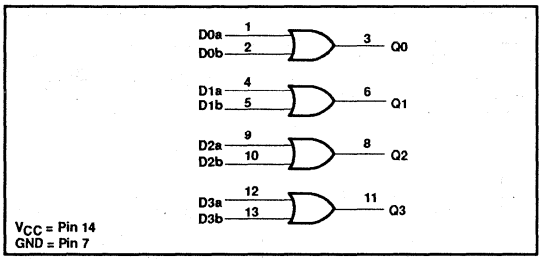
DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F32N	I74F32N
14–pin plastic SO	N74F32D	I74F32D

INPUT AND OUTPUT LOADNG AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/ LOW
Dna, Dnb	Data inputs	1.0/1.0	20µA/0.6mA
Qn	Data output	50/33	1.0mA/20mA

Note to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

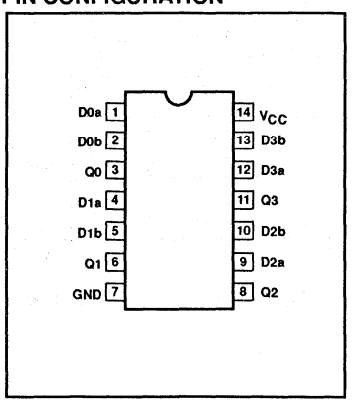


FUNCTION TABLE

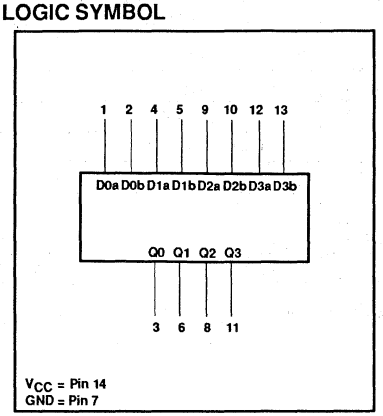
INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	L
L	H	H
H	L	H
H	H	H

Notes to function table
1. H = High voltage level
2. L = Low voltage level

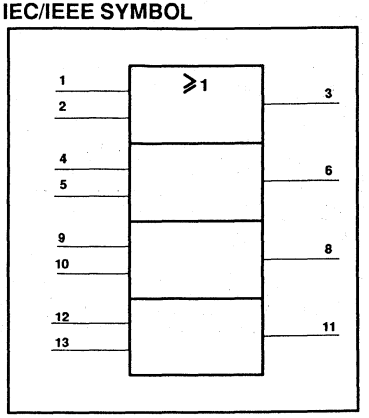
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V		6.1	9.2	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = GND		10.3	15.5	mA

Notes to DC electrical characteristics

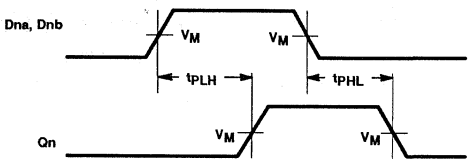
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	Waveform 1	3.0 3.0	4.2 4.0	5.6 5.3	3.0 3.0	6.6 6.3	3.0 3.0	6.6 6.3	ns

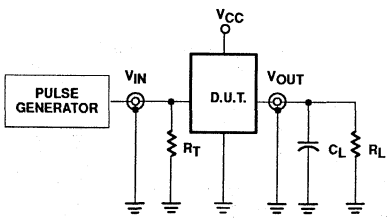
AC WAVEFORMS



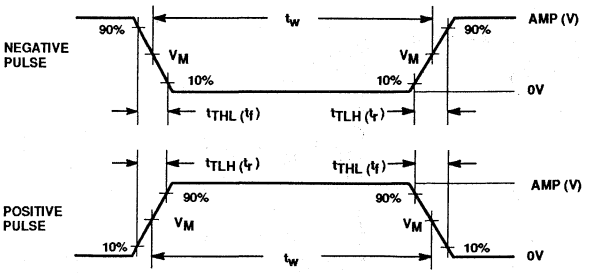
Waveform 1. Propagation delay for inverting outputs

Note to AC Waveforms
1. For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	v_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Document No.	853-0051
ECN No.	99679
Date of issue	May 24, 1990
Status	Product Specification
FAST Products	

FAST 74F37 Buffer

Quad 2-Input NAND Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F37	3.5 ns	13 mA

FUNCTION TABLE

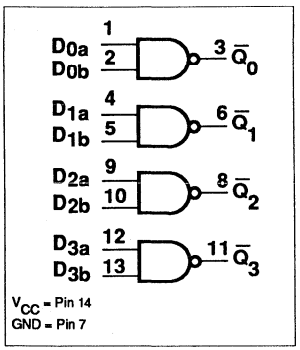
INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F37N
14-Pin Plastic SO	N74F37D

LOGIC DIAGRAM

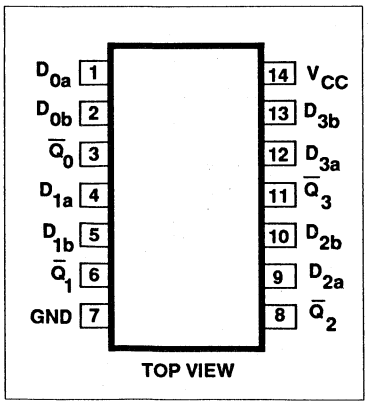


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

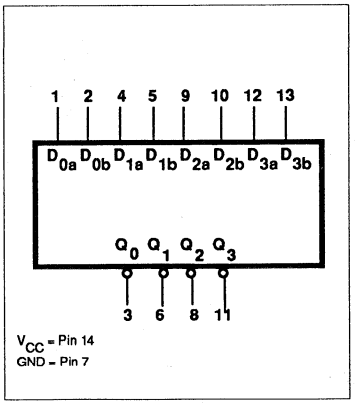
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/2.0	20µA/1.2mA
$\overline{Q}_n$	Data output	750/106.6	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

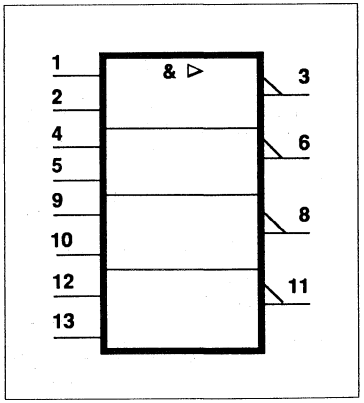
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}= -1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH}= -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-1.2	mA
I_{OS}	Short circuit output current		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN}= GND		3.0	6.0	mA
		I_{CCL}			V_{IN}= 4.5V		23	33	mA

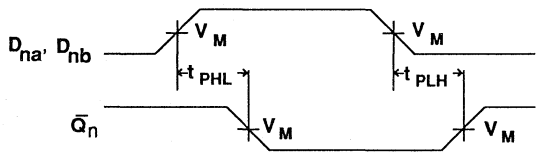
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	2.5 1.5	3.5 2.5	5.5 4.5	2.0 1.5	6.5 5.0	ns

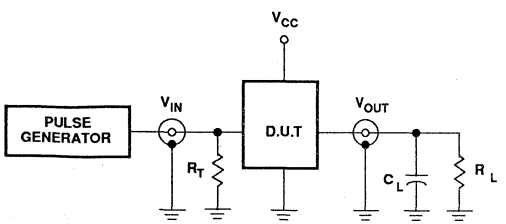
AC WAVEFORMS



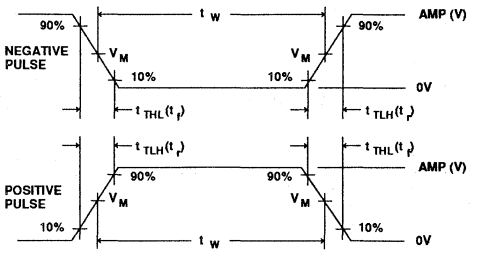
Waveform 1.For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Quad 2-input NAND buffer (open collector) 74F38

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F38	7.0ns	13mA

ORDERING INFORMATION

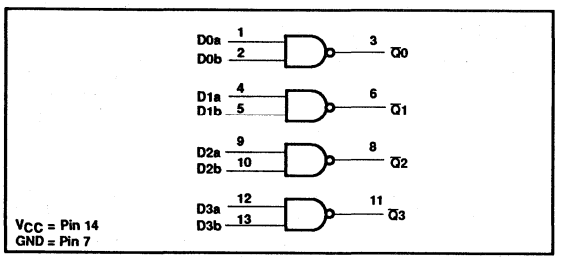
DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F38N	I74F38N
14–pin plastic SO	N74F38D	I74F38D

INPUT AND OUTPUT LOADNG AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/ LOW
Dna, Dnb	Data inputs	1.0/2.0	20µA/1.2mA
$\overline{Q}$n	Data output	OC/106.7	OC/64mA

Notes to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.
2. OC = open collector

LOGIC DIAGRAM

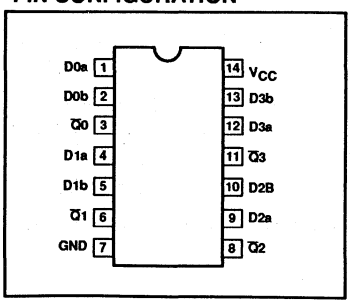


FUNCTION TABLE

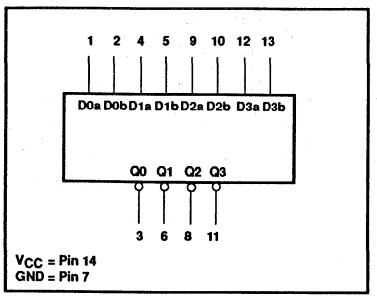
INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}$n
L	L	H
L	H	H
H	L	H
H	H	L

Notes to function table
1. H = High voltage level
2. L = Low voltage level

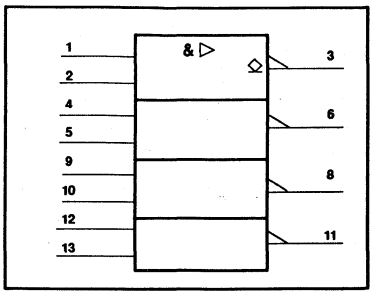
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		128	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
V_{OH}	High–level output voltage				4.5	V
I_{OL}	Low–level output current				64	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}			0.55	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-1.2	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		4.0	7.0	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		22	30	mA

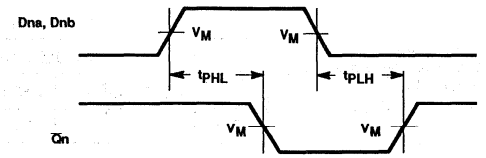
Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	7.5 1.5	10.0 3.0	12.5 5.0	7.5 1.5	13.0 5.5	7.5 1.5	14.5 6.0	ns

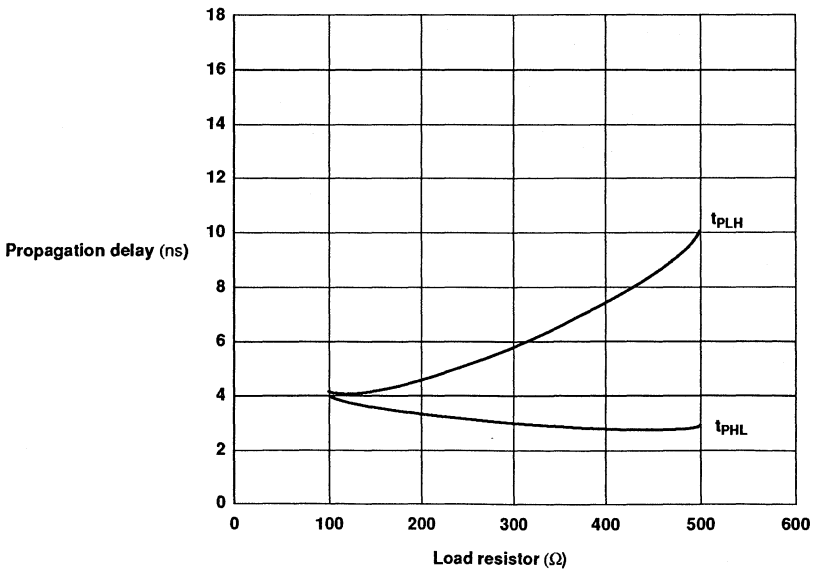
AC WAVEFORMS



Waveform 1. Propagation delay for inverting outputs

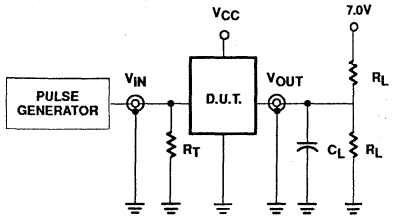
Note to AC Waveforms
1. For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

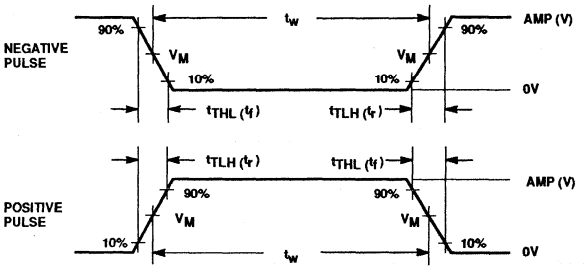


Note to typical propagation delays versus load for open collector outputs
1. When using open collector parts, the value of the pull–up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull–up resistor value from 500 ohm to 100 ohm will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull–up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} minimum specification.

TEST CIRCUIT AND WAVEFORM



Test circuit for open collector outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Document No.	853-0053
ECN No.	96314
Date of issue	April 11, 1989
Status	Product Specification
FAST Products	

FAST 74F40 Buffer

Dual 4-Input NAND Buffer

FUNCTION TABLE

INPUTS				OUTPUT
D_{na}	D_{nb}	D_{nc}	D_{nd}	$\overline{Q}_n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	X	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F40	3.5 ns	6 mA

ORDERING INFORMATION

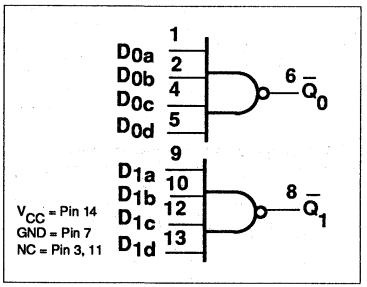
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F40N
14-Pin Plastic SO	N74F40D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

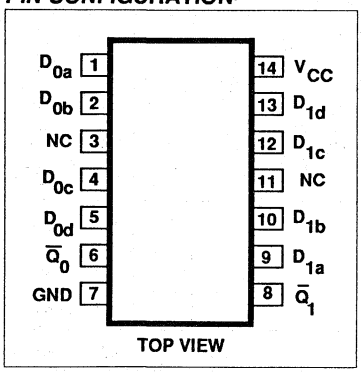
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/2.0	20µA/1.2mA
$\overline{Q}_0$, $\overline{Q}_1$	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

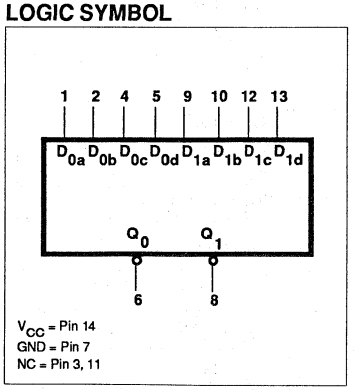
LOGIC DIAGRAM



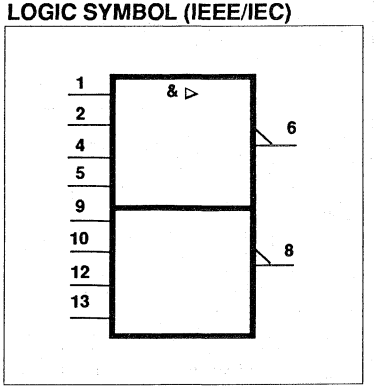
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}= -1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH}= -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-1.2	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN}= GND		1.75	4.0	mA
		I_{CCL}			V_{IN}= 4.5V		11	17	mA

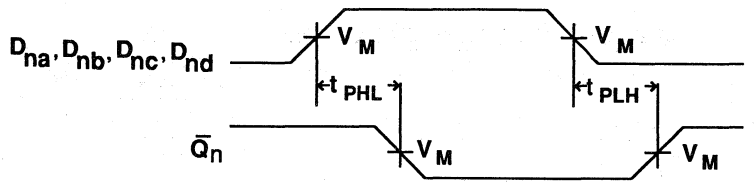
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to $\overline{Q}_n$	Waveform 1	2.0 1.5	4.0 3.0	6.0 5.0	1.5 1.0	7.0 5.5	ns

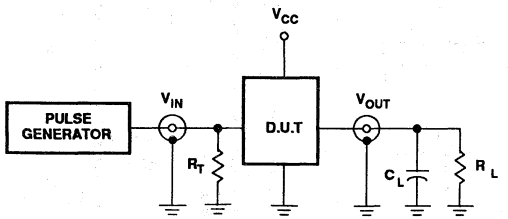
AC WAVEFORMS



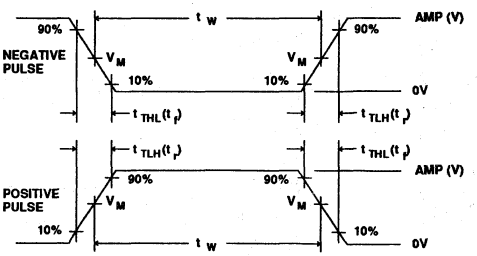
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

Document No.	853-0054
ECN No.	95962
Date of issue	March 3, 1989
Status	Product Specification
FAST Products	

FAST 74F51
Gate

Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-Invert Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F51	3.0 ns	3.5 mA

ORDERING INFORMATION

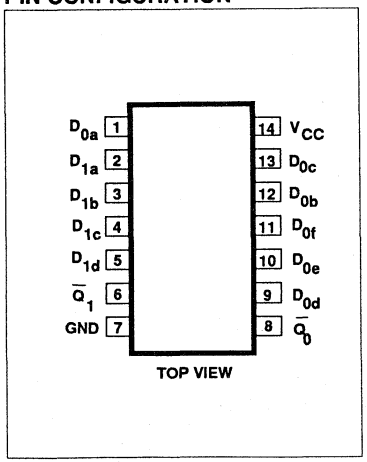
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F51N
14-Pin Plastic SO	N74F51D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

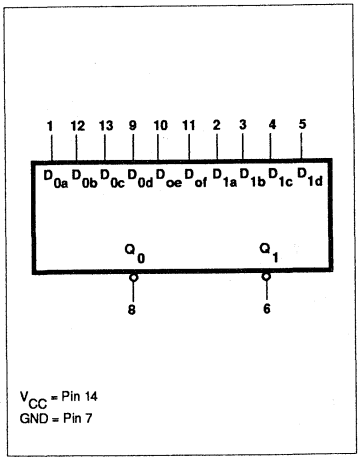
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}, D_{ne}, D_{nf}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

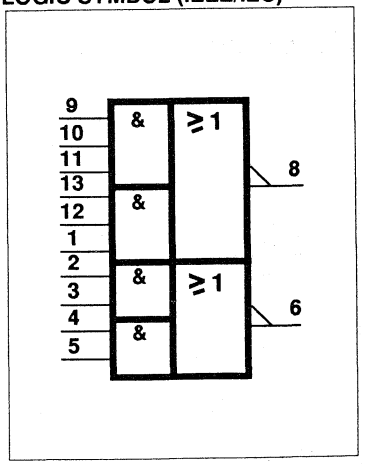
PIN CONFIGURATION



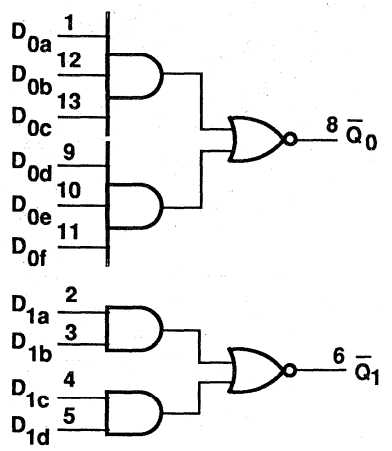
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE for 3-Input Gates

INPUTS						OUTPUT
D_{0a}	D_{0b}	D_{0c}	D_{0d}	D_{0e}	D_{0f}	$\overline{Q}_0$
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE for 2-Input Gates

INPUTS				OUTPUT
D_{1a}	D_{1b}	D_{1c}	D_{1d}	$\overline{Q}_1$
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

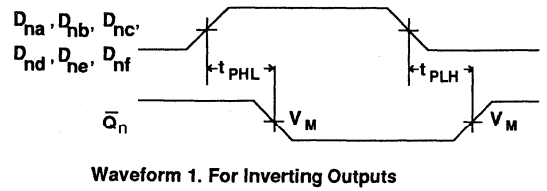
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		1.8	3.0	mA
		I_{CCL}		V_{IN}=4.5V		5.5	7.5	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd}, D_{ne}, D_{nf} to $\overline{Q}_n$	Waveform 1	2.0 1.0	3.5 2.5	5.5 4.0	1.5 1.0	6.5 4.5	ns

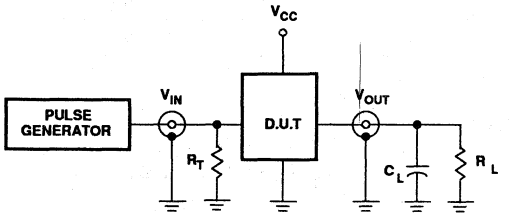
AC WAVEFORMS



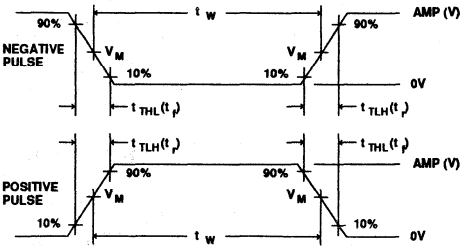
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0334
ECN No.	96147
Date of issue	March 28, 1989
Status	Product Specification
FAST Products	

FAST 74F64 Gate

Four-Two-Three-Two-Input AND-OR-Invert Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F64	4.0 ns	2.5 mA

ORDERING INFORMATION

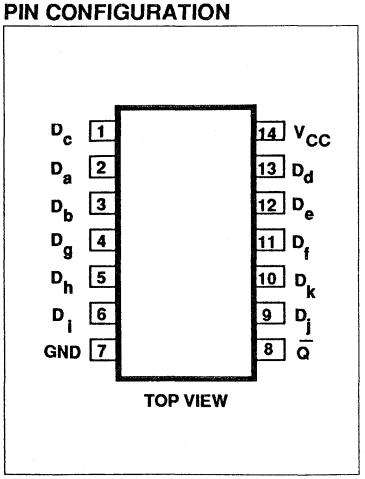
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F64N
14-Pin Plastic SO	N74F64D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

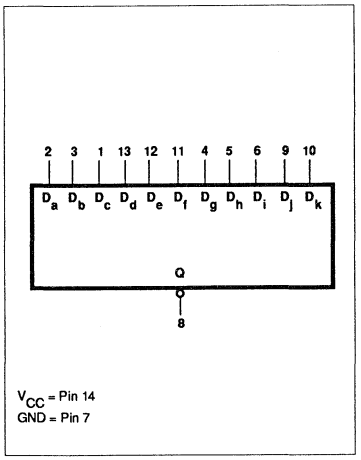
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}$	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

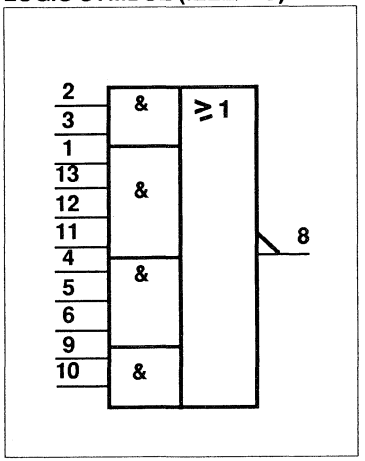
PIN CONFIGURATION



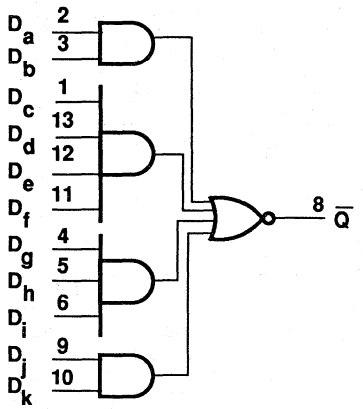
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS											OUTPUT
D_a	D_b	D_c	D_d	D_e	D_f	D_g	D_h	D_i	D_j	D_k	$\overline{Q}$
H	H	H	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

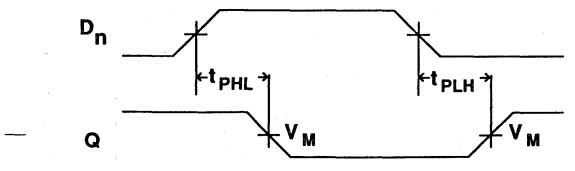
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		1.9	2.8	mA
		I_{CCL}		V_{IN}=4.5V		3.1	4.7	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}$	Waveform 1	2.5 2.0	4.6 3.2	6.0 4.5	2.5 2.0	7.0 5.5	ns

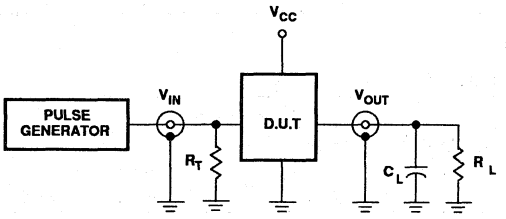
AC WAVEFORMS



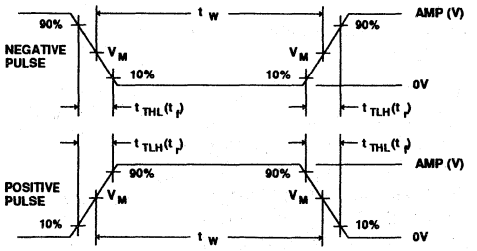
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Dual D-type flip–flop | 74F74

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F74	125MHz	11.5mA

DESCRIPTION

The 74F74 is a dual positive edge–triggered D–type flip–flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock input. When set and reset are inactive (high), data at the D input is transferred to the Q and $\overline{Q}$ outputs on the low–to–high transition of the clock. Data must be stable just one setup time prior to the low–to–high transition of the clock for predictable operation. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive–going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F74N	I74F74N
14–pin plastic SO	N74F74D	I74F74D

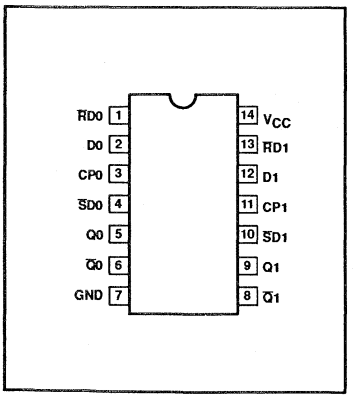
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0, D1	Data inputs	1.0/1.0	20µA/0.6mA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active low)	1.0/3.0	20µA/1.8mA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active low)	1.0/3.0	20µA/1.8mA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	50/33	1.0mA/20mA

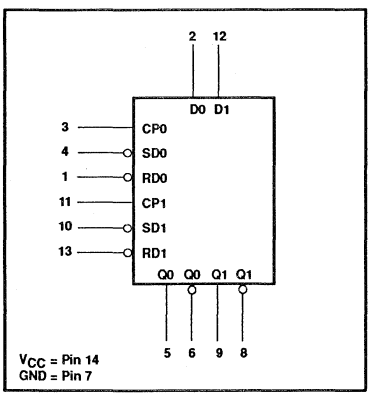
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

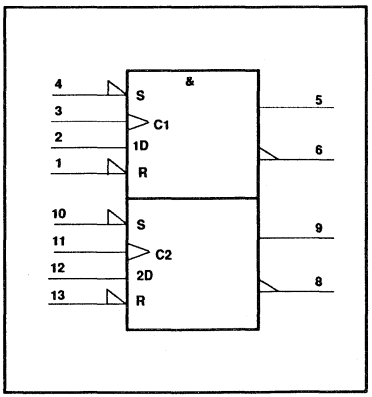
PIN CONFIGURATION



LOGIC SYMBOL

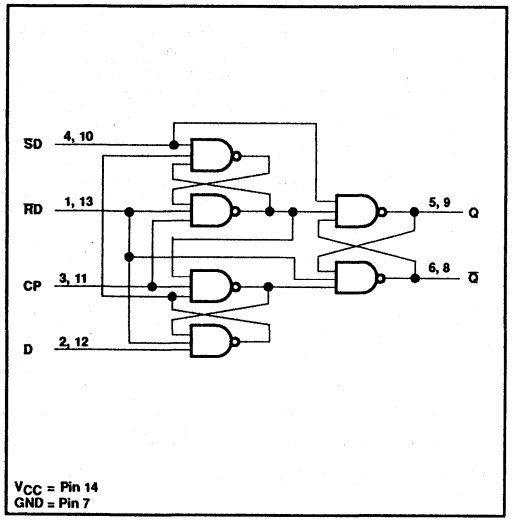


IEC/IEEE SYMBOL



Dual D-type flip–flop | 74F74

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↧	X	NC	NC	Hold

Notes to function table

1. H = High voltage level
2. h = High voltage level one setup time prior to low–to–high clock transition
3. L = Low voltage level
4. l = Low voltage level one setup time prior to low–to–high clock transition
5. NC = No change from the previous setup
6. X = Don't care
7. ↑ = Low–to–high clock transition
8. ↧ = Not low–to–high clock transition
9. * = This setup is unstable and will change when either set or reset return to the high level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Dn, CPn	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{S}$Dn, $\overline{R}$Dn	V_{CC} = MAX, V_I = 0.5V					-1.8	mA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				11.5	16	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

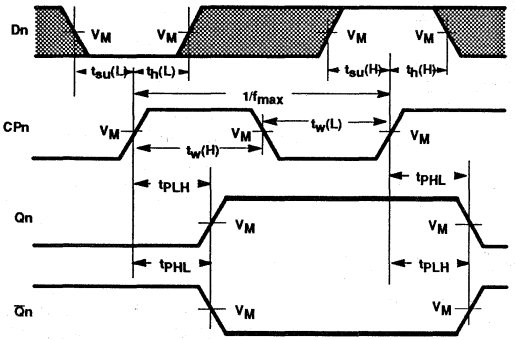
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		LIMITS T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	125		100		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	3.8 4.4	5.3 6.2	6.8 8.0	3.8 4.4	7.8 9.2	3.8 4.4	8.5 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, $\overline{R}$Dn to Qn or $\overline{Q}$n	Waveform 2	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	7.1 10.5	3.2 2.5	7.5 10.5	ns

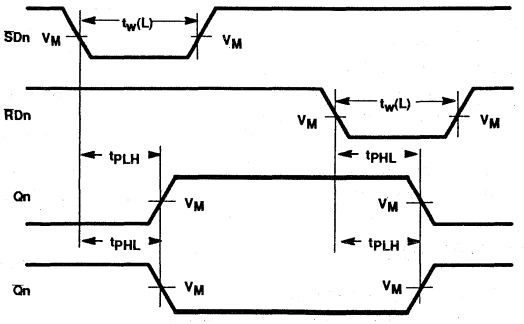
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		LIMITS T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to CPn	Waveform 1	2.0 3.0			2.0 3.0		2.0 3.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.0 1.0		1.0 1.0		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 1	4.0 5.0			4.0 5.0		4.0 5.0		ns
t_w (L)	$\overline{S}$Dn, $\overline{R}$Dn pulse width, low	Waveform 2	4.0			4.0		4.0		ns
t_{rec}	Recovery time $\overline{S}$Dn, $\overline{R}$Dn to CPn	Waveform 3	2.0			2.0		2.0		ns

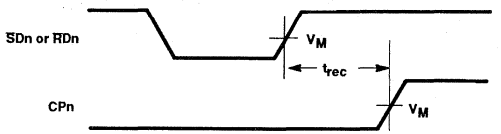
AC WAVEFORMS



Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width

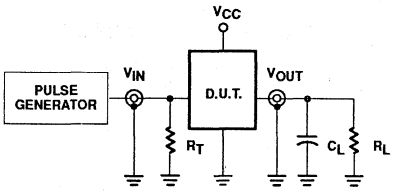


Waveform 3. Recovery time for set or reset to clock

Note to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



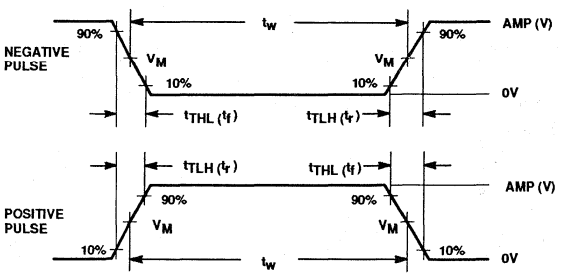
Test circuit for totem-pole outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0055
ECN No.	99494
Date of issue	April 27, 1990
Status	Product Specification
FAST Products	

FAST 74F85 Comparator

4-Bit Magnitude Comparator

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F85	7.0ns	40mA

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Magnitude comparison of any binary words**
- **Serial of parallel expansion without extra gating**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F85N
16-Pin Plastic SOL	N74F85D

DESCRIPTION

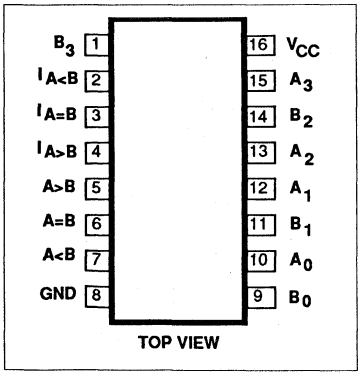
The 74F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0-A_3) and (B_0-B_3) where A_3 and B_3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exists in the parallel expansion scheme. The expansion inputs $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$=Low, $I_{A=B}$=High and $I_{A<B}$=Low.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

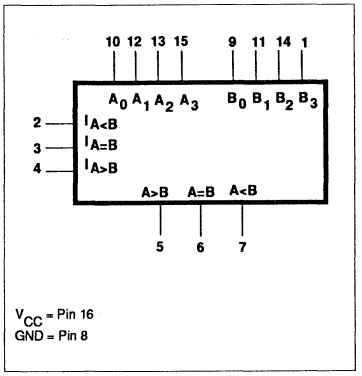
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_3	Comparing inputs	1.0/0.033	20μA/20μA
B_0- B_3	Comparing inputs	1.0/0.033	20μA/20μA
$I_{A<B}$, $I_{A=B}$, $I_{A>B}$	Expansion inputs (active High)	1.0/0.033	20μA/20μA
A<B, A=B, A>B	Data outputs (active High)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

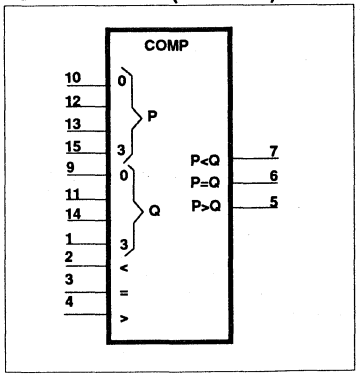
PIN CONFIGURATION



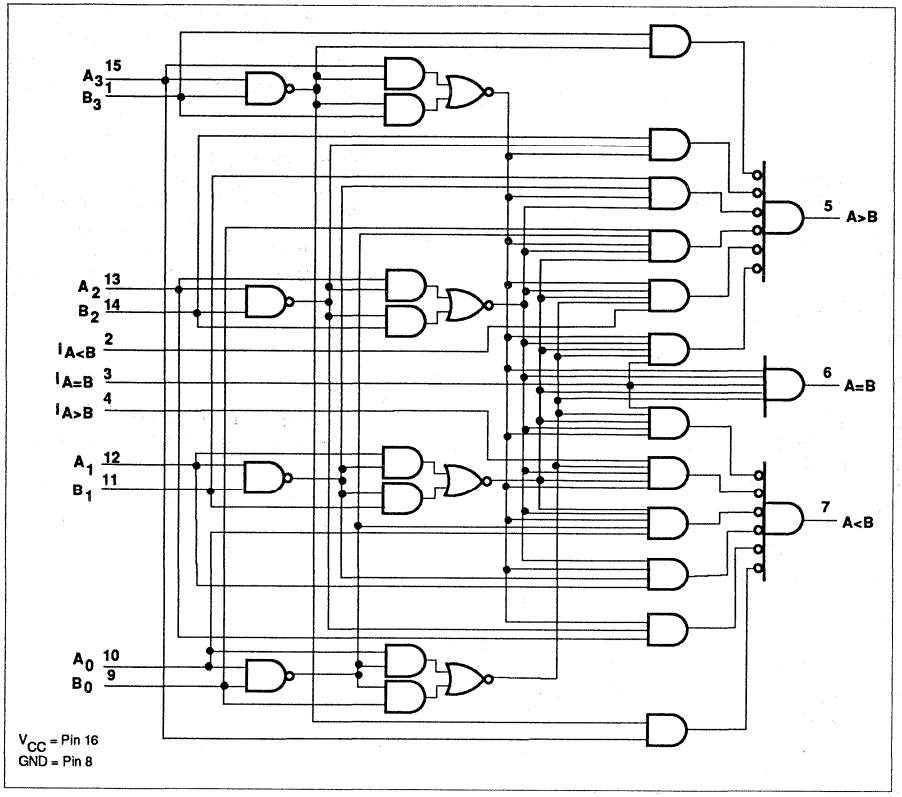
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION

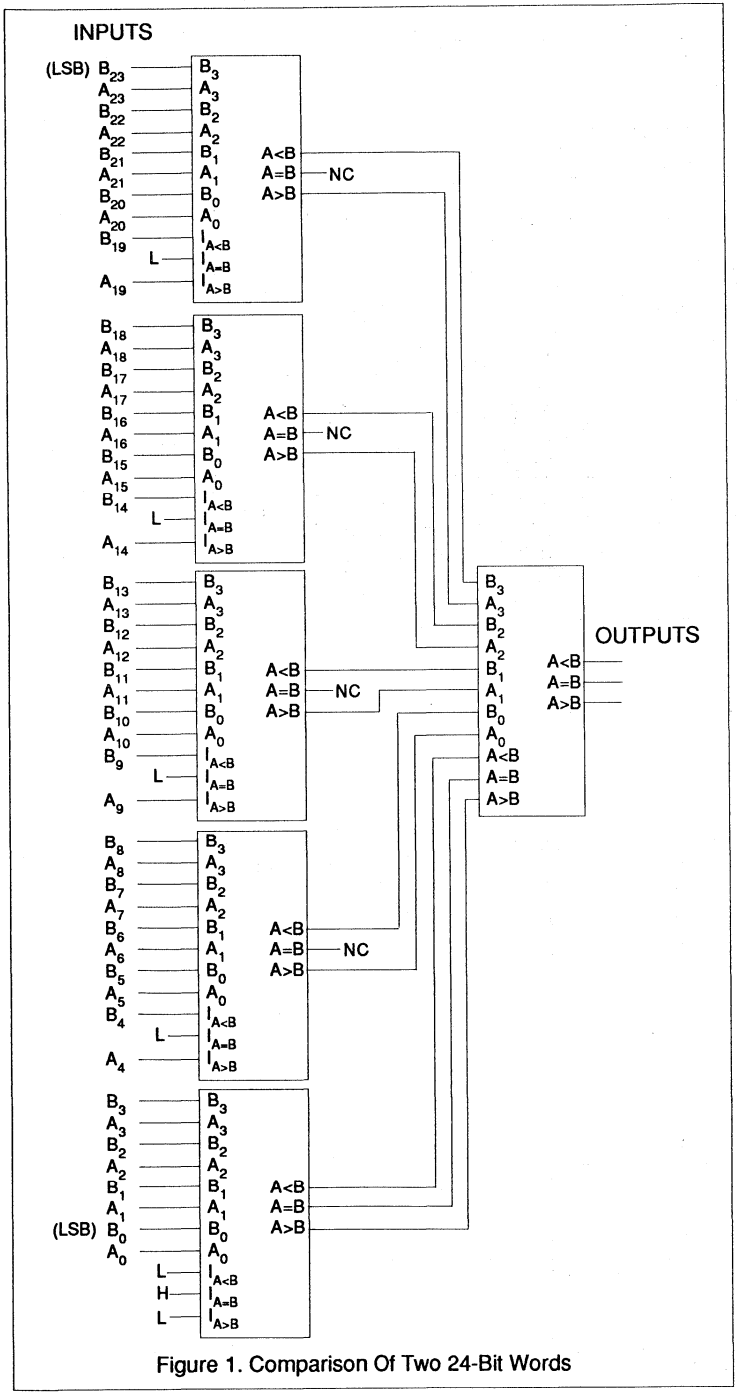


Figure 1. Comparison Of Two 24-Bit Words

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. The expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme.The expansion inputs used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as an "B" input and setting $I_{A=B}$=Low. The 'F85 can be used as 5-bit comparator only when the outputs are used to drive the (A_0-A_3) and (B_0-B_3) inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table1

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS 74F
1-4 Bits	1	12ns
5-24 Bits	2-6	22ns
25-120 Bits	8-31	34ns

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		36	50	mA
		I_{CCL}		A_n=B_n=$I_{A=B}$=GND, $I_{A>B}$=$I_{A<B}$=4.5V		40	54	mA

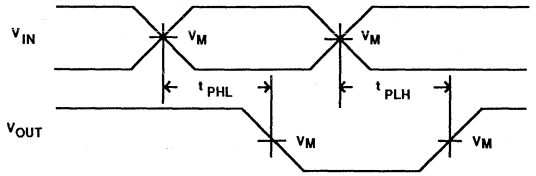
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PLH}	Propagation delay A or B to A<B, A>B	Waveform 1 3 logic levels	6.0 7.0	8.5 9.5	11.0 14.0	5.5 6.5	13.0 15.5	ns
t_{PLH} t_{PLH}	Propagation delay A or B to A=B	Waveform 1 4 logic levels	6.5 7.0	9.0 9.5	11.5 14.0	6.0 6.5	14.0 14.5	ns
t_{PLH} t_{PLH}	Propagation delay $I_{A<B}$ and $I_{A=B}$ to A>B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	7.5 9.0	2.5 2.5	9.0 10.0	ns
t_{PLH} t_{PLH}	Propagation delay $I_{A=B}$ to A=B	Waveform 1 2 logic levels	2.5 3.5	4.5 7.5	7.0 10.0	2.0 2.5	9.0 12.0	ns
t_{PLH} t_{PLH}	Propagation delay $I_{A>B}$ and $I_{A=B}$ to A<B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	8.0 9.0	3.0 2.0	9.5 9.5	ns

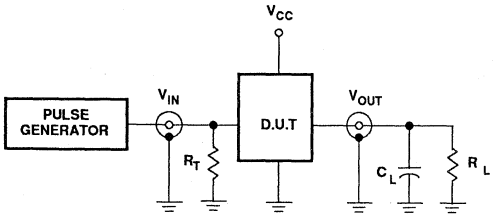
AC WAVEFORMS



Waveform 1. Propagation Delay Input To Output

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



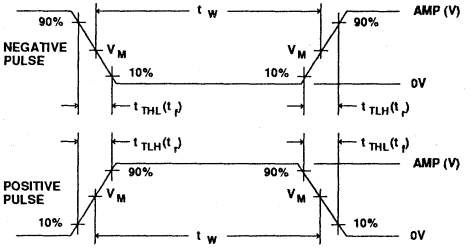
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0336
ECN No.	98773
Date of issue	February 9, 1990
Status	Product Specification
FAST Products	

FAST 74F86 Gate

Quad 2-Input Exclusive-OR Gate

FEATURE

- **Industrial temperature range available (-40°C to +85°C)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F86	4.3 ns	16.5 mA

FUNCTION TABLE

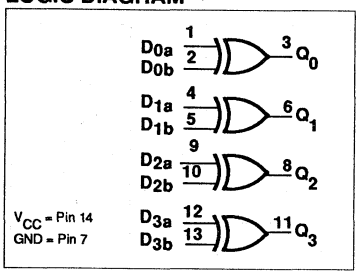
INPUTS		OUTPUT
D_{na}	D_{nb}	Q_n
L	L	L
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
14-Pin Plastic DIP	N74F86N	I74F86N
14-Pin Plastic SO	N74F86D	I74F86D

LOGIC DIAGRAM

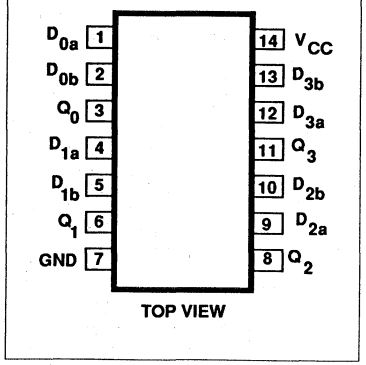


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

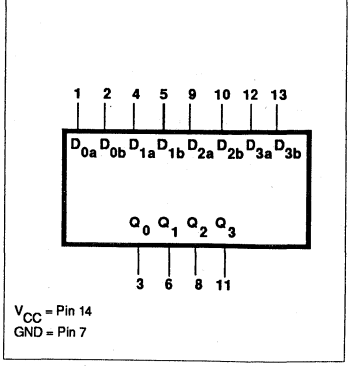
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20μA/0.6mA
Q_n	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

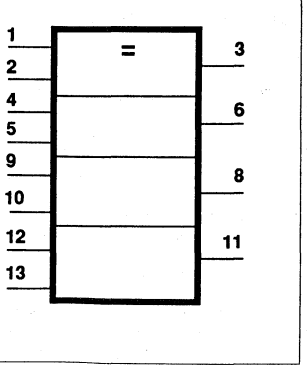
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_A	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	-40		85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuitoutput current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	D_{0a}=GND, D_{0b}=4.5V		15	23	mA
		I_{CCL}		V_{IN}=4.5V		18	28	mA

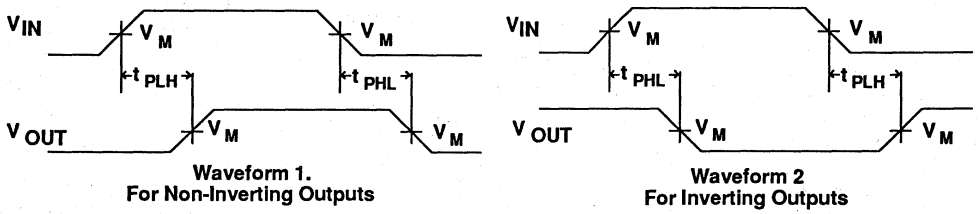
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable typ5
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na} or D_{nb} to Q_n (Other input Low)	Waveform 1	3.0 3.0	4.0 4.2	5.5 5.5	3.0 3.0	6.5 6.5	3.0 2.5	7.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay D_{na} or D_{nb} to Q_n (Other input High)	Waveform 2	3.5 3.0	5.3 4.7	7.0 6.5	3.5 3.0	8.0 7.5	3.5 3.0	10.0 8.0	ns

AC WAVEFORMS

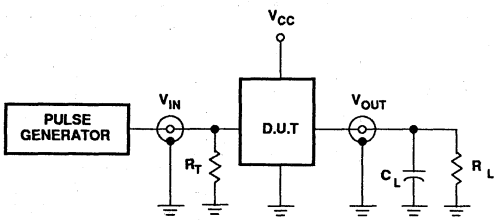


Waveform 1.
For Non-Inverting Outputs

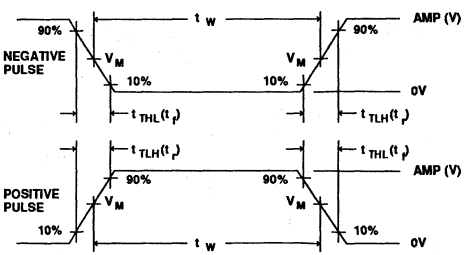
Waveform 2
For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Positive J–$\overline{K}$ positive edge-triggered flip-flops | 74F109

FEATURE

- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F109 is a dual positive edge–triggered JK–type flip–flop featuring individual J, $\overline{K}$, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock (CP) input. The J and $\overline{K}$ are edge–triggered inputs which control the state changes of the flip–flops as described in the function table. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive–going pulse. The J and $\overline{K}$ inputs must be stable just one setup time prior to the low–to–high transition of the clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip–flop by tying J and $\overline{K}$ inputs together. Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F109	125MHz	12.3mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
16–pin plastic DIP	N74F109N	I74F109N
16–pin plastic SO	N74F109D	I74F109D

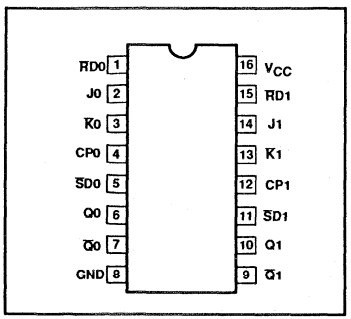
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/1.0	20µA/0.6mA
$\overline{K}$0, $\overline{K}$1	K inputs	1.0/1.0	20µA/0.6mA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active low)	1.0/3.0	20µA/1.8mA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active low)	1.0/3.0	20µA/1.8mA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	50/33	1.0mA/20mA

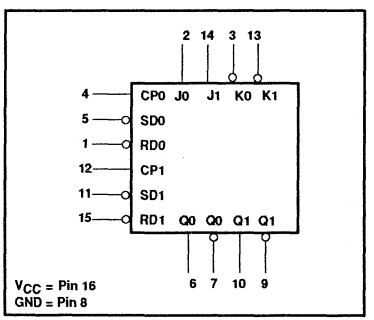
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

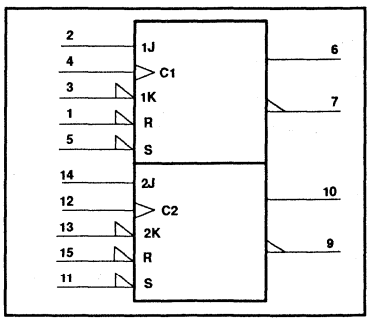
PIN CONFIGURATION



LOGIC SYMBOL

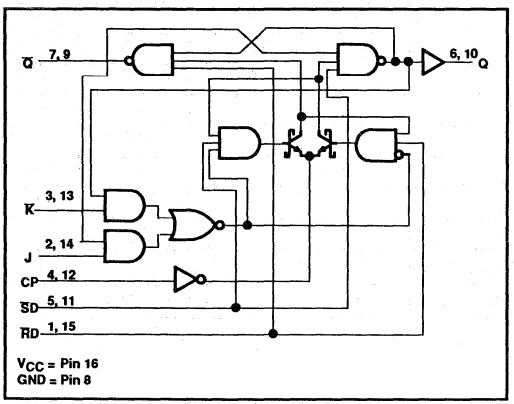


IEC/IEEE SYMBOL



Positive J–$\overline{K}$ positive edge-triggered flip-flops | 74F109

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING
$\overline{SD}$	$\overline{RD}$	CP	J	$\overline{K}$	Q	$\overline{Q}$	MODE
L	H	X	X	X	H	L	Asynchronous set
H	L	X	X	X	L	H	Asynchronous reset
L	L	X	X	X	H	H	Undetermined*
H	H	↕	X	X	q	$\overline{q}$	Hold
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	h	h	H	L	Load "1" (set)
H	H	↑	l	l	L	H	Load "0" (reset)
H	H	↑	l	h	q	$\overline{q}$	Hold 'no change"

Notes to function table

1. H = High–voltage level
2. h = High–voltage level one setup time prior to low–to–high clock transition
3. L = Low–voltage level
4. l = Low–voltage level one setup time prior to low–to–high clock transition
5. q = Lower case indicate the state of the referenced ouput prior to the low–to–high clock transition
6. X = Don't care
7. ↑ = Low–to–high clock transition
8. ↕ = Not low–to–high clock transition
9. * = Both outputs will be high if both $\overline{SD}$ and $\overline{RD}$ go low simultaneously

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

Positive J–$\overline{K}$ positive edge-triggered flip-flops | 74F109

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	J, $\overline{K}$, CPn	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{SD}$n, $\overline{RD}$n	V_{CC} = MAX, V_I = 0.5V					-1.8	mA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				12.3	17	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

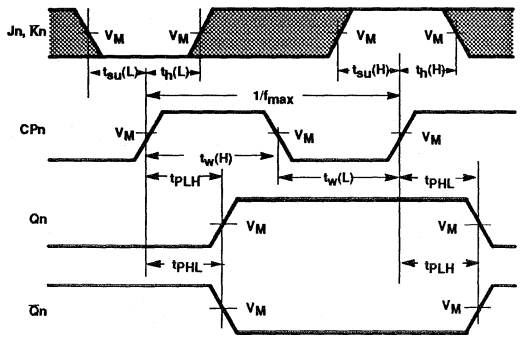
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	90	125		90		90		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	8.0 9.2	3.8 4.4	9.0 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}$n, $\overline{RD}$n to Qn or $\overline{Q}$n	Waveform 2	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	8.0 10.5	2.8 3.5	9.0 10.5	ns

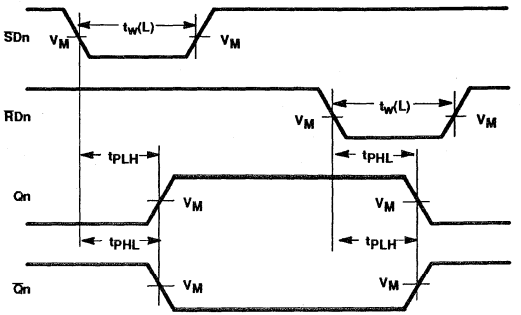
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to CPn	Waveform 1	3.0 3.0			3.0 3.0		3.0 3.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.0 1.0		1.0 1.0		ns
t_w (H) t_w (L)	CP pulse width, high or low	Waveform 1	4.0 5.0			4.0 5.0		4.0 5.0		ns
t_w (L)	$\overline{SD}$n or $\overline{RD}$n pulse width, low	Waveform 2	4.0			4.0		4.0		ns
t_{rec}	Recovery time $\overline{SD}$n or $\overline{RD}$n to CP	Waveform 3	2.0			2.0		2.0		ns

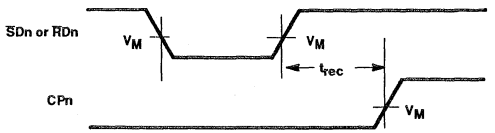
AC WAVEFORMS



Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width

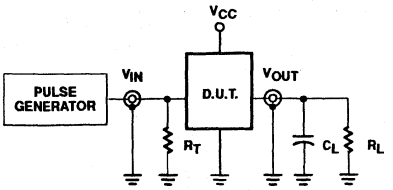


Waveform 3. Recovery time for set or reset to clock

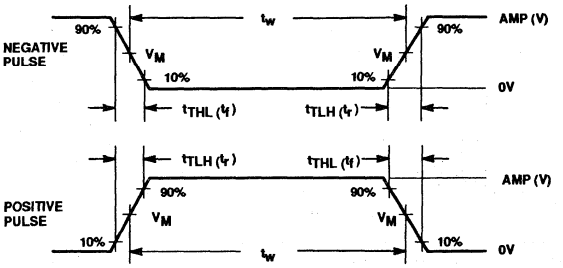
Note to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

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Date of issue	February 9, 1990
Status	Product Specification
FAST Products	

FAST 74F112
Flip-Flop

Dual J-K Negative Edge-triggered Flip-Flop

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F112	100MHz	15mA

FEATURE

- **Industrial temperature range available (-40°C to +85°C)**

DESCRIPTION

The 74F112, Dual Negative Edge-Triggered JK-Type Flip-Flop, features individual J, K, Clock ($\overline{CP}_n$), Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, true (Q_n) and complementary ($\overline{Q}_n$) outputs.

The $\overline{S}_D$ and $\overline{R}_D$ inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the level at the other inputs.

A High level on the clock ($\overline{CP}_n$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}_n$ is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the $\overline{CP}_n$.

ORDERING INFORMATION

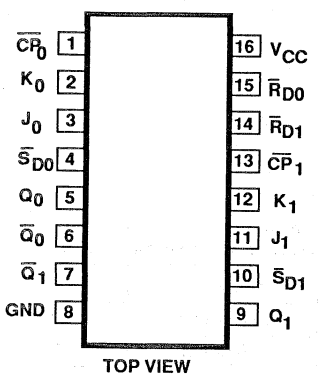
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
16-Pin Plastic DIP	N74F112N	I74F112N
16-Pin Plastic SO	N74F112D	I74F112D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20µA/0.6mA
K_0, K_1	K inputs	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{CP}_0$, $\overline{CP}_1$	Clock Pulse input (active falling edge)	1.0/4.0	20µA/2.4mA
Q_0,$\overline{Q}_0$; Q_1,$\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

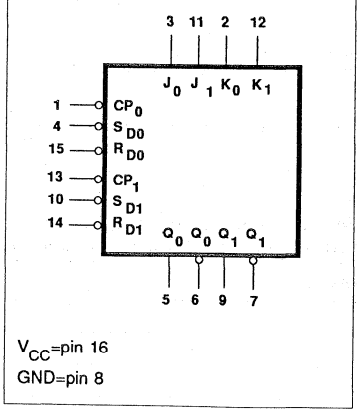
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



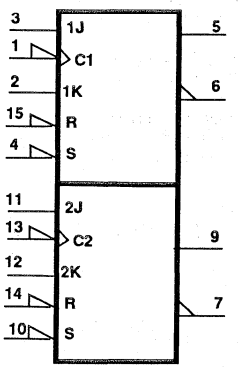
TOP VIEW

LOGIC SYMBOL

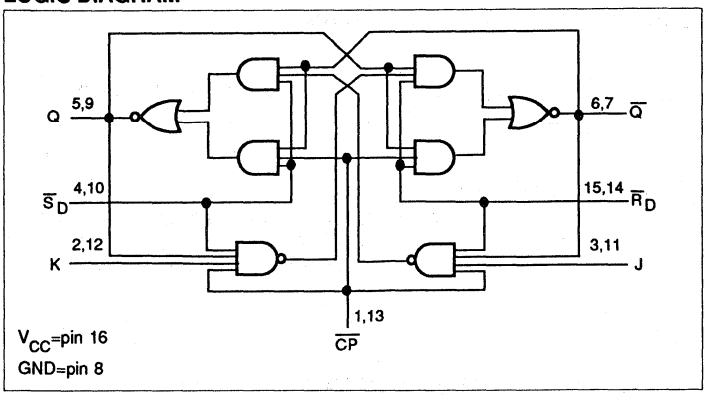


V_{CC}=pin 16
GND=pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronmous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined *
H	H	↓	h	h	$\overline{q}$	q	Toggle
H	H	↓	l	h	L	H	Load "0"(Reset)
H	H	↓	h	l	H	L	Load "1" (Set)
H	H	↓	l	l	q	$\overline{q}$	Hold "no change"
H	H	H	X	X	Q	$\overline{Q}$	Hold "no change"

H = High voltage level
h = High voltage level one setup time prior to High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to High-to-Low clock transition
q=Lower case letters indicate the state of the referenced output prior to the High-to-Low clock transition
X = Don't care
↓= High-to-Low clock transition
* =Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_A	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	-40		85	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	J_n, K_n	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CP}_n$					-2.4	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					-3.0	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.

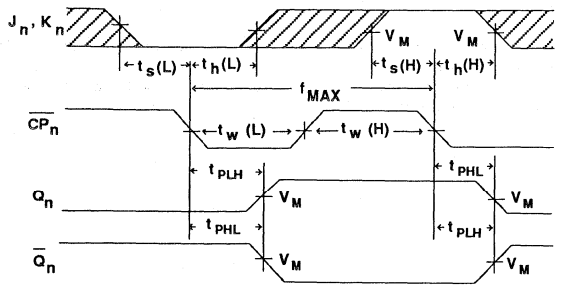
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		80		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	5.0 5.0	6.5 6.5	2.0 2.0	7.5 7.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_D$ to Q_n or $\overline{Q}_n$	Waveform 2,3	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	1.5 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low J_n, K_n to $\overline{CP}$	Waveform 1	4.0 3.5			5.0 4.0		5.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low J_n, K_n to $\overline{CP}$	Waveform 1	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_w(H) t_w(L)	$\overline{CP}$ Pulse width High or Low	Waveform 1	4.5 4.5			5.0 5.0		5.0 5.0		ns
t_w(L)	$\overline{S}_{Dn}$, $\overline{R}_D$ Pulse width Low	Waveform 2,3	4.5			5.0		5.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$, $\overline{R}_D$ to $\overline{CP}$	Waveform 2,3	4.5			5.0		5.0		ns

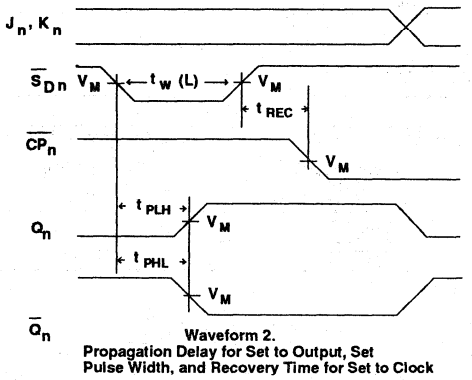
AC WAVEFORMS



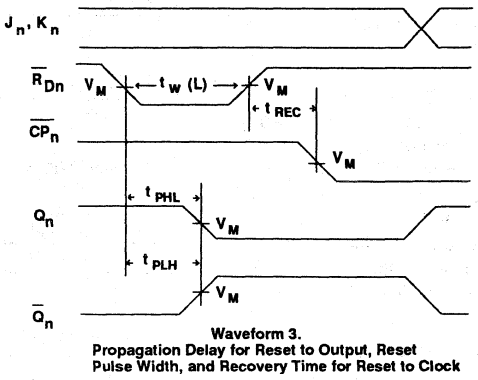
Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock pulse width

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS



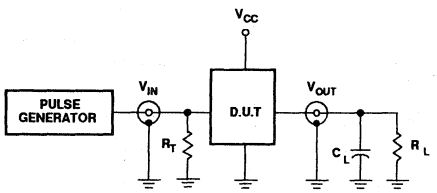
Waveform 2.
Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to Clock



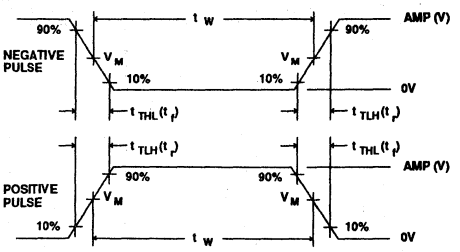
Waveform 3.
Propagation Delay for Reset to Output, Reset Pulse Width, and Recovery Time for Reset to Clock

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Dual J–K negative edge-triggered flip-flops without reset

74F113

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F113	100MHz	15mA

DESCRIPTION

The 74F113, dual negative edge–triggered JK–type flip–flop, features individual J, K, clock ($\overline{CP}$), set ($\overline{SD}$) inputs, true and complementary outputs. The asynchronous $\overline{SD}$ input, when low, forces the outputs to the steady state levels as shown in the function table regardless of the level at the other inputs.

A high level on the clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is high and flip–flop will perform according to the function table as long as minimum setup and hold times are observed. Output changes are initiated by the high–to–low transition of the $\overline{CP}$.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F113N	I74F113N
14–pin plastic SO	N74F113D	I74F109D

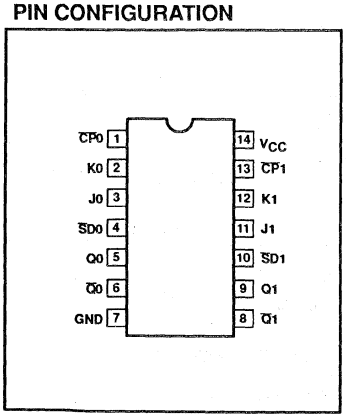
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/1.0	20µA/0.6mA
K0, K1	K inputs	1.0/1.0	20µA/0.6mA
$\overline{CP}$0, $\overline{CP}$1	Clock inputs (active falling edge)	1.0/4.0	20µA/2.4mA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active low)	1.0/5.0	20µA/3.0mA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	50/33	1.0mA/20mA

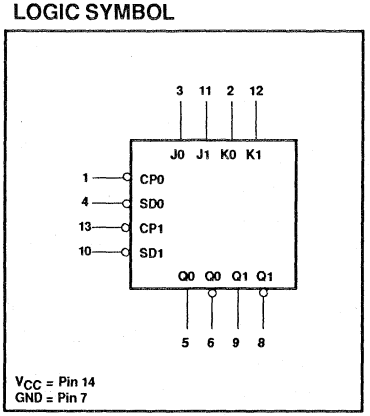
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

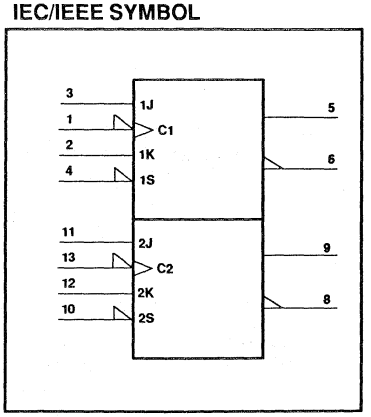
PIN CONFIGURATION



LOGIC SYMBOL



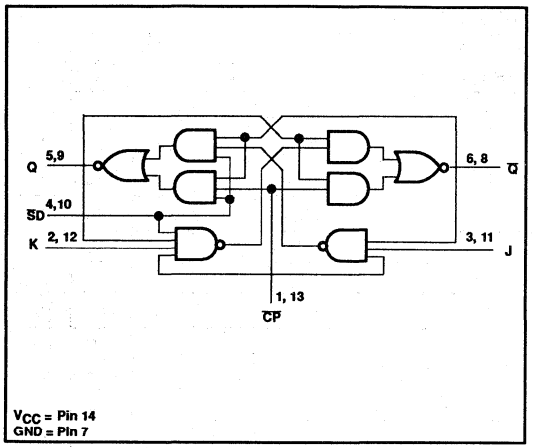
IEC/IEEE SYMBOL



Dual J–K negative edge-triggered flip-flops without reset

74F113

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	X	X	X	H	L	Asynchronous set
H	↓	h	h	$\overline{q}$	q	Toggle
H	↓	h	l	H	L	Load "1" (set)
H	↓	l	h	L	H	Load "0" (reset)
H	↓	l	l	q	$\overline{q}$	Hold 'no change"

Notes to function table

1. H = High–voltage level
2. h = High–voltage level one setup time prior to high–to–low clock transition
3. L = Low–voltage level
4. l = Low–voltage level one setup time prior to high–to–low clock transition
5. q = Lower case indicate the state of the referenced output prior to the high–to–low clock transition
6. X = Don't care
7. ↓ = high–to–low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

Dual J–K negative edge-triggered flip-flops without reset

74F113

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Jn, Kn	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{CP}$n						-2.4	mA
		$\overline{S}$Dn						-3.0	mA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				15	21	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		LIMITS T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	85	100		80		80		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	2.0 2.0	7.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, to Qn or $\overline{Q}$n	Waveform 2	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	2.0 2.0	8.0 7.5	ns

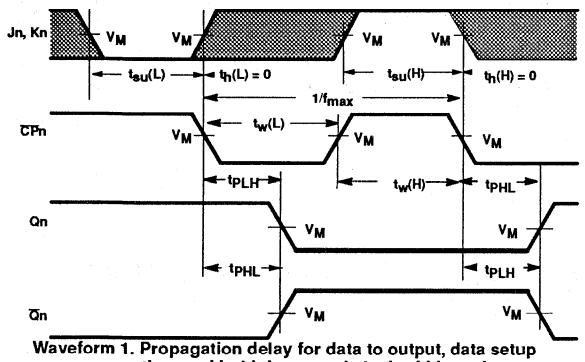
Dual J–K negative edge-triggered flip-flops without reset

74F113

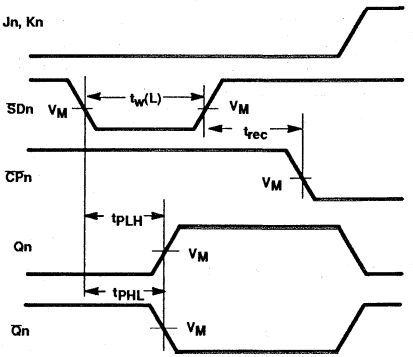
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Jn, Kn to $\overline{CP}$n	Waveform 1	4.0 3.5			5.0 4.0		5.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low Jn, Kn to $\overline{CP}$n	Waveform 1	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_w (H) t_w (L)	$\overline{CP}$n pulse width, high or low	Waveform 1	4.5 4.5			5.0 5.0		5.0 5.0		ns
t_w (L)	$\overline{SD}$n pulse width, low	Waveform 2	4.5			5.0		5.0		ns
t_{rec}	Recovery time, $\overline{SD}$n to CPn	Waveform 2	4.5			5.0		5.0		ns

AC WAVEFORMS



Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency

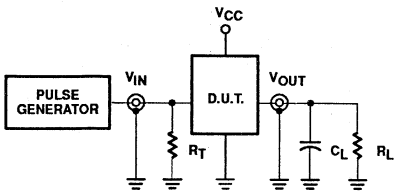


Waveform 2. Propagation delay for set to output, set pulse width, and recovery time for set to clock

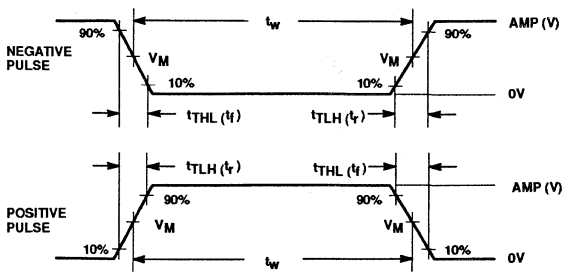
Note to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0340
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Date of issue	March 28, 1989
Status	Product Specification
FAST Products	

FAST 74F114
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flop With Common Clock And Reset

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F114	100MHz	15mA

DESCRIPTION

The 74F114, Dual Negative Edge-Triggered JK-Type Flip-Flop with common clock and reset inputs, features individual J, K, Clock ($\overline{CP}$), Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, true and complementary outputs.

The $\overline{S}_D$ and $\overline{R}_D$ inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the level at the other inputs.

A High level on the clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the $\overline{CP}$.

ORDERING INFORMATION

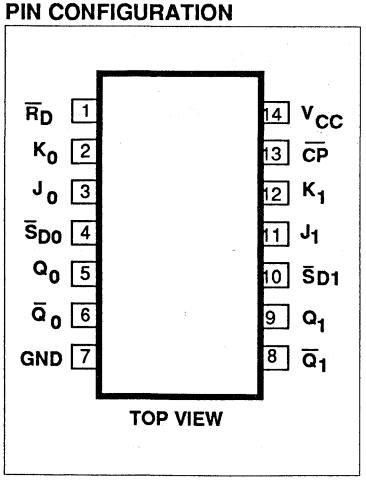
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F114N
14-Pin Plastic SO	N74F114D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20µA/0.6mA
K_0, K_1	K inputs	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{R}_D$	Reset input (active Low)	1.0/10.0	20µA/6.0mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/8.0	20µA/4.8mA
Q_0,$\overline{Q}_0$; Q_1, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

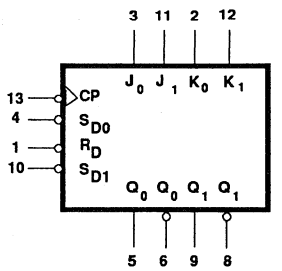
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



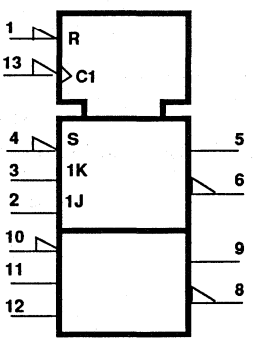
TOP VIEW

LOGIC SYMBOL

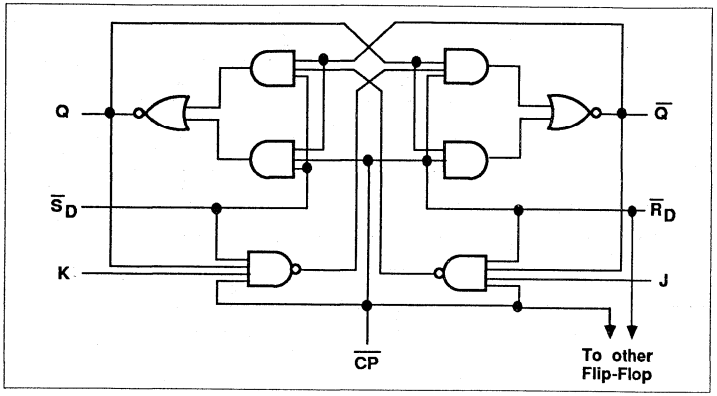


V_{CC} = pin 14
GND = pin 7

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined *
H	H	↓	h	l	$\overline{q}$	q	Toggle
H	H	↓	l	l	L	H	Load "0"(Reset)
H	H	↓	h	l	H	L	Load "1" (Set)
H	H	↓	l	l	q	$\overline{q}$	Hold "no change"

H = High voltage level
h = High voltage level one setup time prior to High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to High-to-Low clock transition
q=Lower case letters indicate the state of the referenced output prior to the High-to-Low clock transition
X = Don't care
↓= High-to-Low clock transition
Asynchronous inputs: Low input to $\overline{S}_D$ sets Q to High level, Low input to $\overline{R}_D$ sets Q to Low level
Set and Reset are independent of clock
Simultaneous Low on both $\overline{S}_D$ and $\overline{R}_D$ makes both Q and $\overline{Q}$ High
* =Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	J_n, K_n	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CP}$					-4.8	mA
		$\overline{S}_{Dn}$					-3.0	mA
		$\overline{R}_D$					-6.0	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.

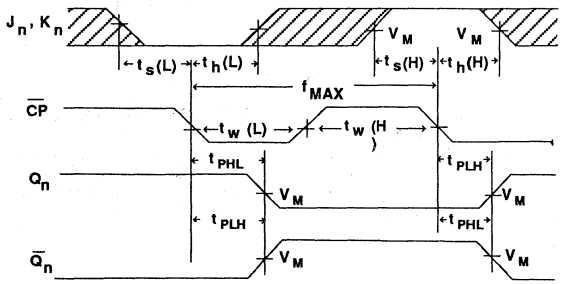
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	5.0 5.5	6.5 7.5	2.0 2.0	7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_D$ to Q_n or $\overline{Q}_n$	Waveform 2,3	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low J_n, $\overline{K}_n$ to $\overline{CP}$	Waveform 1	4.0 3.5			5.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low J_n, $\overline{K}_n$ to $\overline{CP}$	Waveform 1	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	$\overline{CP}$ Pulse width High or Low	Waveform 1	4.5 4.5			5.0 5.0		ns
t_w(L)	$\overline{S}_{Dn}$, $\overline{R}_D$ Pulse width Low	Waveform 2,3	4.5			5.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$, $\overline{R}_D$ to $\overline{CP}$	Waveform 2,3	4.5			5.0		ns

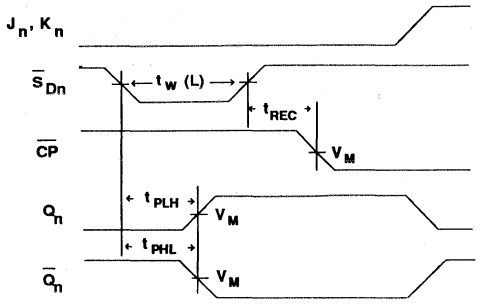
AC WAVEFORMS



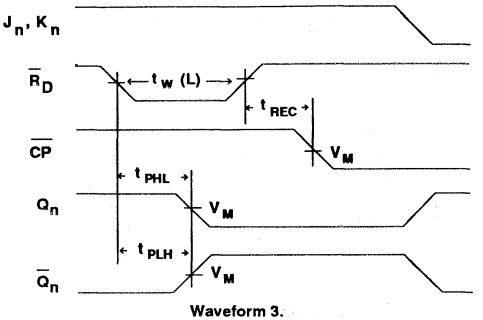
Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Width

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS



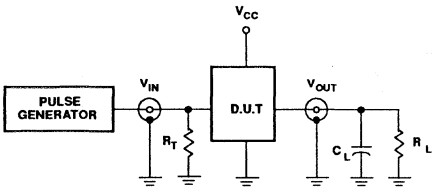
Waveform 2.
Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to clock



Waveform 3.
Propagation Delay forReset to Output, Reset Pulse Width, and Recovery Time for Reset to Clock

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



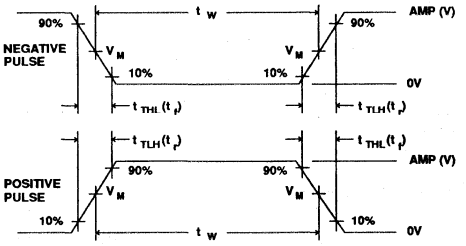
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0341
ECN No.	
Date of issue	June 12, 1990
Status	Product Specification
FAST Products	

FAST 74F125, 74F126
Buffers

74F125 Quad Buffer (3-State)
74F126 Quad BUffer (3-State)

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F125	5.0ns	23mA
74F126	5.0ns	26mA

ORDERING INFORMATION

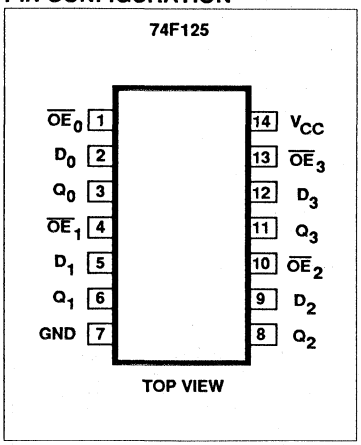
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F125N, N74F126N
14-Pin Plastic SO	N74F125D, N74F126D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

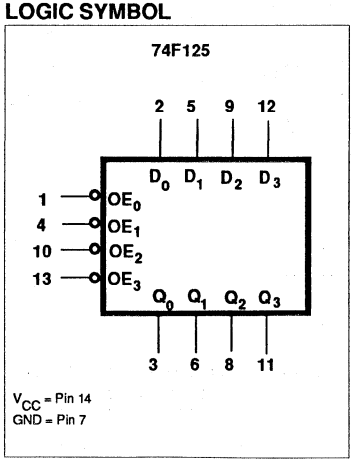
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0-D_3	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$-$\overline{OE}_3$	Output Enable inputs (active Low) , F125	1.0/0.033	20μA/20μA
OE_0-OE_3	Output Enable inputs (active High) , F126	1.0/0.033	20μA/20μA
Q_0-Q_3	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

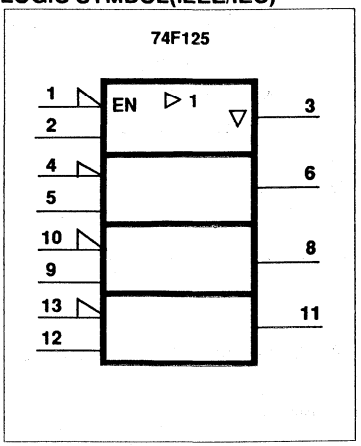
PIN CONFIGURATION



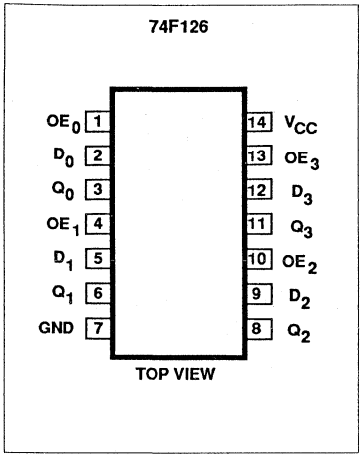
LOGIC SYMBOL



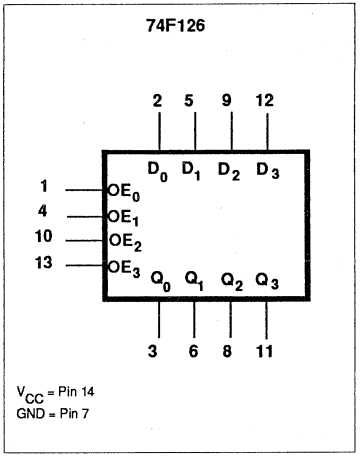
LOGIC SYMBOL(IEEE/IEC)



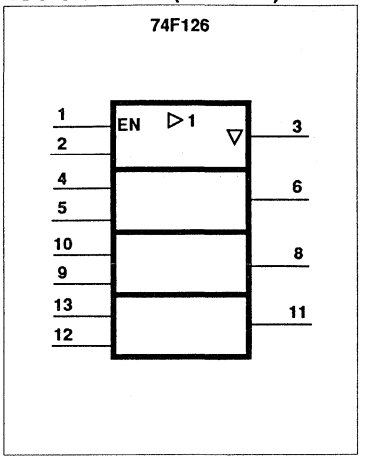
PIN CONFIGURATION



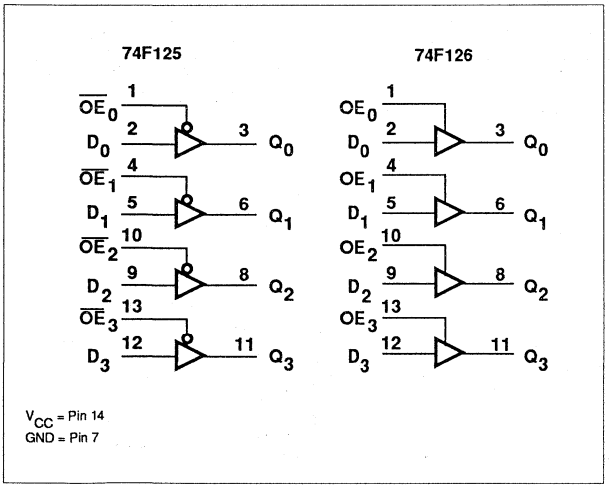
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE, 74F125

INPUTS		OUTPUT
$\overline{OE}_n$	D_n	Q_n
L	L	L
L	H	H
H	X	Z

FUNCTION TABLE, 74F126

INPUTS		OUTPUT
OE_n	D_n	Q_n
H	L	L
H	H	H
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

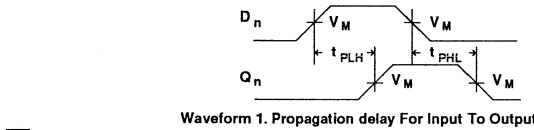
SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
					I_{OH}=-15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum Input voltage			V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O= 0.5V					-50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F125	I_{CCH}	V_{CC} = MAX	$\overline{OE}_n$ = GND, D_n=4.5V			17	24	mA
			I_{CCL}		$\overline{OE}_n$ = D_n=GND			28	40	mA
			I_{CCZ}		$\overline{OE}_n$ = D_n=4.5V			25	35	mA
		'F126	I_{CCH}	V_{CC} = MAX	OE_n = D_n=4.5V			20	30	mA
			I_{CCL}		OE_n = 4.5V, D_n=GND			32	48	mA
			I_{CCZ}		OE_n = GND, D_n=4.5V			26	39	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

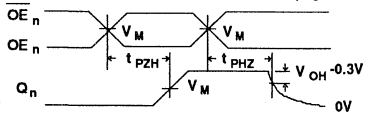
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F125	Waveform 1	2.0 3.0	4.0 5.5	6.0 7.5	2.0 3.0	6.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 2 Waveform 3	3.5 4.0	5.5 6.0	7.5 8.0	3.5 4.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 2 Waveform 3	1.5 1.5	3.5 3.5	5.0 5.5	1.5 1.5	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F126	Waveform 1	2.0 3.0	4.0 5.5	6.5 8.0	2.0 3.0	7.0 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 2 Waveform 3	4.0 4.0	6.0 6.0	7.5 8.0	3.5 3.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 2 Waveform 3	2.0 3.0	4.5 5.5	6.5 7.5	2.0 3.0	7.5 8.0	ns

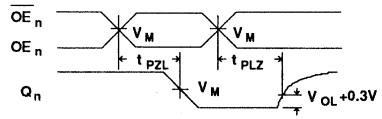
AC WAVEFORMS



Waveform 1. Propagation delay For Input To Output



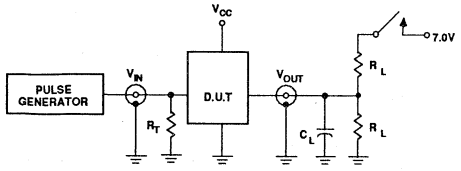
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

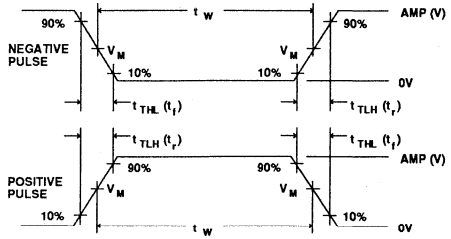
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Schmitt trigger — FAST 74F132

Quad 2-input NAND Schmitt trigger

DESCRIPTION

The 74F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates. Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mv) is determined by reisistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transition of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F132	6.3 ns	13 mA

ORDERING INFORMATION

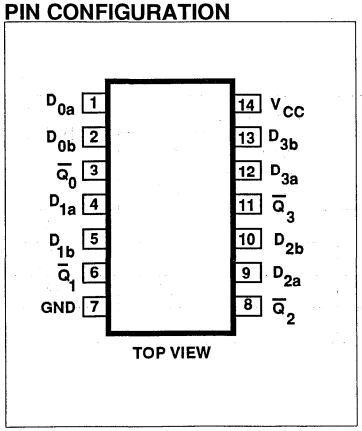
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C
14-Pin Plastic DIP	N74F132N
14-Pin Plastic SO	N74F132D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

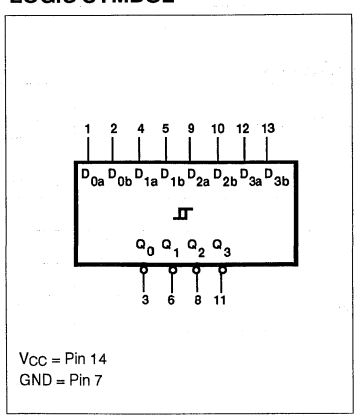
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

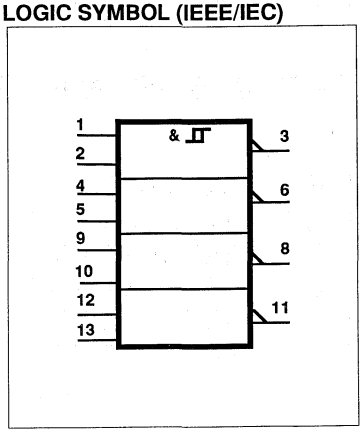
PIN CONFIGURATION



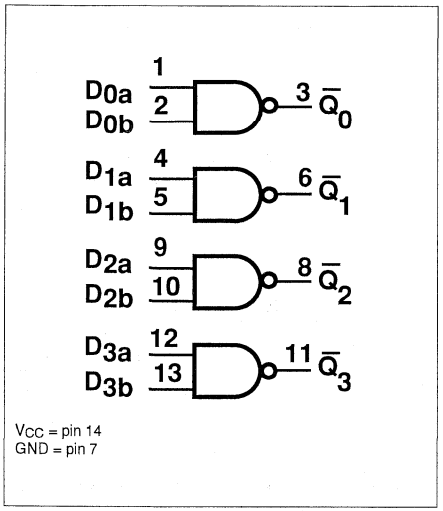
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{T+}	Positive-going threshold		V_{CC} =5.0V		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold		V_{CC} =5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis (V_{T+}- V_{T-})		V_{CC} =5.0V		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} =MIN,	±10%V_{CC}	2.5			V
			V_I=V_{T-MIN}, I_{OH} =MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} =MIN,	±10%V_{CC}		0.30	0.50	V
			V_I=V_{T+MAX}, I_{OL} =MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_{T+}	Input current at positive-going threshold		V_{CC} =5.0V, V_I = V_{T+}			0		µA
I_{T-}	Input current at negative-going threshold		V_{CC} =5.0V, V_I = V_{T-}			-350		µA
I_I	Input current at maximun input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} =MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX	V_{IN}=GND		8.5	12.0	mA
		I_{CCL}		V_{IN}=4.5V		13.0	19.5	mA

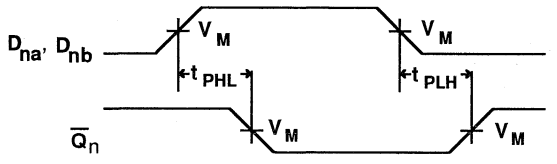
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	3.5 4.5	5.5 6.0	7.0 8.5	3.0 4.5	8.5 9.0	ns

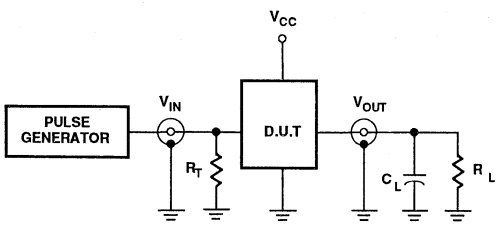
AC WAVEFORMS



Waveform 1.
For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



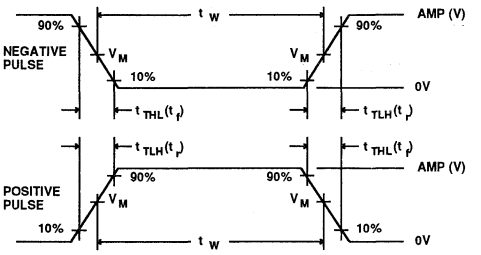
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-1154
ECN No.	97893
Date of issue	October 16, 1989
Status	Product Specification
FAST Products	

FAST 74F133 Gate

13-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F133	4.0 ns	2.0 mA

ORDERING INFORMATION

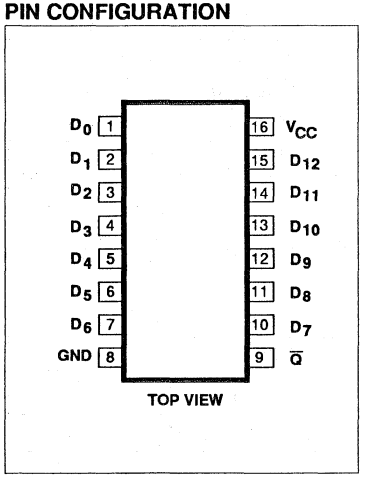
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F133N
14-Pin Plastic SO	N74F133D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

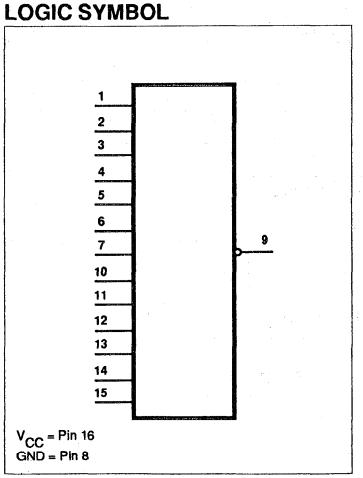
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0-D_{12}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}$	Data Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

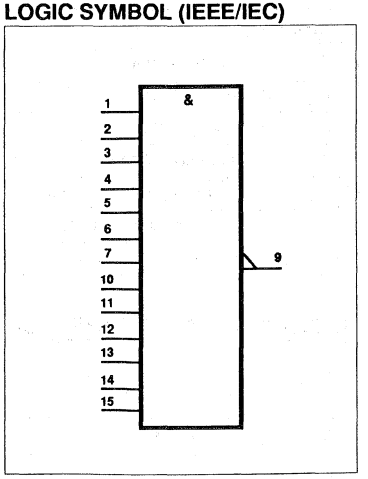
PIN CONFIGURATION



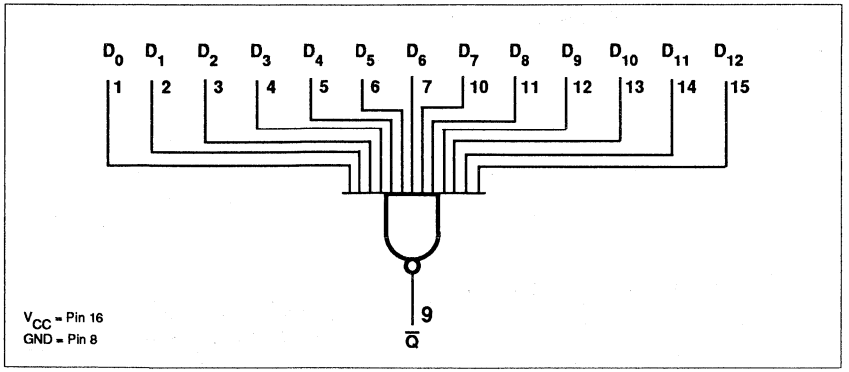
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS													OUTPUT
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	$\overline{Q}$
H	H	H	H	H	H	H	H	H	H	H	H	H	L
Any one input = L													H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

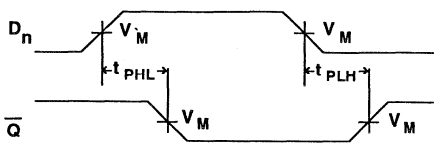
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			1.0	2.0	mA
		I_{CCL}				2.5	4.0	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}$	Waveform 1	2.0 2.5	4.0 4.5	7.0 7.5	1.5 2.0	7.5 8.0	ns

AC WAVEFORMS

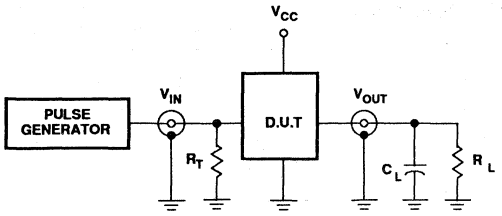


Waveform 1.

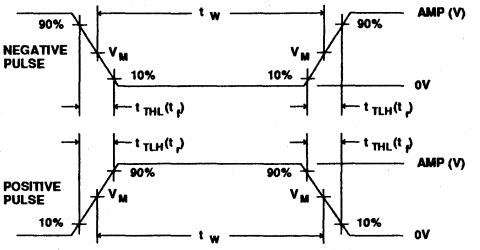
Propagation Delay for Data to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

1–of–8 decoder/demultiplexer — 74F138

FEATURE

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F138 decoder accepts three binary weighted inputs (A0, A1, A2) and when enabled, provides eight mutually exclusive, active low outputs ($\overline{Q}0 - \overline{Q}7$). The device features three enable inputs; two active low ($\overline{E}0$, $\overline{E}1$) and one active high (E2). Every output will be high unless $\overline{E}0$ and $\overline{E}1$ are low and E2 is high. This multiple enable function allows easy parallel expansion of the device to 1–of–32 (5 lines to 32 lines) decoder with just four 74F138s and one inverter (see Fig. 1). The device can be used as an eight output demultiplexer by using one of the active low enable inputs as the data input and the remaining enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active high or active low state.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F138	5.8ns	13mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
16–pin plastic DIP	N74F138N	I74F138N
16–pin plastic SO	N74F138D	I74F138D

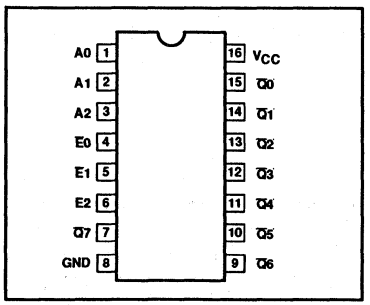
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}0$, $\overline{E}1$	Enable inputs (active low)	1.0/1.0	20µA/0.6mA
E2	Enable input (active high)	1.0/1.0	20µA/0.6mA
$\overline{Q}0 - \overline{Q}7$	Data outputs	50/33	1.0mA/20mA

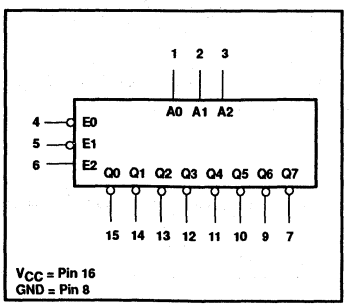
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

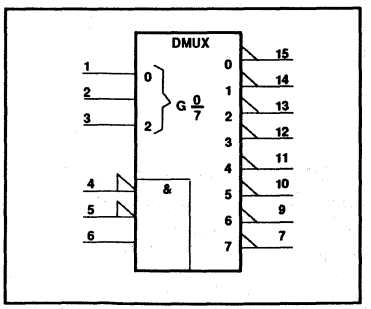
PIN CONFIGURATION



LOGIC SYMBOL

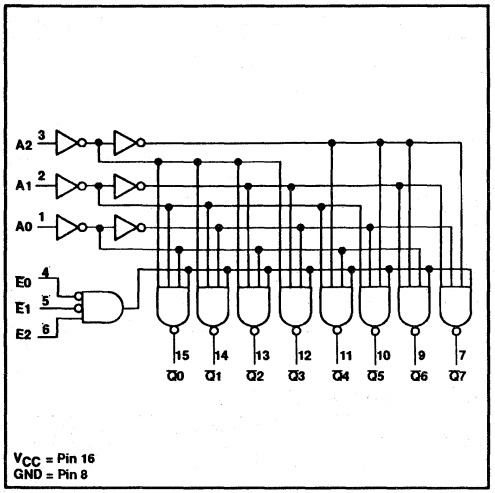


IEC/IEEE SYMBOL



1–of–8 decoder/demultiplexer | 74F138

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E0}$	$\overline{E1}$	E2	A0	A1	A2	$\overline{Q0}$	$\overline{Q1}$	$\overline{Q2}$	$\overline{Q3}$	$\overline{Q4}$	$\overline{Q5}$	$\overline{Q6}$	$\overline{Q7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Notes to function table
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care

APPLICATION

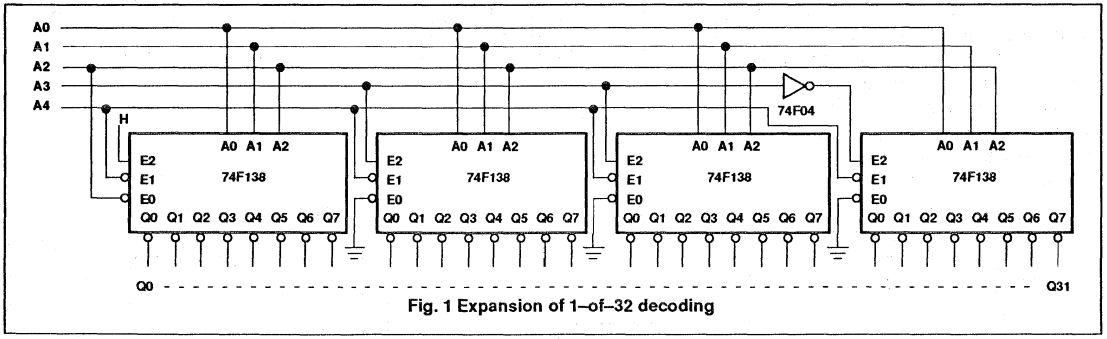


Fig. 1 Expansion of 1–of–32 decoding

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage	V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage	V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short–circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				13	20	mA

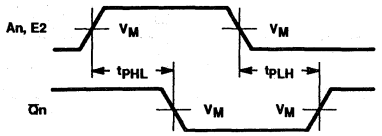
Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IN} on all inputs = 4.5V.

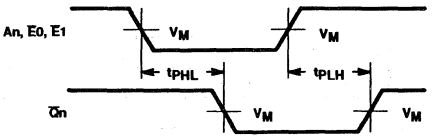
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Q}n$	Waveform 1, 2	3.5 4.0	5.6 6.1	7.0 8.0	3.5 4.0	8.0 9.0	3.0 3.5	8.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}0$ or $\overline{E}1$ to $\overline{Q}n$	Waveform 2	3.5 3.0	6.4 5.3	7.0 7.0	3.5 3.0	8.0 7.5	3.0 3.0	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay E2 to $\overline{Q}n$	Waveform 1	4.0 3.5	6.2 5.6	8.0 7.5	4.0 3.5	9.0 8.5	4.0 3.5	9.5 8.5	ns

AC WAVEFORMS



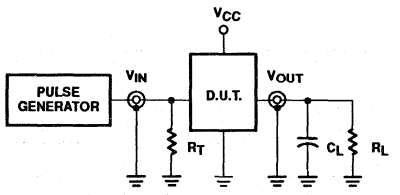
Waveform 1. Propagation delay for inverting outputs



Waveform 2. Propagation delay for non-Inverting outputs

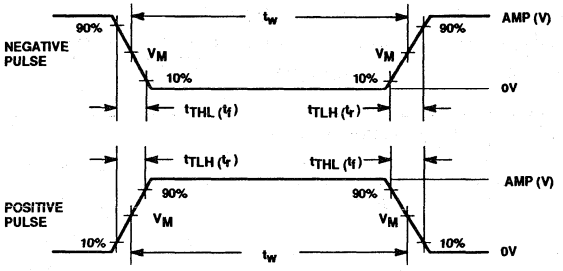
Note to AC waveforms
1. For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0344
ECN No.	98903
Date of issue	February 23, 1990
Status	Product Specification
FAST Products	

FAST 74F139
Decoder/Demultiplexer

Dual 1-of-4 Decoder//Demultiplexer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F139	5.3ns	13mA

FEATURES

- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Multifunction capability**

DESCRIPTION

The 74F139 is a high speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_{0n}, A_{1n}) and providing four mutually exclusive active-Low outputs ($\overline{Q}_{0n}$ - $\overline{Q}_{3n}$). Each decoder has an active-Low Enable ($\overline{E}$). When $\overline{E}$ is High, every output is forced High. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

ORDERING INFORMATION

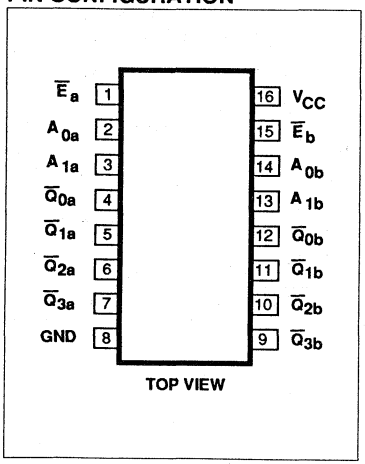
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F139N
16-Pin Plastic SO	N74F139D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

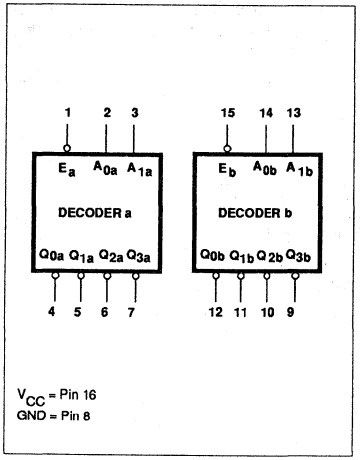
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{na}, A_{nb}	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Q}_{0n}$ - $\overline{Q}_{3n}$	Data outputs (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

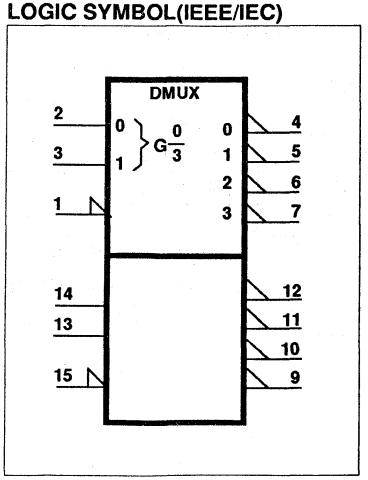
PIN CONFIGURATION



LOGIC SYMBOL

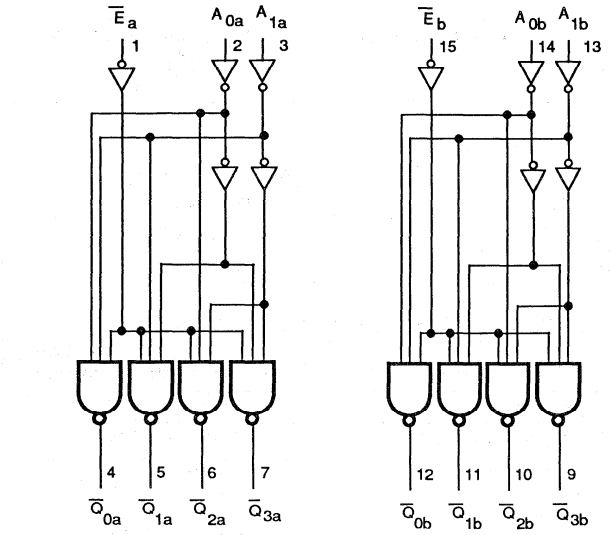


LOGIC SYMBOL(IEEE/IEC)



Decoder/Demultiplexer FAST 74F139

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuitoutput current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]	V_{CC} = MAX			13	20	mA

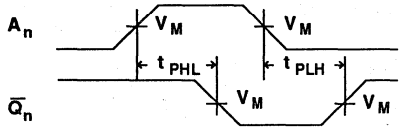
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

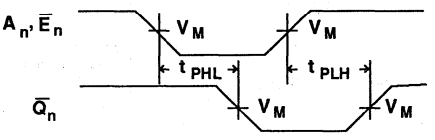
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_0 or A_1 to $\overline{Q}_{na}$, $\overline{Q}_{nb}$	Waveform 1 , 2	3.5 4.0	5.3 6.1	7.0 8.0	3.0 4.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Q}_{na}$, $\overline{Q}_{nb}$	Waveform 2	3.5 3.0	5.4 4.7	7.0 6.5	3.5 3.0	8.0 7.5	ns

AC WAVEFORMS



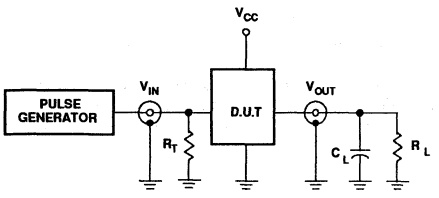
Waveform 1. For Inverting Outputs



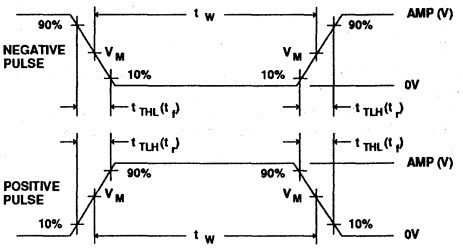
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M =1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

Document No.	853-0345
ECN No.	98994
Date of issue	March 1, 1990
Status	Product Specification
FAST Products	

FAST 74F148
Encoder

8-Input Priority Encoder

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F148	6.0ns	23mA

FEATURES

- **Code conversions**
- **Multi-channel D/A converter**
- **Decimal-to-BCD converter**
- **Cascading for priority encoding of "N" bits**
- **Input enable capability**
- **Priority encoding-automatic selection of highest priority input line**
- **Output enable-active Low when all inputs are High**
- **Group signal output-active when any input is Low**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F148N
16-Pin Plastic SO	N74F148D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

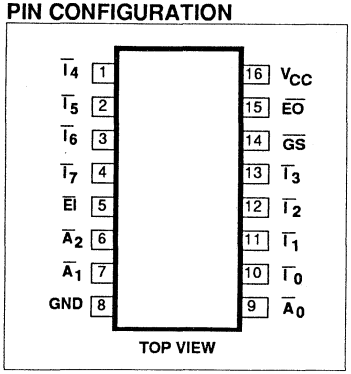
	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{I}_1$-$\overline{I}_7$	Priority inputs (active Low)	1.0/2.0	20µA/1.2mA
$\overline{I}_0$	Priority input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{EI}$ PINS	Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{EO}$	Enable output (active Low)	50/33	1.0mA/20mA
$\overline{GS}$	Group select output (active Low)	50/33	1.0mA/20mA
$\overline{A}_0$- $\overline{A}_2$	Address outputs (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

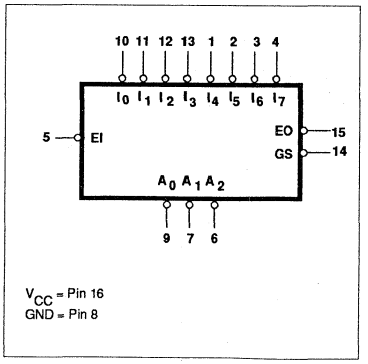
DESCRIPTION

The 74F148 8-input priority encoder accepts data from eight active-Low inputs and provides a binary representation on the three active-Low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I}_7$ having the highest priority. A High on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (High) state and allow new data to settle without producing erroneous information at the outputs. A Group Signal ($\overline{GS}$) output and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active-Low when any input is Low: this indicates when any input is active. The $\overline{EO}$ is active-Low when all inputs are High. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are active-High when the Enable Input is High.

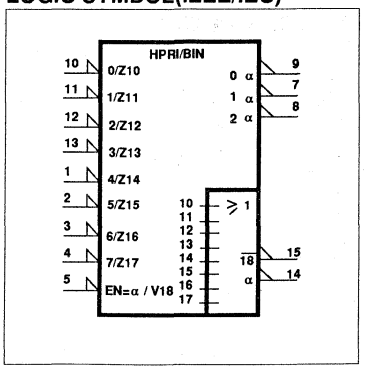
PIN CONFIGURATION



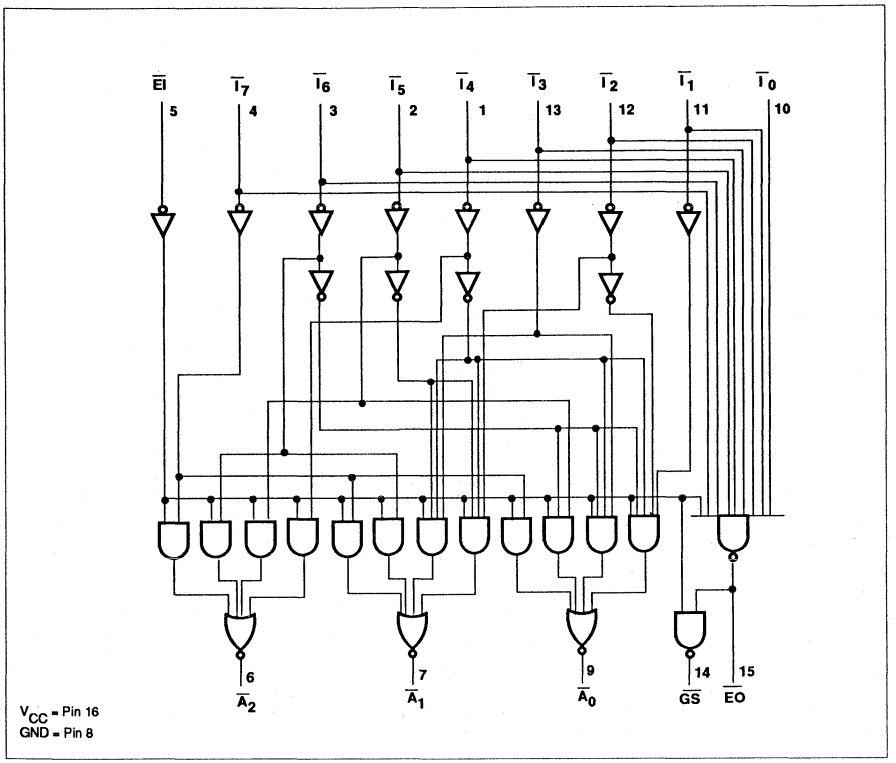
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM

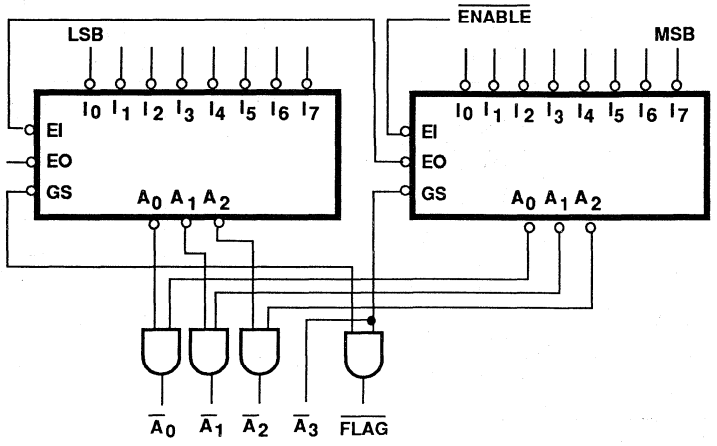


FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION



16-Input priority Encoder

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

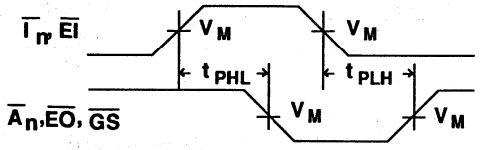
SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current $\bar{I}_0$	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
	Low-level input current $\bar{I}_1$-$\bar{I}_7$, $\overline{EI}$					-1.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]	V_{CC} = MAX			23	35	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IN} on all inputs=4.5V.

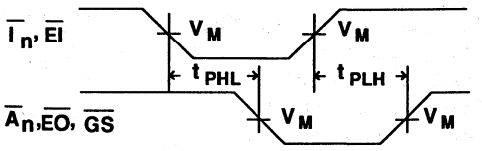
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\bar{I}_n$ to $\bar{A}_n$	Waveform 2	3.5 3.5	6.0 6.0	9.0 9.0	3.5 3.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{I}_n$ to $\overline{EO}$	Waveform 1	1.5 1.5	3.0 2.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{I}_n$ to $\overline{GS}$	Waveform 2	2.0 2.0	4.0 4.0	8.0 8.0	2.0 2.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\bar{A}_n$	Waveform 2	3.5 3.0	6.0 5.5	8.5 8.0	3.5 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{GS}$	Waveform 2	2.5 3.0	4.5 5.5	7.0 7.5	2.5 3.0	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{EO}$	Waveform 2	3.0 3.5	5.0 5.0	7.0 7.5	3.0 3.5	8.0 9.0	ns

AC WAVEFORMS



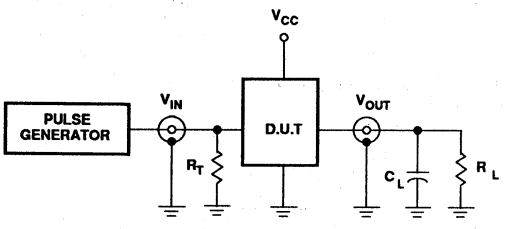
Waveform 1. For Inverting Outputs



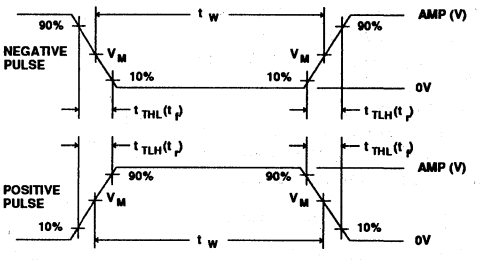
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M =1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

Document No.	853-1158
ECN No.	95943
Date of issue	March 3, 1989
Status	Product Specification
FAST Products	

FAST 74F151, 74F151A Multiplexers

74F151 8-input Multiplexer
74F151A 8-input Multiplexer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F151	5.5ns	13.5mA
74F151A	4.5ns	17mA

FEATURES

- **High speed 8-to-1 multiplexing**
- **On chip decoding**
- **Multifunction capability**
- **Complementary outputs**
- **See 'F251/'F251A for 3-state version**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F151N, N74F151AN
16-Pin Plastic SO	N74F151D, N74F151AD

DESCRIPTION

The 74F151 and 74F151A are logic implementations of a single-pole, 8-position switch with the switch position controlled by the state of three Select (S_0, S_1, S_2) inputs. True(Y) and complementary ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active Low. When $\overline{E}$ is High, the $\overline{Y}$ output is High and the Y output is Low, regardless of all other inputs. In one package the 74F151 or 74F151A provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and the negation with correct manipulation.

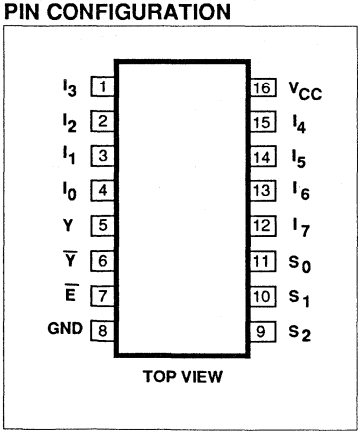
74F151A is the faster version of 74F151.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

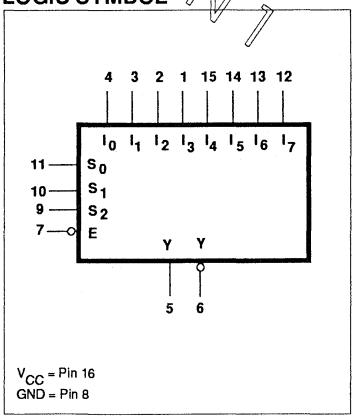
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0-I_7	Data inputs	1.0/1.0	20µA/0.6mA
S_0-S_2	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
Y, $\overline{Y}$	Data outputs	150/33	3mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

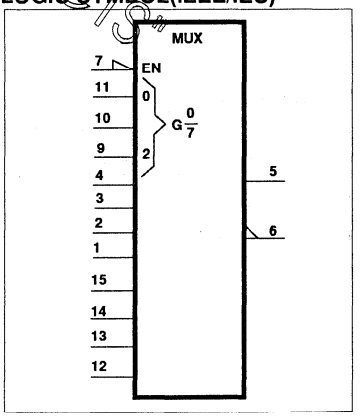
PIN CONFIGURATION



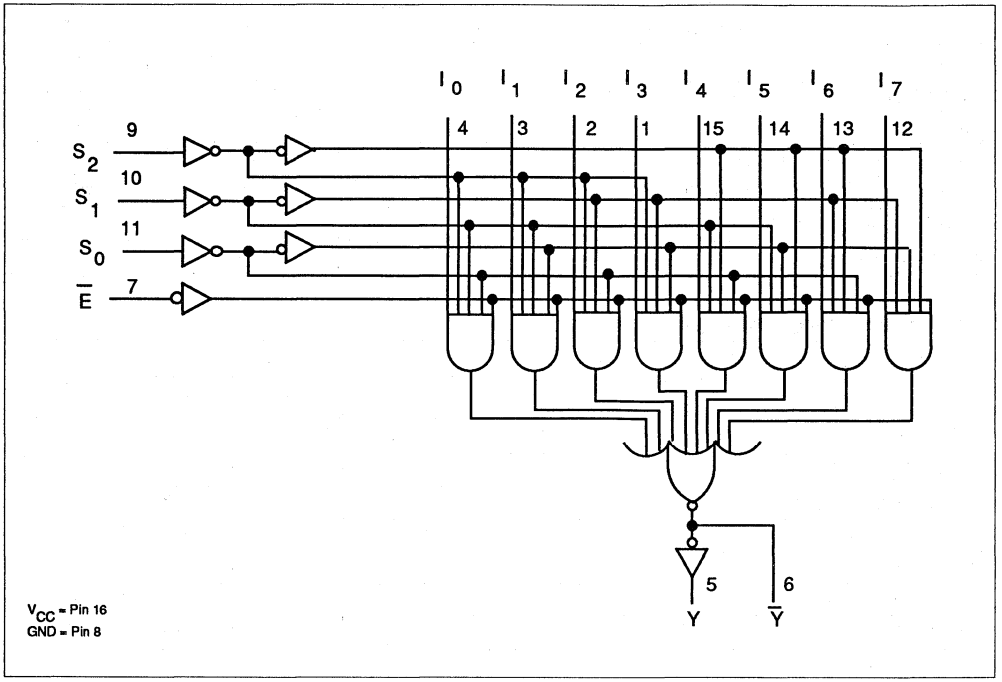
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{E}$	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F151	V_{CC} = MAX			13	18	mA
		I_{CCL}					15	20	mA
		I_{CCH}	74F151A	V_{CC} = MAX			18	25	mA
		I_{CCL}					17	25	mA

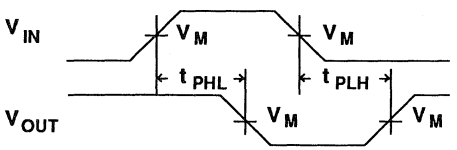
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

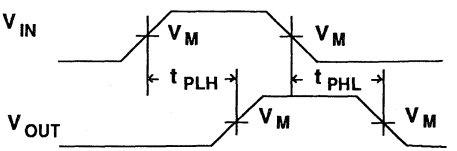
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F151	Waveform 1	3.0 3.0	4.5 4.5	6.5 6.5	2.5 3.0	9.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$		Waveform 2	2.0 1.0	4.0 2.5	6.0 4.0	2.0 1.0	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y		Waveform 1,2	4.0 4.5	7.0 7.0	9.5 9.0	4.0 4.5	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$		Waveform 1,2	4.0 2.0	6.5 4.5	9.0 7.0	3.5 2.0	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y		Waveform 1	6.0 4.0	8.0 5.5	10.0 7.0	5.5 4.0	11.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$		Waveform 1	3.5 4.0	5.0 5.5	6.5 7.5	3.5 4.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F151A	Waveform 1	2.5 2.5	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$		Waveform 2	2.0 1.0	4.0 2.0	7.0 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y		Waveform 1,2	4.5 4.0	6.5 6.0	10.0 8.5	4.0 3.5	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$		Waveform 1,2	3.5 2.5	5.5 4.5	8.5 7.0	3.0 2.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y		Waveform 1	4.0 3.0	6.5 5.0	9.0 7.0	3.5 3.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$		Waveform 1	2.5 2.0	4.5 3.5	6.5 5.5	2.5 1.5	7.0 6.0	ns

AC WAVEFORMS



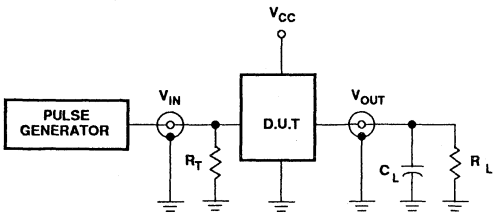
Waveform 1. For Inverting Outputs



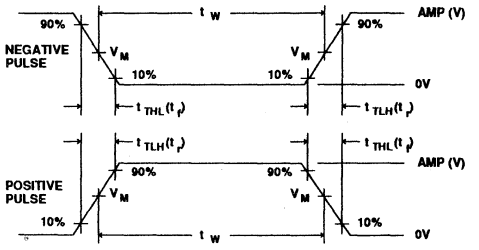
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M =1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

Document No.	853-0100
ECN No.	96351
Date of issue	April 14, 1989
Status	Product Specification
FAST Products	

FAST 74F153
Multiplexer

Dual 4-Line to 1-Line Multiplexer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F153	7.0ns	12mA

FEATURES

- **Non-inverting outputs**
- **Separate enable for each section**
- **Common select inputs**
- **See 'F253 for 3-state version**

DESCRIPTION

The 74F153 is a dual 4-input multiplexer that can select 2 bits of data from up to four sources selected by common Select inputs (S_0,S_1). The two 4-input multiplexer circuits have individual active-Low Enables ($\overline{E}_a$,$\overline{E}_b$) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced Low when the corresponding Enables ($\overline{E}_a$,$\overline{E}_b$) are High.

The 'F153 is the logic implementation of a 2-pole, 4-position switch where the switch is determined by the logic levels supplied to the common select inputs.

ORDERING INFORMATION

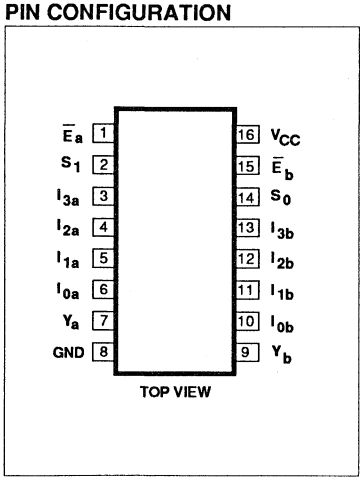
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F153N
16-Pin Plastic SO	N74F153D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

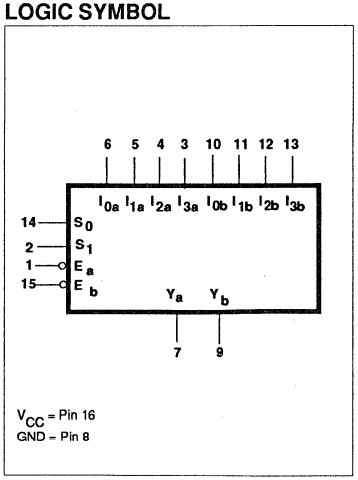
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}- I_{3a}	Port A data inputs	1.0/1.0	20µA/0.6mA
I_{0b}- I_{3b}	Port B data inputs	1.0/1.0	20µA/0.6mA
S_0, S_1	Common Select inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$	Port A Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{E}_b$	Port B Enable input (active Low)	1.0/1.0	20µA/0.6mA
Y_a, Y_b	Port A, B data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

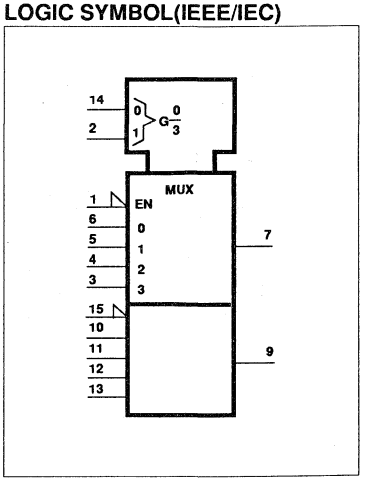
PIN CONFIGURATION



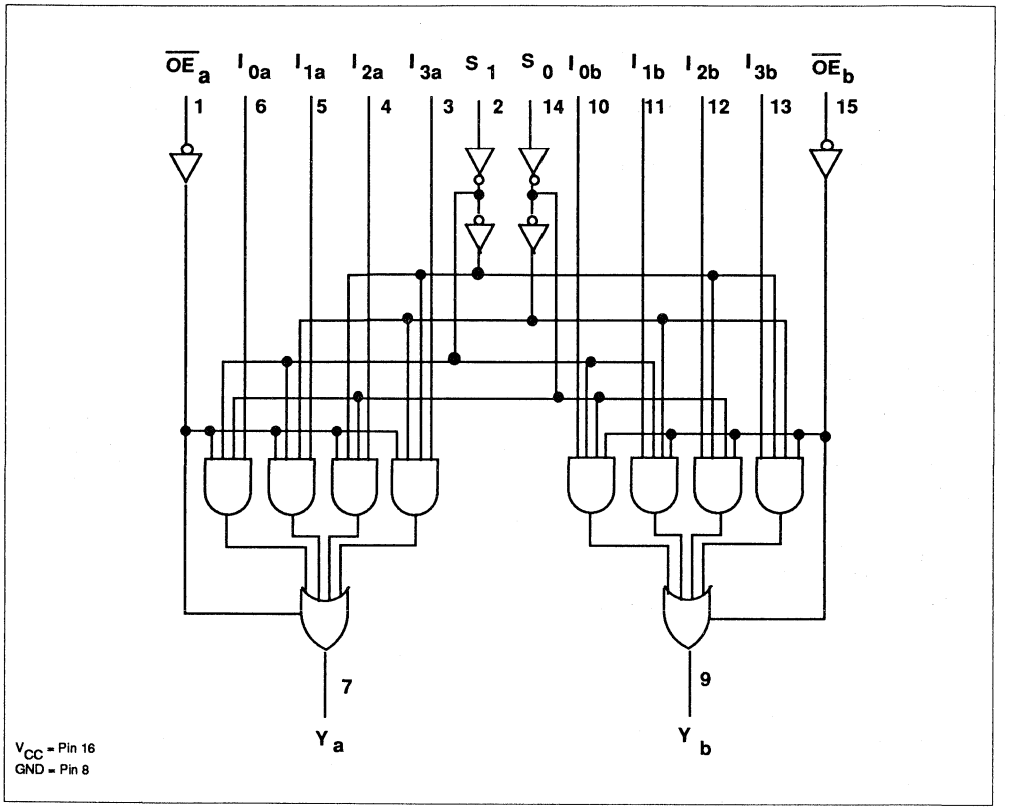
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	$\overline{E}_n$	I_{on}	I_{1n}	I_{2n}	I_{3n}	Y_n
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{E}_n$=GND, S_n=I_n=4.5V		12	20	mA
		I_{CCL}		$\overline{E}_n$=S_n=I_n=GND		12	20	mA

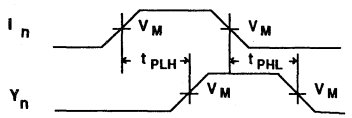
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

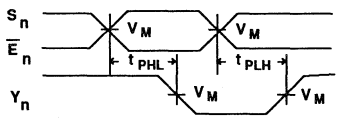
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 2	5.0 5.0	8.0 8.0	10.5 10.5	4.5 4.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y_n	Waveform 2	5.0 4.0	7.5 5.5	9.0 7.0	4.5 3.5	10.5 8.0	ns

AC WAVEFORMS



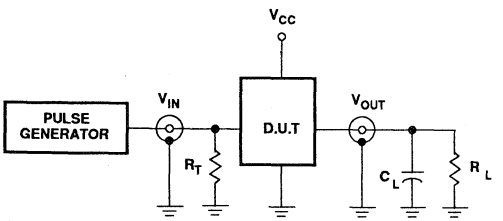
Waveform 1. Propagation Delay, Data to Output



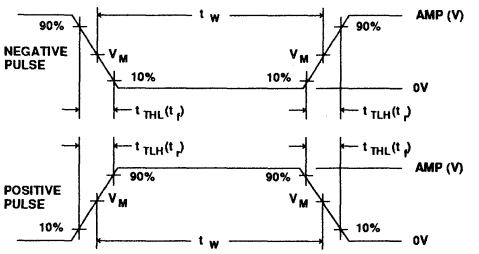
Waveform 2. Propagation Delay, Enable and Select to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-1155
ECN No.	98493
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F154
Decoder/Demultiplexer

1-of-16 Decoder/Demultiplexer

FEATURES

- **16-line demultiplexing capability**
- **Mutually exclusive outputs**
- **2-input enable gate for strobing or expansion**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F154	5.5 ns	26mA

DESCRIPTION

The 74F154 decoder accepts four active High binary address inputs and provides 16 mutually exclusive active Low outputs. The 2-input Enable ($\overline{E}_0$, $\overline{E}_1$) gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The Enable gate has two AND'ed inputs which must be Low to enable the outputs.

The 74F154 can be used as a 1-of-16 demultiplexer by using one of the Enable inputs as the multiplexed data input. When the other Enable is Low, the addressed output will follow the state of the applied data.

ORDERING INFORMATION

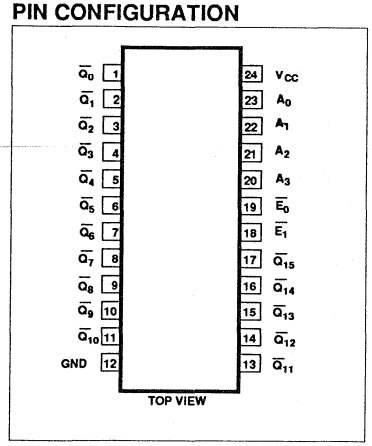
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F154N
24-Pin Plastic SOL	N74F154D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

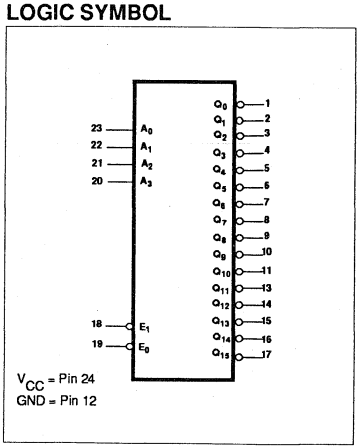
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{O}_0$ - $\overline{O}_{15}$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

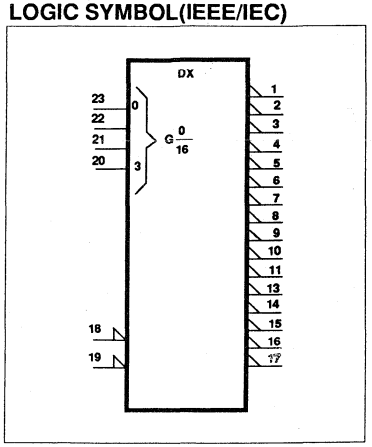
PIN CONFIGURATION



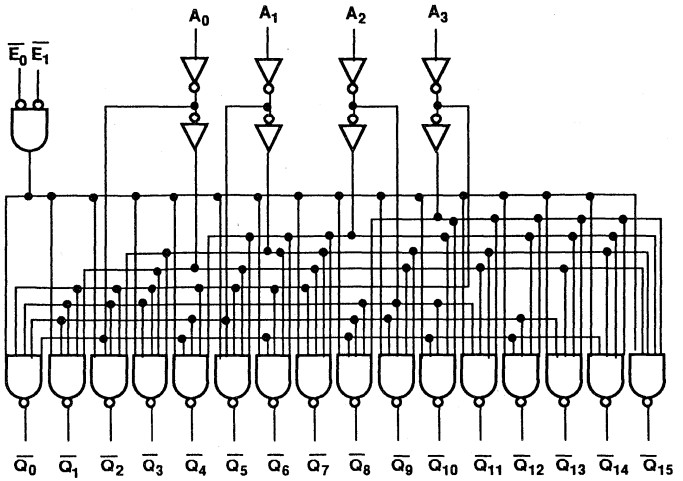
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC}=pin 24
GND=pin 12

FUNCTION TABLE

INPUTS						OUTPUTS													
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$	$\overline{Q}_{10}$	$\overline{Q}_{11}$	$\overline{Q}_{12}$	$\overline{Q}_{13}$	$\overline{Q}_{14}$	$\overline{Q}_{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			26	40	mA
		I_{CCL}				35	45	mA

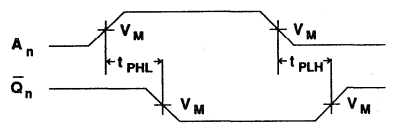
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

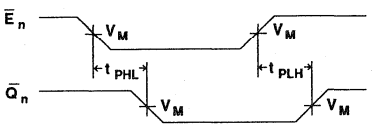
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 1	2.0 3.5	5.0 6.5	9.5 10.0	1.5 3.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n	Waveform 2	2.0 4.0	4.0 6.0	7.5 9.0	1.5 3.5	8.0 9.5	ns

AC WAVEFORMS



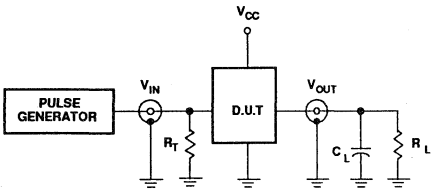
Waveform 1. Propagation Delay For Address To Output



Waveform 2. Propagation Delay For Enable To Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



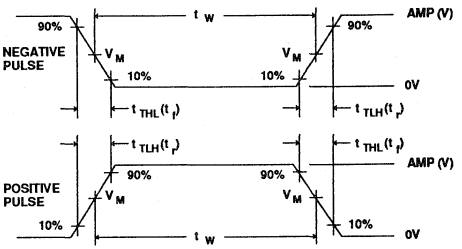
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0346
ECN No.	94810
Date of issue	October 13, 1988
Status	Product Specification
FAST Products	

FAST 74F157, 74F157A 74F158, 74F158A

Data Selectors/Multiplexers

74F157/157A Quad 2-Input Data Selector/ Multiplexer, Non-Inverting
74F158/158A Quad 2-Input Data Selector/Multiplexer, Inverting

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F157	4.6ns	15mA
74F158	3.7ns	10mA
74F157A	4.6ns	15mA
74F158A	3.7ns	10mA

DESCRIPTION

The 74F157/74F157A is a high speed Quad 2-input multiplexer which selects 4 bits of data from one of two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active when Low. When $\overline{E}$ is High, all of the outputs (Y_n) are forced Low regardless of all other input conditions.

Moving data from two registers to a common output bus is a common use of the 'F157/157A. The state of the Select input determines the particular register from which the data comes.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

The 74F158/74F158A is similar but has inverting outputs ($\overline{Y}_n$).

ORDERING INFORMATION

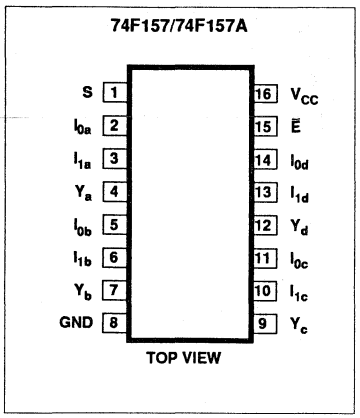
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-pin Plastic DIP	N74F157N, N74F157AN, N74F158N, N74F158AN
16-pin Plastic SO	N74F157D, N74F157AD, N74F158D, N74F158AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

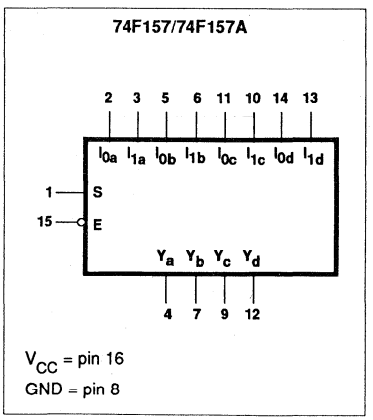
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{na}, I_{nb}, I_{nc}, I_{nd}	Data inputs	1.0/1.0	20µA/0.6mA
S	Select input	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input	1.0/1.0	20µA/0.6mA
Y_a - Y_d	Data outputs ('F157/'F157A)	50/33	1.0mA/20mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs ('F158/'F158A)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

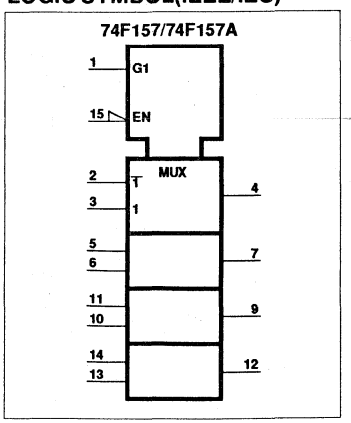
PIN CONFIGURATION



LOGIC SYMBOL

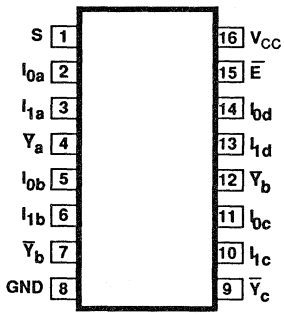


LOGIC SYMBOL(IEEE/IEC)



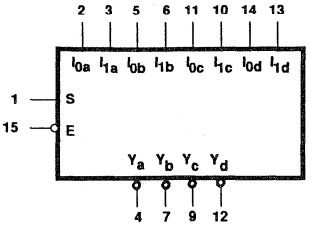
PIN CONFIGURATION

74F158/158A



LOGIC SYMBOL

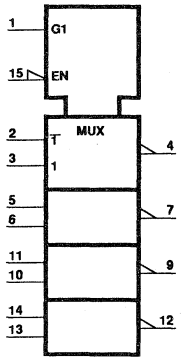
74F158/158A



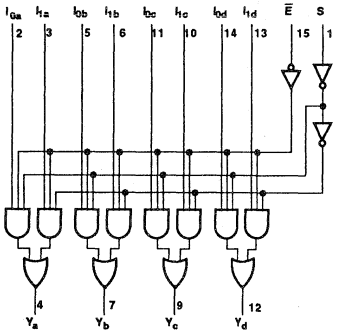
V_{CC} = pin 16
GND = pin 8

LOGIC SYMBOL(IEEE/IEC)

74F158/158A

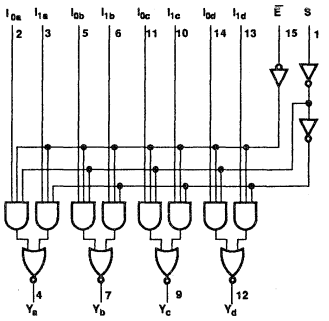


LOGIC DIAGRAM, 74F157/157A



V_{CC} = pin 16
GND = pin 8

LOGIC DIAGRAM, 74F158/158A



V_{CC} = pin 16
GND = pin 8

FUNCTION TABLE, 74F157/157A

INPUTS				OUTPUT
$\overline{E}$	S	I_{0n}	I_{1n}	Y_n
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE, 74F158/158A

INPUTS				OUTPUT
$\overline{E}$	S	I_{0n}	I_{1n}	$\overline{Y}_n$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)	'F157/157A	V_{CC} = MAX			15.0	23.0	mA
		'F158/158A				14.0	19.0	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

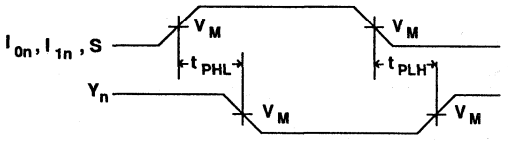
AC ELECTRICAL CHARACTERISTICS for 74F157 and 74F158

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{0n}, I_{1n} to Y_n	74F157	Waveform 1	3.5 2.5	4.5 3.5	7.0 5.5	3.0 1.5	8.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y_n		Waveform 3	5.0 3.8	7.5 5.0	10.0 7.0	5.0 3.8	11.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Y_n		Waveform 1	4.5 3.5	8.0 6.0	13.0 8.0	4.5 3.5	15.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay I_{0n}, I_{1n} to $\overline{Y}_n$	74F158	Waveform 2	3.0 1.5	4.0 2.5	5.9 4.5	2.5 1.0	7.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}_n$		Waveform 4	4.5 3.5	6.0 5.5	8.0 8.5	4.0 3.5	9.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$		Waveform 2	4.0 4.0	6.5 5.5	8.5 9.0	4.0 3.5	9.5 10.5	ns

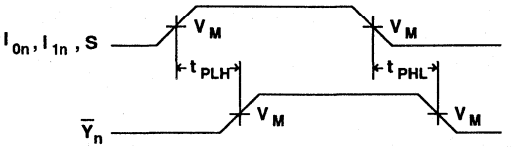
AC ELECTRICAL CHARACTERISTICS for 74F157A and 74F158A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{0n}, I_{1n} to Y_n	74F157A	Waveform 1	3.5 2.5	4.5 3.5	6.5 5.0	3.0 1.5	7.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y_n		Waveform 3	6.0 4.0	7.5 5.0	9.0 6.5	5.5 4.0	10.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Y_n		Waveform 1	5.5 4.5	7.5 6.0	10.0 7.5	5.0 4.0	11.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{0n}, I_{1n} to $\overline{Y}_n$	74F158A	Waveform 2	3.0 1.5	4.0 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}_n$		Waveform 4	4.5 5.0	5.5 6.0	7.0 7.5	4.0 5.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$		Waveform 2	4.5 4.0	6.5 5.5	8.5 7.5	4.0 3.5	9.5 8.0	ns

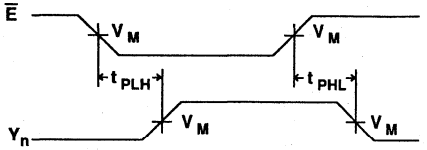
AC WAVEFORMS



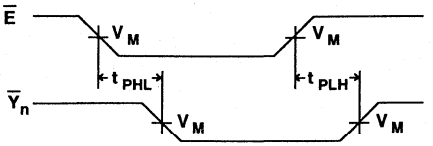
Waveform 1. Propagation Delay For Data And Select To Output



Waveform 2. Propagation Delay For Data And Select To Output



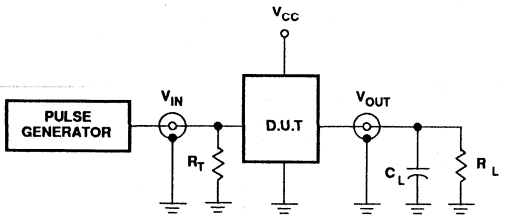
Waveform 3. Propagation Delay For Enable To Output



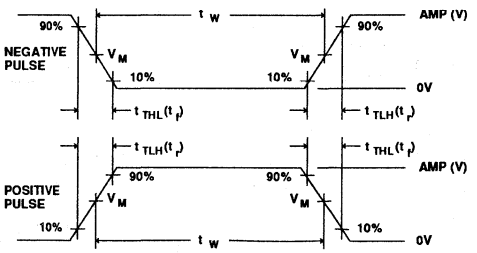
Waveform 4. Propagation Delay For Enable To Output

NOTE: For all waveforms, V_M =1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0347
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Date of issue	October 7, 1988
Status	Product Specification
FAST Products	

FAST 74F160A,74F161A 74F162A,74F163A Counters

'F160A, 'F162A BCD Decade Counter
'F161A, 'F163A 4-Bit Binary Counter

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F160A,74F161A 74F162A,74F163A	130MHz	46mA

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous Master Reset ('F160A, 'F161A)**
- **Synchronous Reset ('F162A, 'F163A)**
- **High speed synchronous expansion**
- **Typical count rate of 130MHz**

DESCRIPTION

Synchronous presettable decade ('F160A, 'F162A) and 4-bit binary('F161A, 'F163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The clock input is buffered.

The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0-D_3 inputs to be loaded into the counter on the positive-going edge of the clock (provided that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

ORDERING INFORMATION

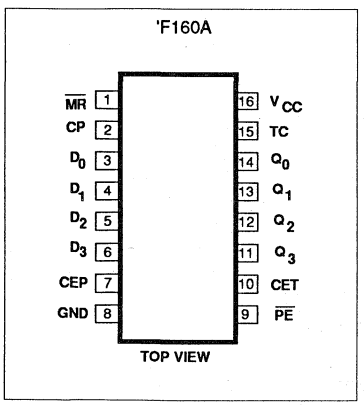
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F160AN, N74F161AN, N74F162AN, N74F163AN
16-Pin Plastic SO	N74F160AD, N74F161AD, N74F162AD, N74F163AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

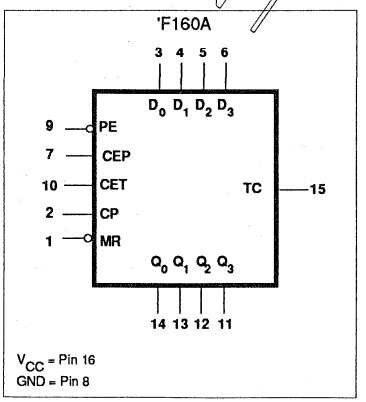
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
CEP	Count Enable Parallel input	1.0/1.0	20µA/0.6mA
CET	Count Enable Trickle input	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{MR}$	Asynchronous Master Reset input (active Low) for 'F160A and 'F161A	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low) for 'F162A and 'F163A	1.0/1.0	20µA/0.6mA
TC	Terminal count output	50/33	1.0mA/20mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

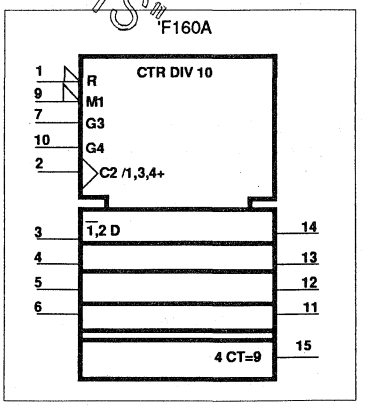
PIN CONFIGURATION



LOGIC SYMBOL

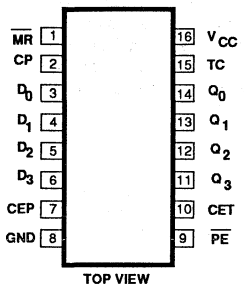


LOGIC SYMBOL(IEEE/IEC)



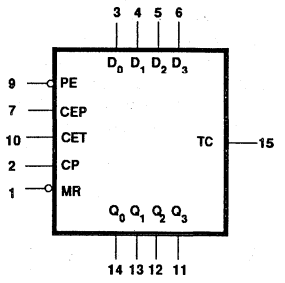
PIN CONFIGURATION

'F161A



LOGIC SYMBOL

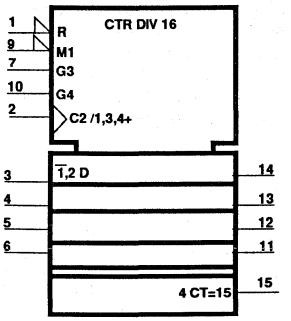
'F161A



VCC = Pin 16
GND = Pin 8

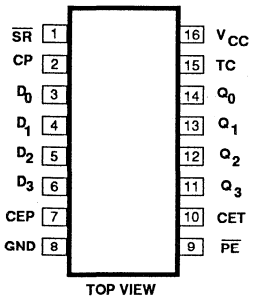
LOGIC SYMBOL(IEEE/IEC)

'F161A



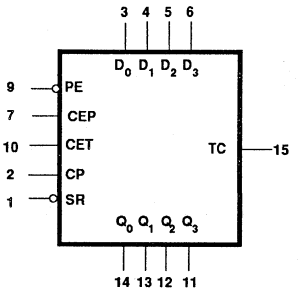
PIN CONFIGURATION

'F162A



LOGIC SYMBOL

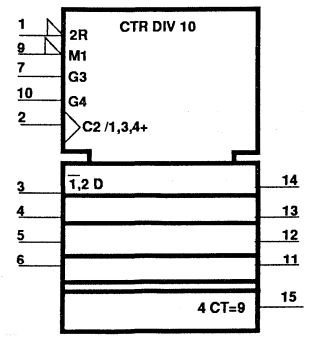
'F162A



VCC = Pin 16
GND = Pin 8

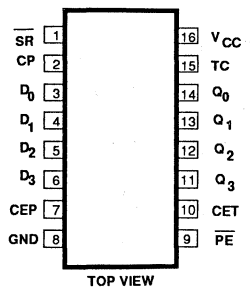
LOGIC SYMBOL(IEEE/IEC)

'F162A



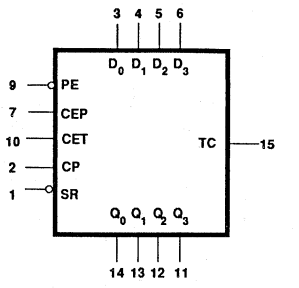
PIN CONFIGURATION

'F163A



LOGIC SYMBOL

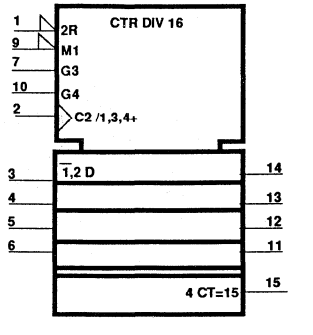
'F163A



VCC = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)

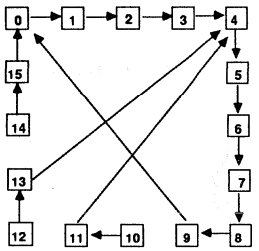
'F163A



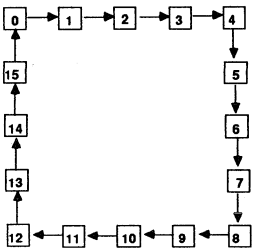
A Low level at the Master Reset ($\overline{MR}$) input sets all the four outputs of the flip-flops (Q_0 - Q_3) in 'F160A and 'F161A to Low levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function). For the 'F162A/'F163A the clear function is synchronous. A Low level at the Synchronous Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q_0-Q_3) to Low levels after the next positive-going transition on the clock (CP) input (provided that the setup and hold time requirements for $\overline{SR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A). The carry look-ahead simplifies serial cascading of the counters. Both Count Enable (CEP and CET) inputs must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B). The TC output is subjected to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

STATE DIAGRAM

Logic equations: Count Enable=CEP•CET•$\overline{PE}$
TC=Q_0•$\overline{Q}_1$•$\overline{Q}_2$•Q_3•CET
'F160A, 'F162A



Logic equations: Count Enable=CEP•CET•$\overline{PE}$
TC=Q_0•Q_1•Q_2•Q_3•CET
'F161A,'F163A



APPLICATIONS

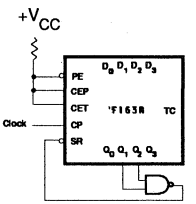


Fig. A Maximum count modifying scheme
Terminal count = 6

H H = Enable count
or
L L = Disable count

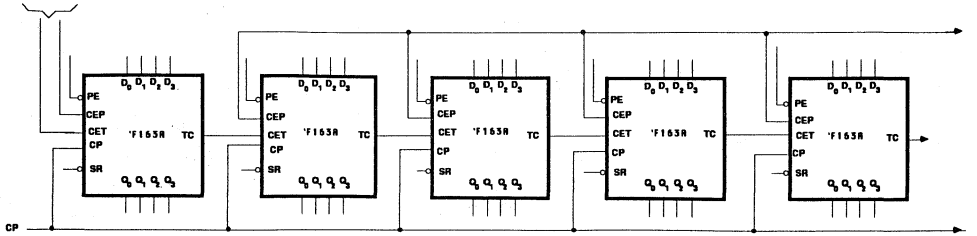


Fig. B Synchronous multistage counting scheme

MODE SELECT-FUNCTION TABLE for 'F160A, 'F161A

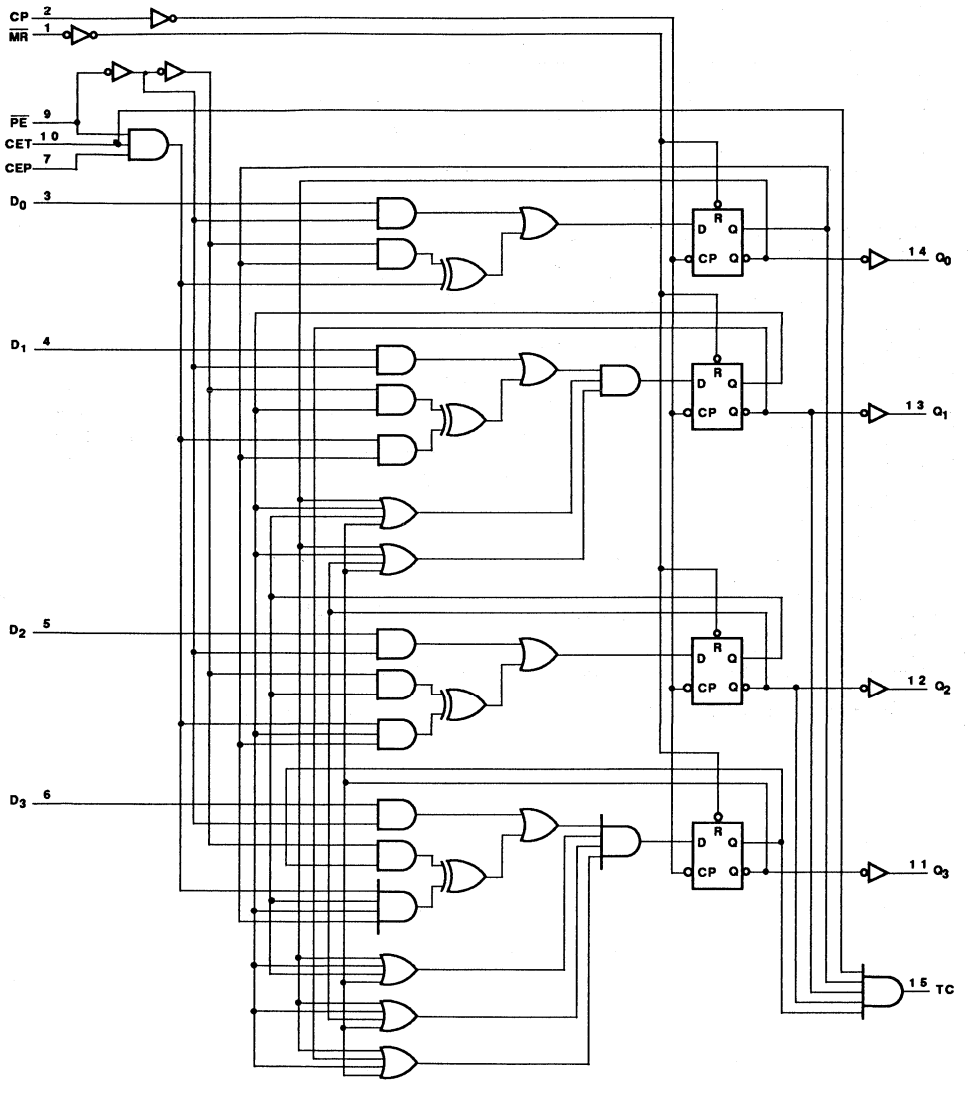
INPUTS						OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC	
L	X	X	X	X	X	L	L	Reset (clear)
H	↑	X	X	l	l	L	L	Parallel load
H	↑	X	X	l	h	H	(1)	
H	↑	h	h	h	X	count	(1)	Count
H	X	l	X	h	X	q_n	(1)	Hold (do nothing)
H	X	X	l	h	X	q_n	L	

MODE SELECT-FUNCTION TABLE for 'F162A, 'F163A

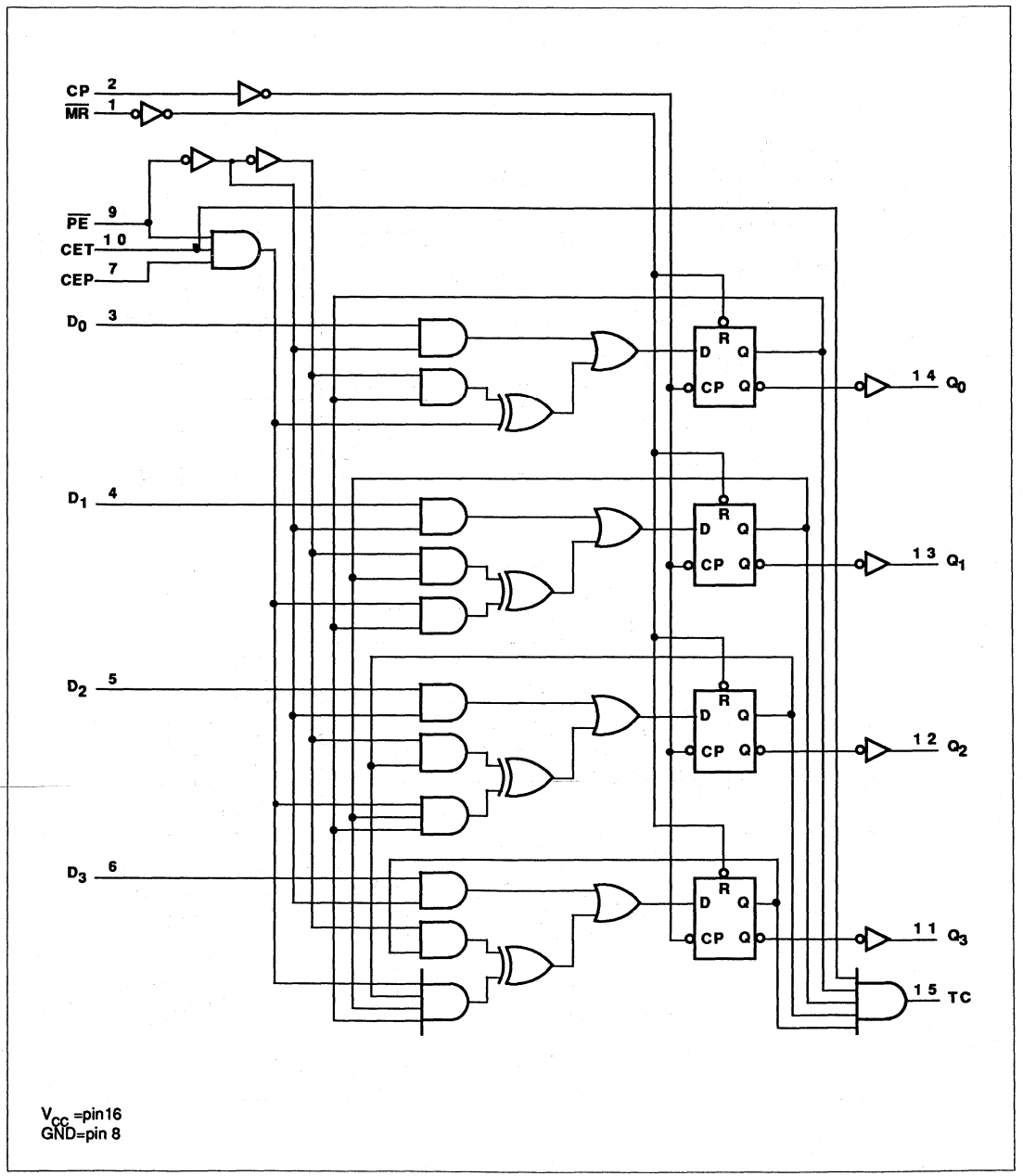
INPUTS						OUTPUTS		OPERATING MODE
$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC	
l	↑	X	X	X	X	L	L	Reset (clear)
h	↑	X	X	l	l	L	L	Parallel load
h	↑	X	X	l	h	H	(2)	
h	↑	h	h	h	X	count	(2)	Count
h	X	l	X	h	X	q_n	(2)	Hold (do nothing)
h	X	X	l	h	X	q_n	L	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(1) = The TC output is High when CET is High and the counter is at Terminal Count (HLLH for 'F160A and HHHH for 'F161A)
(2) = The TC output is High when CET is High and the counter is at Terminal Count (HLLH for 'F162A and HHHH for 'F163A)

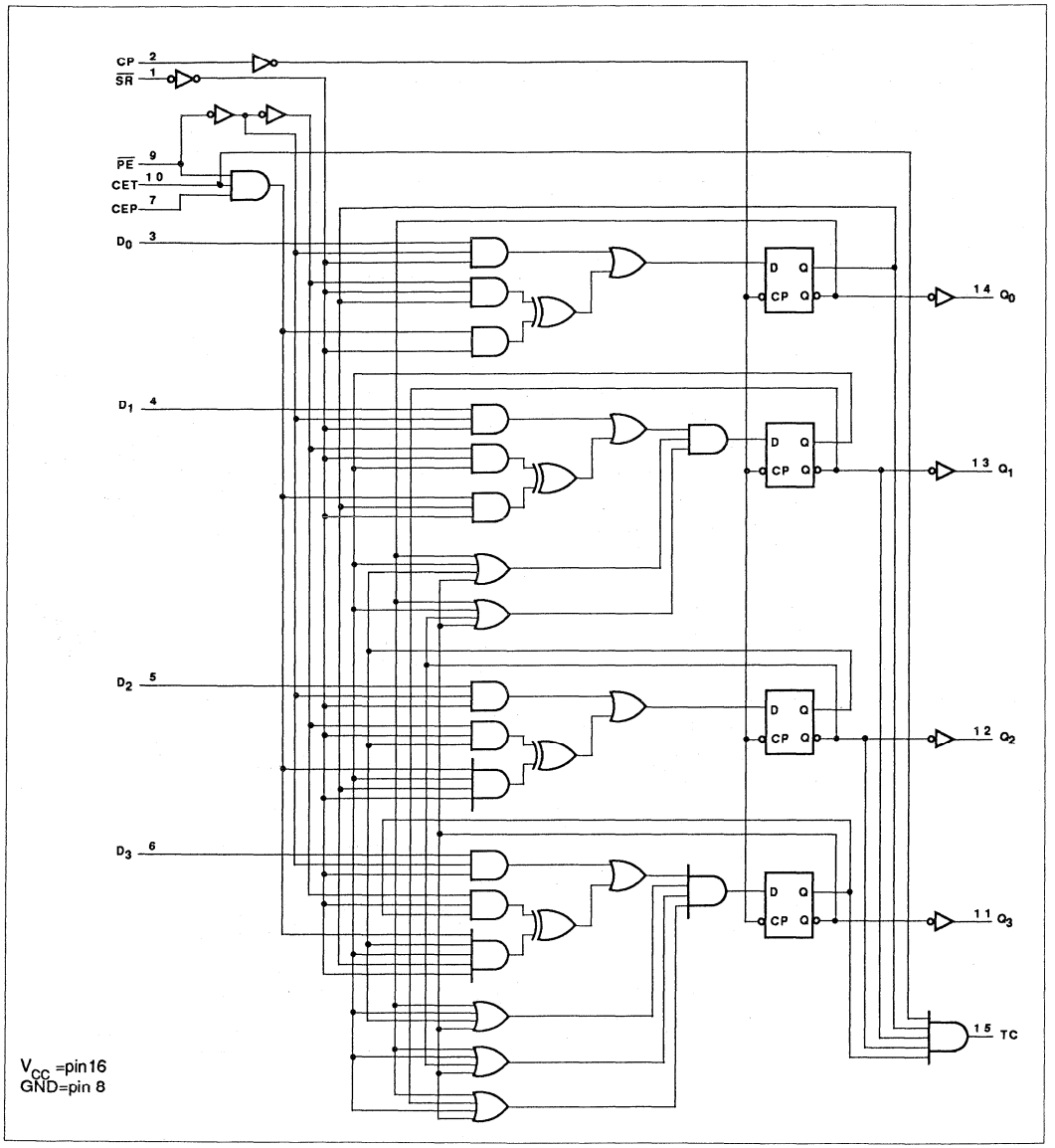
LOGIC DIAGRAM for 'F160A



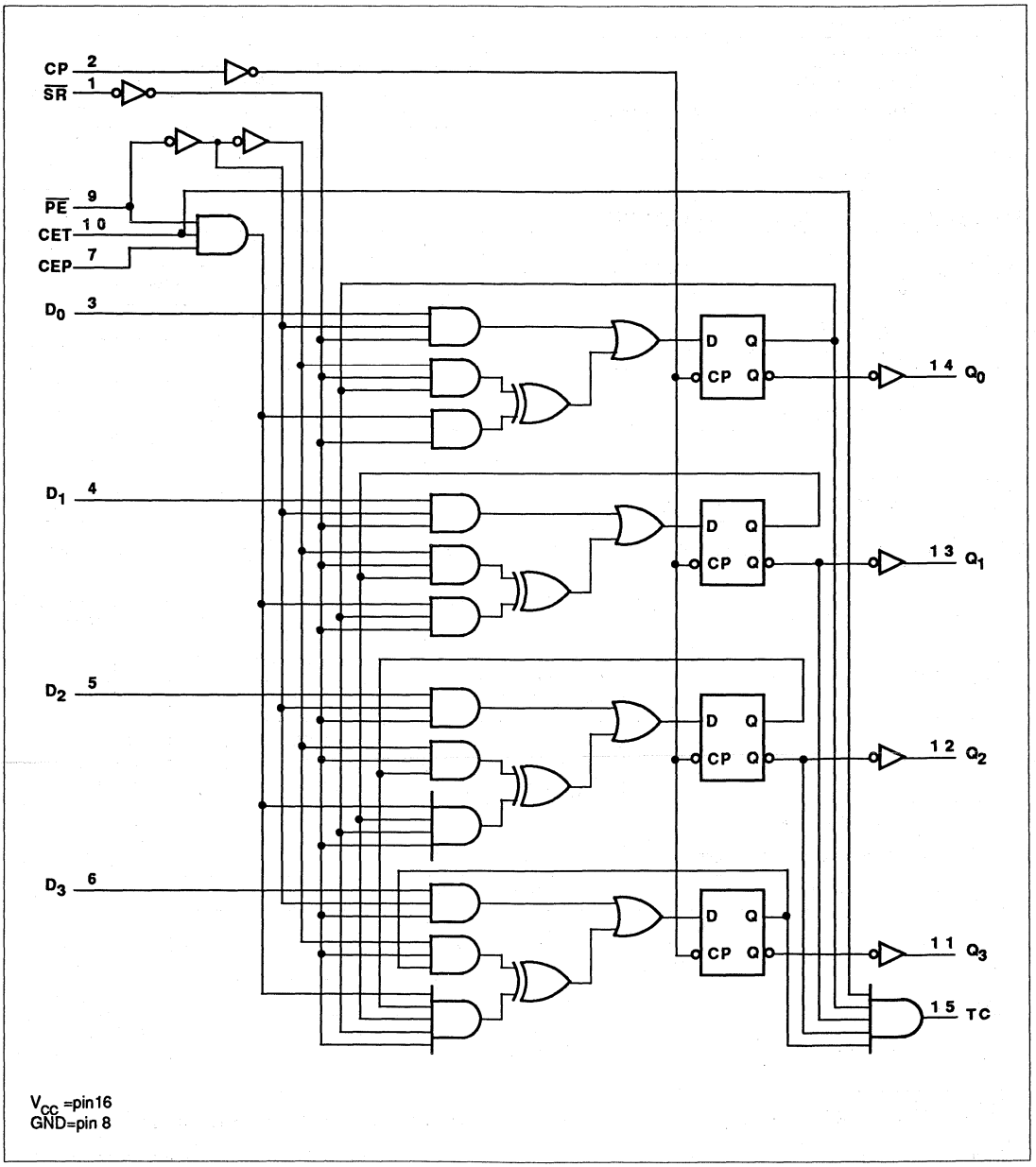
LOGIC DIAGRAM for 'F161A



LOGIC DIAGRAM for 'F162A



LOGIC DIAGRAM for 'F163A



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum Input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	CET, $\overline{PE}$	V_{CC} = MAX, V_I = 0.5V					-1.2	mA
		others						-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				42	55	mA
		I_{CCL}					49	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F160A and 74F162A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)		Waveform 1	2.0 4.0	4.5 7.0	7.0 10.0	2.0 4.0	8.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = Low)		Waveform 1	2.0 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	4.5 4.5	8.0 7.5	10.5 9.5	4.5 4.5	11.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	4.0 5.0	6.5 7.0	1.5 2.5	7.0 7.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	'F160A	Waveform 3	6.5	9.0	12.0	6.5	13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F160A	Waveform 3	6.0	8.0	10.0	5.5	11.0	ns

AC SETUP REQUIREMENTS for 74F160A and 74F162A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 6	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	11.0 7.0			11.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CET or CEP to CP		Waveform 4	11.0 6.0			11.0 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CET or CEP to CP		Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width (Load) High or Low		Waveform 1	4.0 5.0			4.0 6.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width (Count) High or Low		Waveform 1	4.0 5.5			4.0 6.5		ns
$t_w(L)$	$\overline{MR}$ pulse width Low	'F160A	Waveform 3	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	'F160A	Waveform 3	5.0			6.0		ns

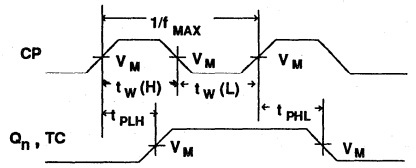
AC ELECTRICAL CHARACTERISTICS for 74F161A and 74F163A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)		Waveform 1	2.0 4.0	4.0 6.5	6.5 10.0	2.0 4.0	7.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = Low)		Waveform 1	2.0 3.5	4.5 5.5	6.5 8.5	2.0 3.5	7.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	5.0 4.5	7.5 7.5	10.5 10.5	5.0 4.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	3.5 5.0	6.5 7.5	1.5 2.5	7.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	'F161A	Waveform 3	6.0	8.5	12.0	5.5	13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F161A	Waveform 3	5.0	8.5	10.0	5.0	11.0	ns

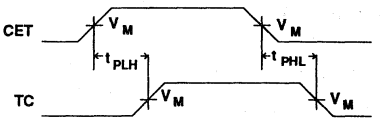
AC SETUP REQUIREMENTS for 74F161A and 74F163A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP		Waveform 6	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP		Waveform 6	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	9.0 6.5			9.5 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low CET or CEP to CP		Waveform 4	10.5 6.0			10.5 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low CET or CEP to CP		Waveform 4	0 0			0 0		ns
t_w(H) t_w(L)	CP pulse width (Load) High or Low		Waveform 1	4.0 5.0			4.0 5.5		ns
t_w(H) t_w(L)	CP pulse width (Count) High or Low		Waveform 1	4.0 6.0			4.0 7.0		ns
t_w(L)	$\overline{MR}$ pulse width Low	'F161A	Waveform 3	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	'F161A	Waveform 3	6.0			6.5		ns

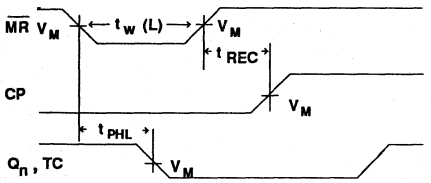
AC WAVEFORMS



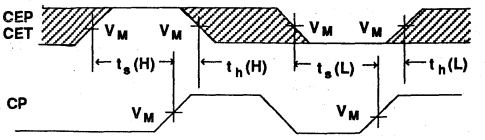
Waveform 1.
Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



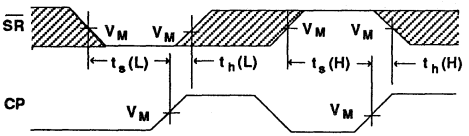
Waveform 2.
Propagation Delay, CET Input to TC Output



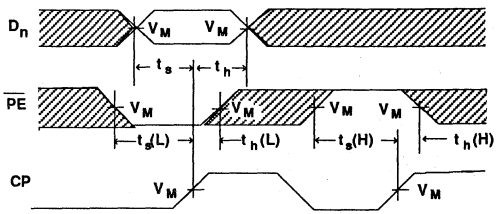
Waveform 3.
Master Reset pulse width, Master Reset to Output Delay and Master Reset to Recovery Time



Waveform 4.
CEP and CET Reset Setup and Hold Times



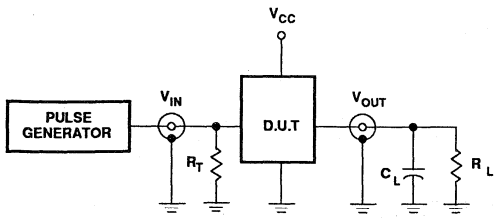
Waveform 5.
Synchronous Reset Setup and Hold Times



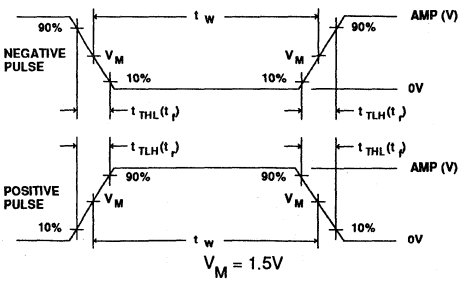
Waveform 6.
Parallel Data and Parallel Enable Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Register | FAST 74F164

8-bit serial-in parallel-out shift register

FEATURES

- Gated serial data inputs
- Typical shift frequency of 100MHz
- Asynchronous Master Reset
- Fully buffered clock and data inputs
- Fully synchronous data transfers

DESCRIPTION

The 74F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered through one of two inputs (D_{sa}, D_{sb}); either input can be used as an active High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two data inputs (D_{sa}, D_{sb}) that existed one setup time before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F164	100MHz	33mA

ORDERING INFORMATION

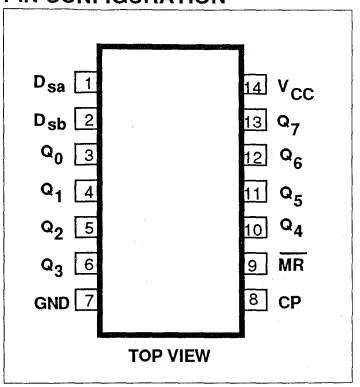
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C
14-pin Plastic DIP	N74F164N
14-pin Plastic SO	N74F164D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

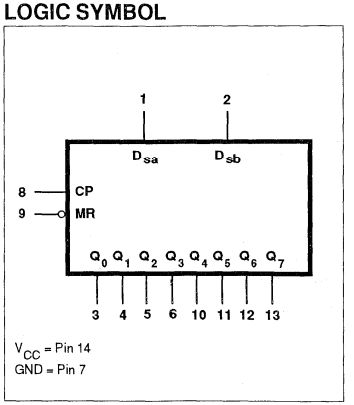
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{sa}, D_{sb}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

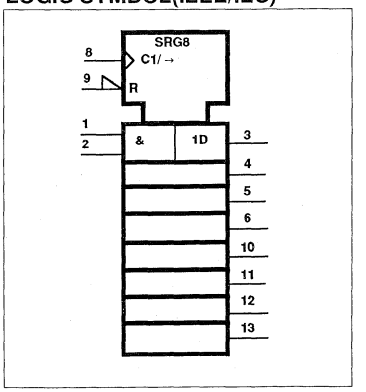
PIN CONFIGURATION



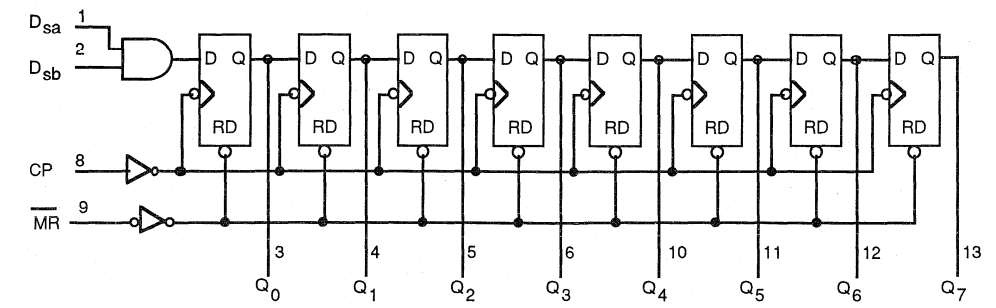
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

FUNCTION TABLE

INPUTS				OUTPUTS			OPERATING MODE
$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1 - - - - Q_7		
L	X	X	X	L	L	L	Reset (clear)
H	↑	l	l	L	q_0	q_6	Shift
H	↑	l	h	L	q_0	q_6	
H	↑	h	l	L	q_0	q_6	
H	↑	h	h	H	q_0	q_6	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

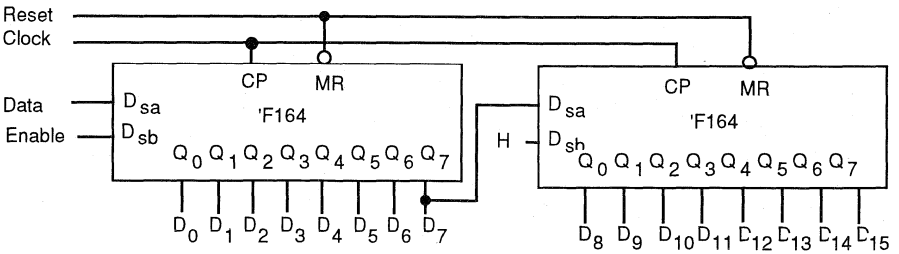
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuitoutput current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]	V_{CC} = MAX			33	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the serial inputs grounded , the clock input at 2.4 V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

APPLICATION



NOTE: The 'F164 can be cascaded to form synchronous shift registers of longer length. Here, two 'F164 are combined to form a 16 bit shift register.

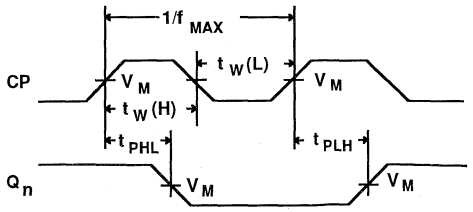
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 5.0	5.0 7.0	8.0 10.0	2.5 5.0	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.5	7.5	10.5	5.5	11.5	ns

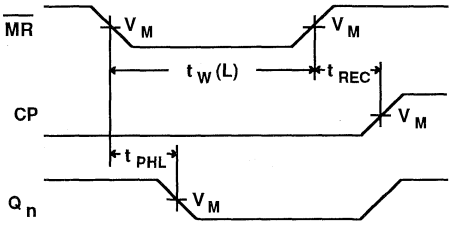
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 3	7.0 7.0			7.0 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 3	1.0 1.0			2.0 2.0		ns
t_w(H) t_w(L)	CP Pulse width High or Low	Waveform 1	4.0 7.0			4.0 7.0		ns
t_w(L)	$\overline{MR}$ Pulse width Low	Waveform 2	7.0			7.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			7.0		ns

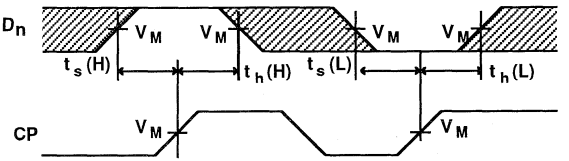
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

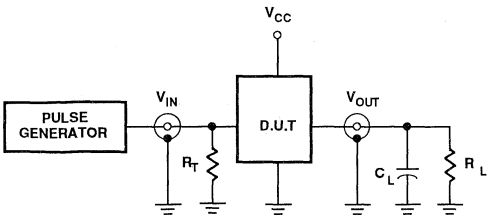


Waveform 3. Data Setup And Hold Times

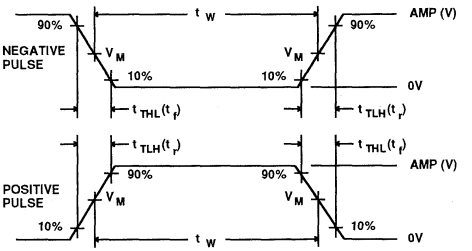
NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

8-Bit bidirectional universal shift register | 74F166

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in high and low states)
- Synchronous parallel to serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous master reset
- Expandable to 16 bits in 8–bit increments
- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F166	175MHz	50mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
16–pin plastic DIP	N74F166N	I74F166N
16–pin plastic SO	N74F166D	I74F166D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Parallel data inputs	1.0/0.033	20μA/20μA
Ds	Serial data input (shift right)	2.0/0.066	40μA/40μA
CP	Clock input (active rising edge)	1.0/0.033	20μA/20μA
$\overline{CE}$	Clock enable input (active low)	1.0/0.033	20μA/20μA
$\overline{PE}$	Parallel enable input (active low)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master reset input (active low)	2.0/0.066	40μA/40μA
Q7	Data output	50/33	1.0mA/20mA

Note to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

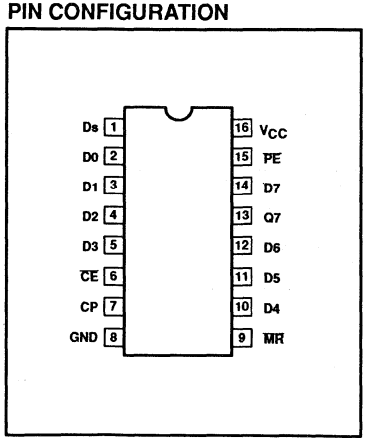
DESCRIPTION

The 74F166 is a high speed 8–bit shift register that has fully synchronous serial parallel data entry selected by an active low parallel enable ($\overline{PE}$) input. When the $\overline{PE}$ is low one setup time before the low–to–high clock transition, parallel data is entered into the register.

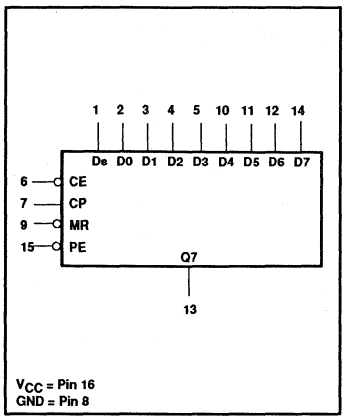
When $\overline{PE}$ is high, data is entered into internal bit position Q0 from serial data input (Ds), and the remaining bits are shifted one place to the right (Q0 → Q1 → Q2, etc.) with each positive going clock transition.

For expansion of the register in parallel to serial converters, the Q7 output is connected to the Ds input of the succeeding stage. The clock input is gated OR structure which allows one input to be used as an active–low clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The low–to–high transition of $\overline{CE}$ input should only take place while the CP is high for predictable operation. A low on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a low state.

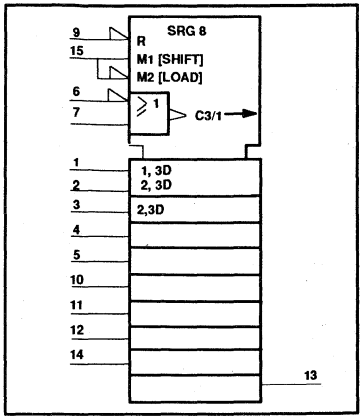
PIN CONFIGURATION



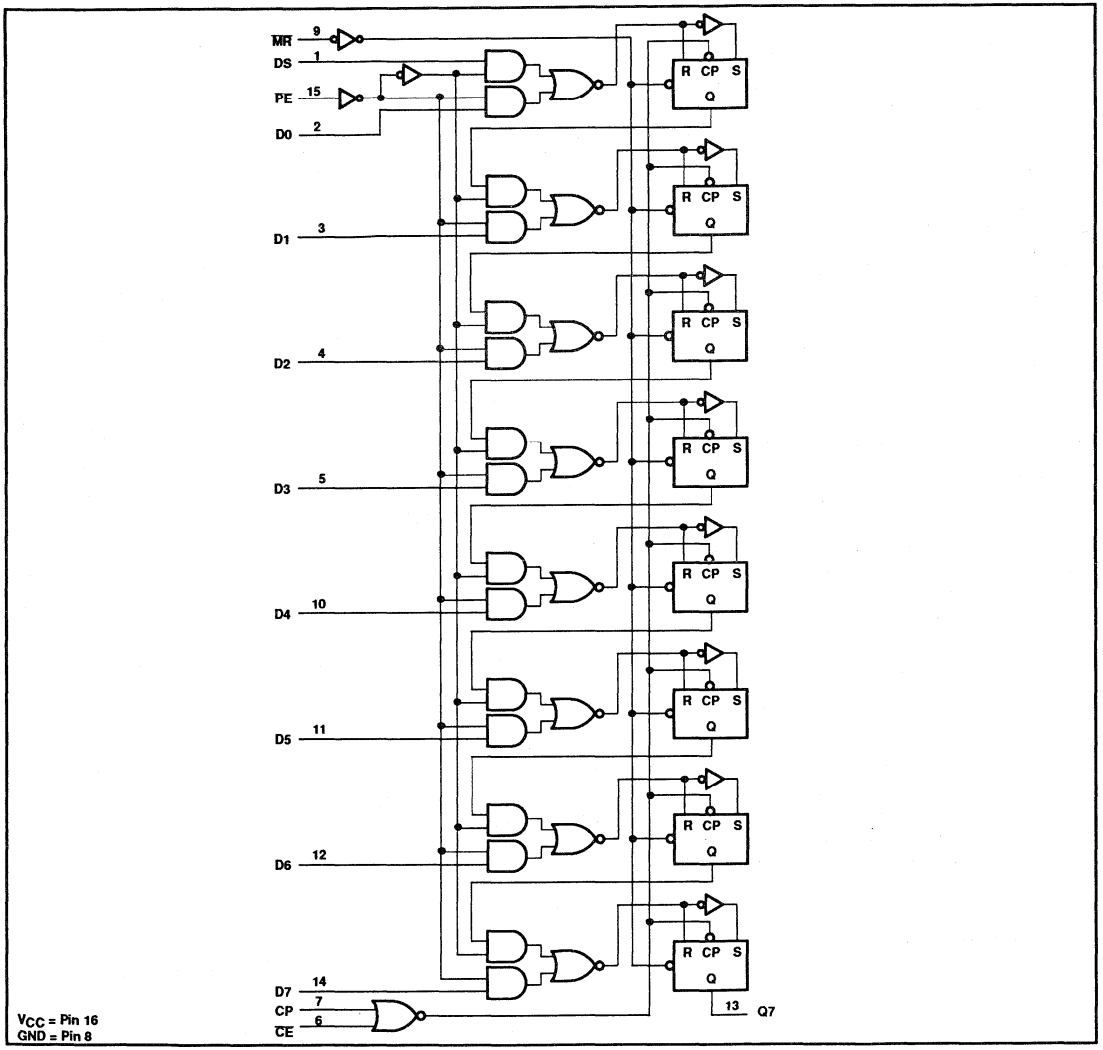
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					Qn REGISTER		OUTPUT	OPERATING MODE
$\overline{PE}$	$\overline{CE}$	CP	DS	D0 –D7	Q0	Q1 – Q6	Q7	
l	l	↑	X	l – l	L	L – L	L	Parallel load
l	l	↑	X	h – h	H	H – H	H	
h	l	↑	l	X – X	L	q0 – q5	q6	Serial shift
h	l	↑	h	X – X	H	q0 – q5	q6	
X	h	X	X	X – X	qn	q1 – q6	q7	Hold (do nothing)

Notes to function table
1. H = High–voltage level

2. h = High voltage level one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low voltage level one setup time before the low–to–high clock transition
5. qn = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the low–to–high clock transition
6. X = Don't care
7. ↑ = Low–to–high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		$\overline{CE}$, CP[3]							
I_{IH}	High–level input current	others	V_{CC} = MAX, V_I = 2.7V					20	µA
		$\overline{MR}$, Ds						40	µA
		Industrial only: others						40	µA
		Industrial only: $\overline{MR}$, Ds						80	µA
I_{IL}	Low–level input current	others	V_{CC} = MAX, V_I = 0.5V					-20	µA
		$\overline{MR}$, Ds						-40	µA
I_{OS}	Short–circuit output current[4]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{PE}$ = $\overline{CE}$ = Dn = GND, $\overline{MR}$ = Ds = 4.5V, CP = ↑				50	70	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. When testing CP, $\overline{CE}$ must remain in high state, whereas CP must remain in high state when testing $\overline{CE}$.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

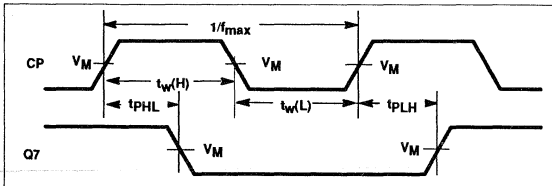
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			LIMITS: T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		LIMITS: T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	135	175		110		100		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q7	Waveform 1	5.0 4.0	7.5 6.0	10.0 8.0	5.0 3.5	12.0 9.0	5.0 3.5	13.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q7	Waveform 2	4.0	6.5	8.5	4.0	9.5	4.0	9.5	ns

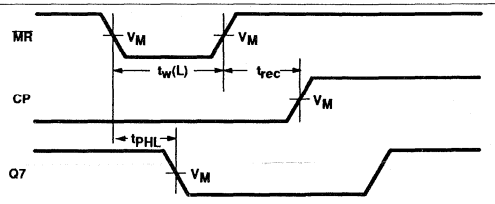
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Dn, Ds to CP, $\overline{CE}$	Waveform 3	3.0 2.5			4.0 3.0		4.0 3.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn, Ds to CP	Waveform 3	0.0 0.0			1.0 0.0		1.0 0.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn, Ds to $\overline{CE}$	Waveform 3	1.5 0.0			2.0 0.0		2.0 0.0		ns
t_{su}(L)	Setup time, low $\overline{CE}$ to CP	Waveform 3	5.0			6.0		6.0		ns
t_h (H)	Hold time, high $\overline{CE}$ to CP	Waveform 3	0.0			0.0		0.0		ns
t_{su} (H) t_{su}(L)	Setup time, high or low $\overline{PE}$ to CP, $\overline{CE}$	Waveform 3	3.0 3.0			4.0 4.0		4.0 6.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{PE}$ to CP	Waveform 3	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_w (H) t_w (L)	CP pulse width, high or low	Waveform 1	3.0 4.5			3.5 5.0		3.5 6.0		ns
t_w (L)	$\overline{MR}$ pulse width, low	Waveform 2	4.0			4.0		4.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.5		4.5		ns

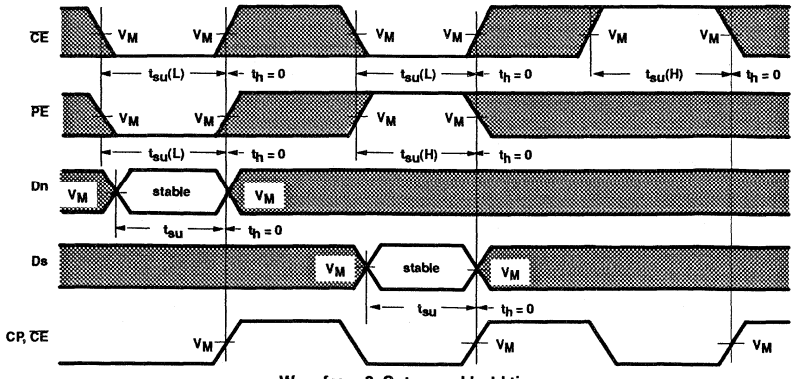
AC WAVEFORMS



Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time

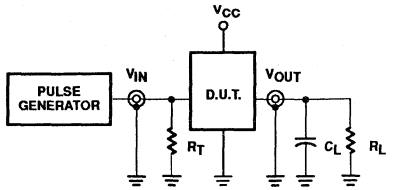


Waveform 3. Setup and hold times

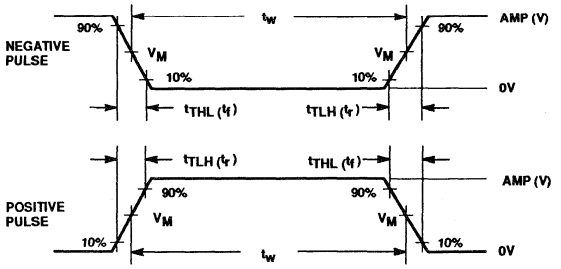
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0350
ECN No.	95942
Date of issue	March 3, 1989
Status	Product Specification
FAST Products	

FAST 74F168, 74F169 Counters

74F168 4-Bit Up/Down Decade Synchronous Counter
74F169 4-Bit Up/Down Binary Synchronous Counter

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F168	115MHz	35mA
74F169	115MHz	35mA

FEATURES

- **Synchronous counting and loading**
- **Up/down counting**
- **BCD decade counter- 'F168**
- **Modular 16 binary counter- 'F169**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Built-in lookahead carry capability**
- **Presettable for programmable operation**

DESCRIPTION

The 74F168 and 74F169 are 4-bit synchronous Up/Down Counters. The 74F168 is a synchronous, presettable BCD Decade Up/Down Counter featuring an internal carry look-ahead for applications in high speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the Low-to-High transition of the clock. The counter is fully programmable; that is, the outputs may be preset to either level.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F168N, N74F169N
16-Pin Plastic SO	N74F168D, N74F169D

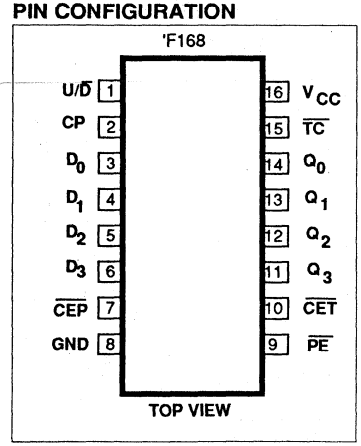
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
Q_0 -Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

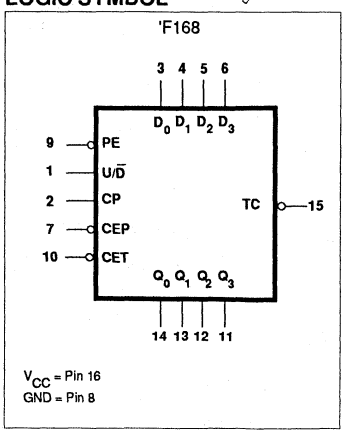
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A Low level on the Parallel Enable ($\overline{PE}$) input disables the counter

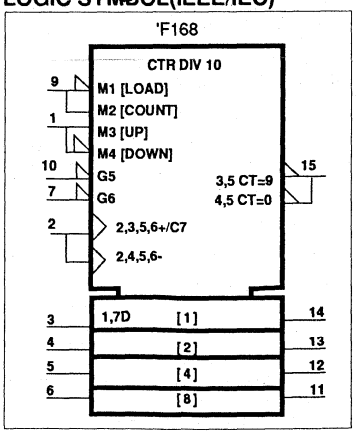
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

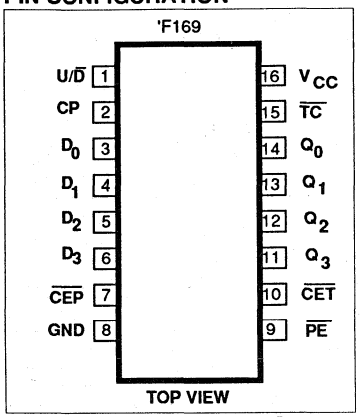


causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

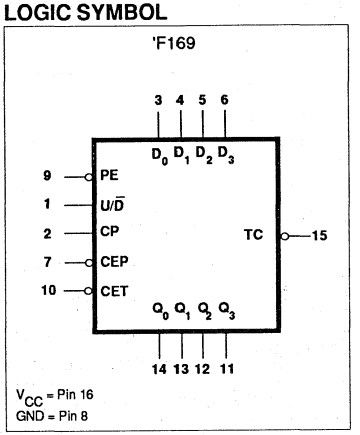
The direction of the counting is controlled by the by the Up/Down (U/$\overline{D}$) input; a High will cause the count to increase, a Low will cause the count to decrease.

The carry look ahead circuitry is provided for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enables($\overline{CEP}$, $\overline{CET}$) inputs and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be Low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal the High level portion of Q_0 output. The Low level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure 1 for the fast synchronous multistage counting connections. The 74F169 is identical except that it is a Modula 16 counter.

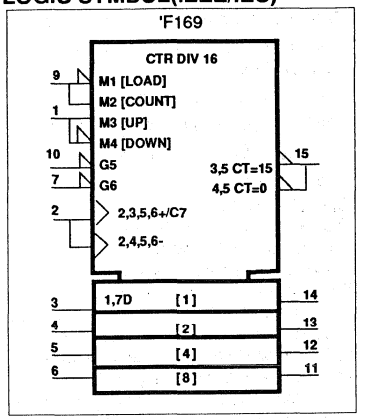
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTIONAL DESCRIPTION

The 'F168 and 'F169 use edge triggered J-K type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedance over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the D_0-D_3 inputs enter the flip-flops on the next rising edge of the clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the U/$\overline{D}$ input determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low, provided that $\overline{CET}$ is Low. When a counter reaches zero in the count down mode or reaches 9 (15 for 'F169) in the count up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'F168 decade counter can also be Low in the illegal states 11, 13, 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'F168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (See logic equations below).

1) Count Enable= $\overline{CEP}\cdot\overline{CET}\cdot\overline{PE}$
2) Up: $\overline{TC}=Q_0\cdot Q_3\cdot(U/\overline{D})\cdot\overline{CET}$
3) Down: $\overline{TC}=\overline{Q_0}\cdot\overline{Q_1}\cdot\overline{Q_2}\cdot\overline{Q_3}\cdot(U/\overline{D})\cdot\overline{CET}$

MODE SELECT-FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$	
↑	X	X	X	l	l	L	(1)	Parallel load (Dn → Qn)
↑	X	X	X	X	X	H	(1)	
↑	h	l	l	h	X	Count up	(1)	Count up (increment)
↑	l	l	l	h	X	Count down	(1)	Count down (decrement)
↑	X	h	X	h	X	q_n	(1)	Hold (do nothing)
↑	X	X	X	h	X	q_n	H	

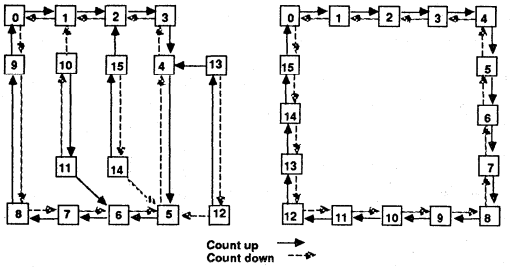
H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(1) = $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Ternminal Count.
The Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for 'F168.
The Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for 'F169.

MODE SELECT TABLE

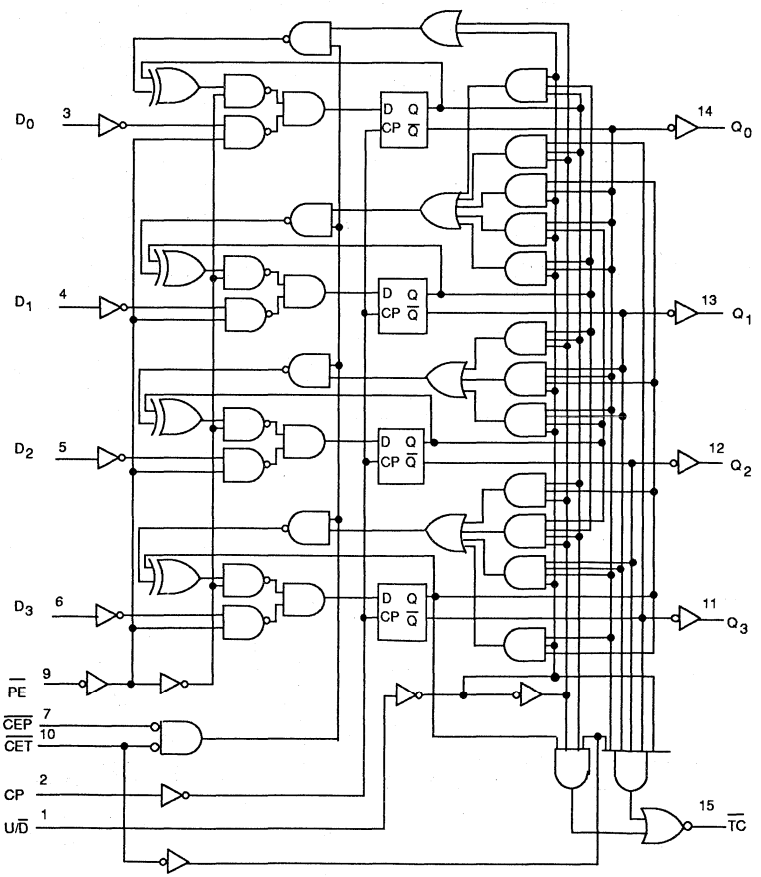
INPUTS				OPERATING MODE
$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	
L	X	X	X	Load (Dn → Qn)
H	L	L	H	Count up (increment)
H	L	L	L	Count down (decrement)
H	H	X	X	No change (Hold)
H	X	H	X	No change (Hold)

H = High voltage level
L = Low voltage level
X = Don't care

STATE DIAGRAM

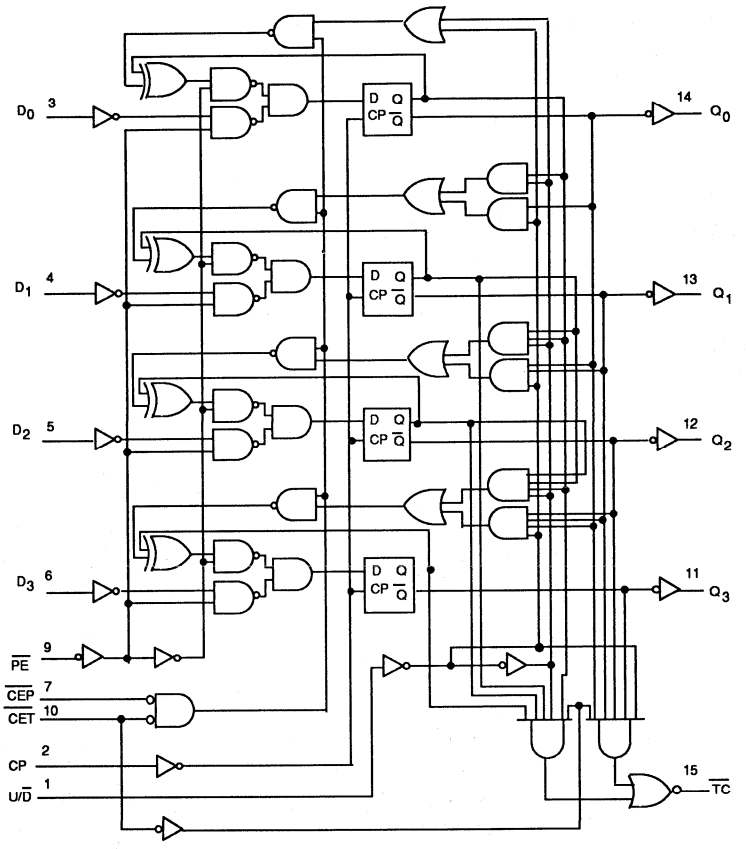


LOGIC DIAGRAM for'F168



V_{CC} =pin16
GND=pin 8

LOGIC DIAGRAM for 'F169



V_{CC} =pin16
GND=pin 8

APPLICATION

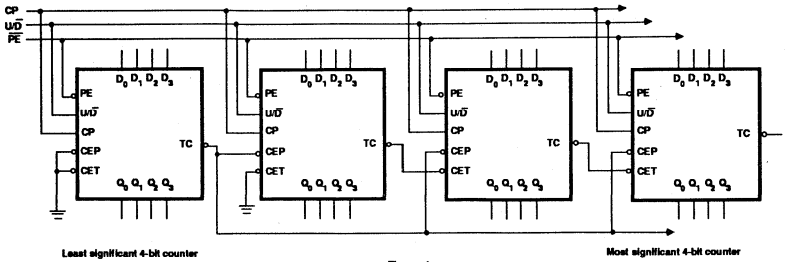


Figure 1
Synchronous multistage counting scheme

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{CET}$	V_{CC} = MAX, V_I = 0.5V				-1.2	mA
		others					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			35	52	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with after applying a momentary 4.5V, then ground to the clock input with all other inputs grounded and all outputs open.

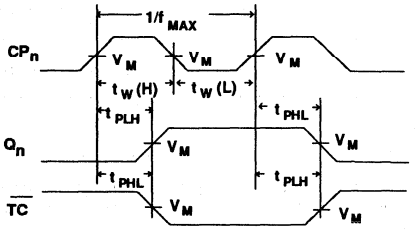
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, High or Low)		Waveform 1	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	9.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		Waveform 1	5.5 4.0	12.0 8.5	15.5 11.0	5.5 4.0	17.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$		Waveform 2	2.5 2.5	4.5 6.0	6.0 8.0	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F168	Waveform 3	3.5 4.0	8.5 12.5	11.0 16.0	3.5 4.0	12.5 17.5	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F169	Waveform 3	3.5 4.0	8.5 8.0	15.0 10.5	3.5 4.0	15.5 12.0	ns

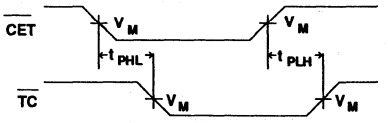
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 4	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 4	3.0 3.0			3.5 3.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 5	5.0 5.0			5.5 5.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP		Waveform 4	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP		Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F168	Waveform 6	11.0 16.5			12.5 18.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F169	Waveform 6	11.0 7.0			12.5 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP		Waveform 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP_U or CP_D Pulse width, High or Low		Waveform 1	5.0 5.0			5.5 5.5		ns

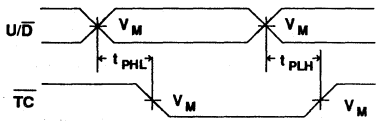
AC WAVEFORMS



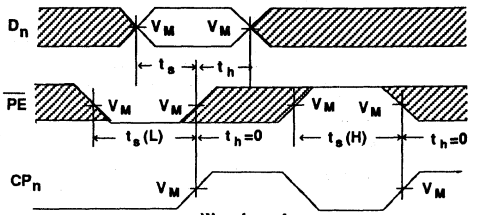
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



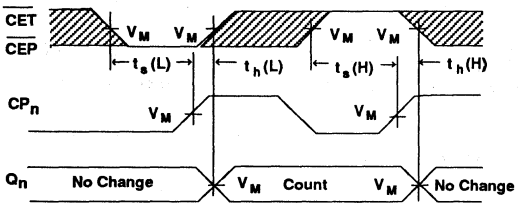
Waveform 2.
Propagation Delay, $\overline{CET}$ input to Terminal Count Output



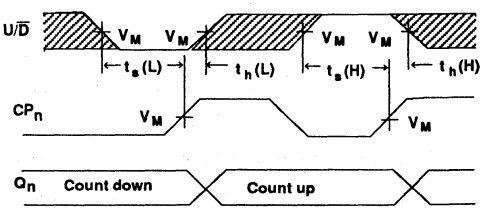
Waveform 3.
Propagation Delay, U/$\overline{D}$ input to Terminal Count Output



Waveform 4.
Data Parallel Data And Parallel Enable Setup And Hold Times



Waveform 5.
Count Enable Data Setup And Hold Times

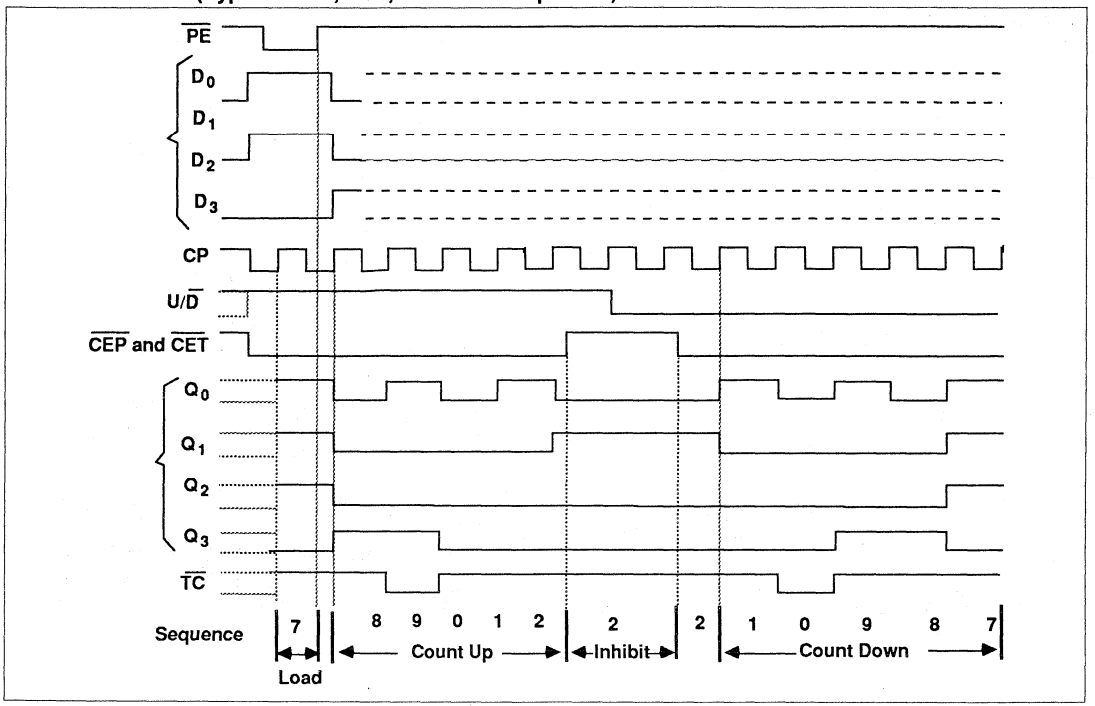


Waveform 6.
Up/Down Control Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

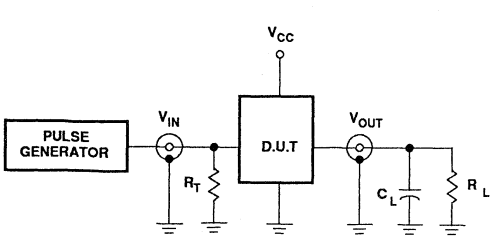
TIMING DIAGRAM (Typical clear, load, and count sequence) for 'F168



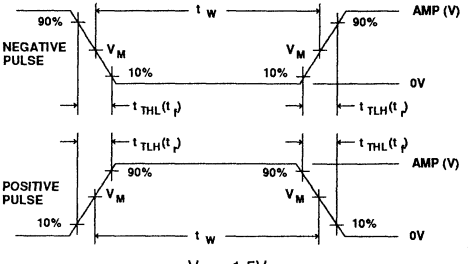
NOTES: Illustrated above is the sequence for the 'F168. The operation of the 'F169 is similar.

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum),zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine eightm and seven

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Quad D-type flip–flop (3-State) 74F173

FEATURES

- Edge–triggered D–type register
- Gated clock enable for hold "do nothing" mode
- 3–state output buffers
- Gated output enable control
- Speed upgrade of N8T10 and current sink upgrade
- Controlled output edges to minimize ground bounces
- 48mA sinking capability

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F173	125MHz	23mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16–pin plastic DIP	N74F173N
16–pin plastic SO	N74F173D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{E}$0, $\overline{E}$1	Clock enable inputs	1.0/1.0	20µA/0.6mA
MR	Master reset input	1.0/1.0	20µA/0.6mA
$\overline{OE}$0, $\overline{OE}$1	Output enable inputs	1.0/1.0	20µA/0.6mA
Q0 – Q3	Data outputs	750/80	15mA/48mA

Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

DESCRIPTION

The 74F173 is a high speed 4–bit parallel load registor with clock enable control, 3–state buffered outputs, and master reset (MR). When the two clock enable ($\overline{E}$0 and $\overline{E}$1) inputs are low, the data on the D inputs is loaded into the register simultaneously with low–to–high clock (CP) transition. When one or both enable inputs are high one setup time before the low–to–high clock transition, the register retains the previous data.

Data inputs and clock enable inputs are fully edge–triggered and must be stable only one setup time before the low–to–high clock transition.

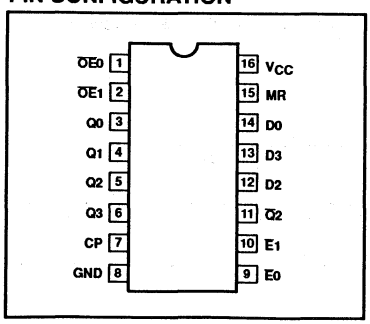
The master reset (MR) is an active–high asynchronous input. When the MR is high, all four flip–flops are reset (cleared) independently of any other input condition.

The 3–state output buffers are controlled by a 2–input NOR gate. When both output enable ($\overline{OE}$0 and $\overline{OE}$1) inputs are low, the data in the register is presented at the Q output.

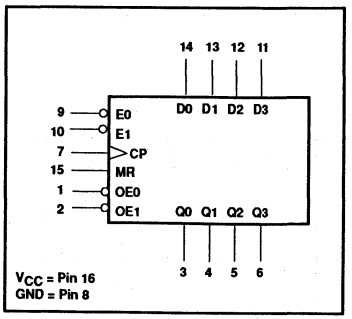
When one or both $\overline{OE}$ inputs are high, the outputs are forced to a high impedance "off" state.

The 3–state output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

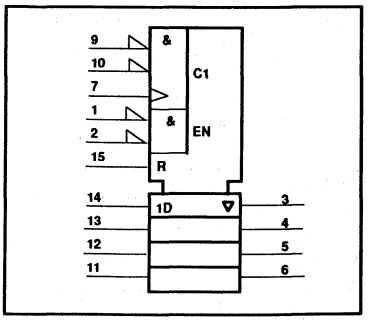
PIN CONFIGURATION



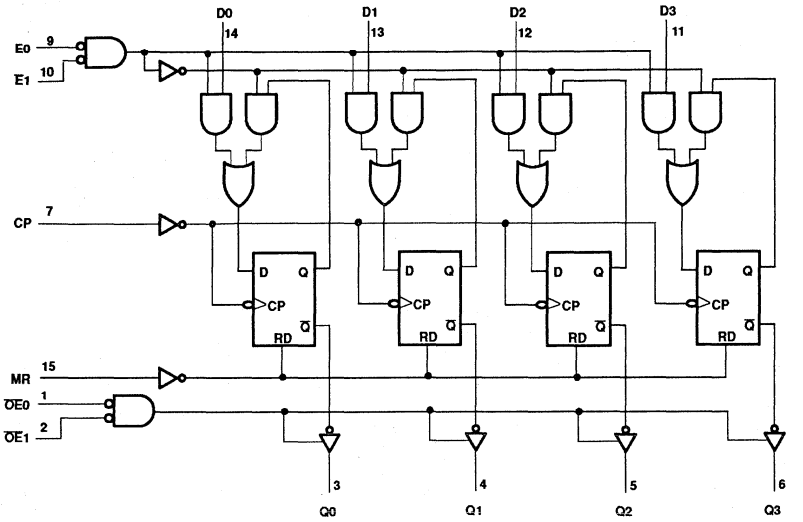
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS					OUTPUTS	OUTPUTS
MR	CP	$\overline{E0}$	$\overline{E1}$	Dn	Qn (register)	
H	X	X	X	X	L	Reset (clear)
L	↑	l	l	l	L	Parallel load
L	↑	l	l	h	H	
L	X	h	X	X	qn	Hold (do nothing)
L	X	X	h	X	qn	

Notes to function table
1. H = High–voltage level
2. h = High state one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low state one setup time before the low–to–high clock transition
5. qn = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the low–to–high clock transition
6. X = Don't care
7. ↑ = Low–to–high clock transition

FUNCTION TABLE

INPUTS			OUTPUTS	OUTPUTS
Qn (register)	$\overline{OE0}$	OE1	Qn	
L	L	L	L	Read
H	L	L	H	
X	H	X	Z	Disabled
X	X	H	Z	

Notes to function table
1. H = High–voltage level
2. L = Low–voltage level
3. X = Don't care
4. Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High–level output current			–15	mA
I_{OL}	Low–level output current			48	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.0			V
		V_{IH} = MIN, I_{OH} = –15mA	±5%V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off–state output current, high–level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off–state output current, low–level voltage applied	V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short–circuit output current3	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		19	26	mA
		I_{CCL}			27	37	mA
		I_{CCZ}			23	32	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

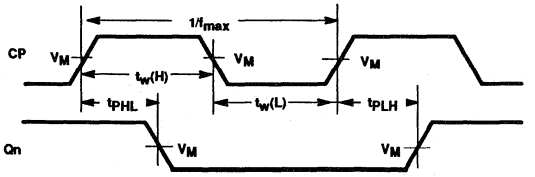
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	4.5 6.0	6.5 8.0	9.0 10.5	4.0 5.5	10.0 11.5	ns
t_{PHL}	Propagation delay MR to Qn	Waveform 2	6.5	8.5	11.5	6.0	12.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	Waveform 4 Waveform 5	3.5 5.5	5.0 7.0	8.0 10.0	2.5 4.5	8.5 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 4 Waveform 5	1.5 3.0	3.5 5.0	7.0 8.5	1.0 2.5	8.0 9.0	ns
t_{THL} t_{TLH}	Transition time 10% to 90%, 90% to 10%	Waveform 5 Waveform 4	2.0 4.0	5.0 7.5	8.0 10.0	2.0 4.0	8.5 11.0	ns

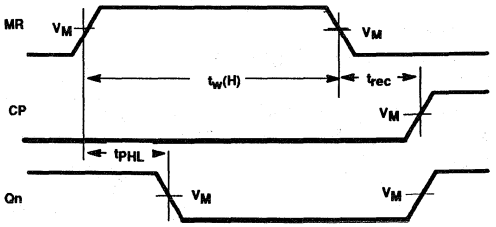
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to CP	Waveform 3	2.5 2.5			3.0 4.0		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to CP	Waveform 3	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low level $\overline{E}$ to CP	Waveform 3	4.5 7.5			5.0 8.5		ns
t_h (H) t_h (L)	Hold time, high or low level $\overline{E}$ to CP	Waveform 3	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	Waveform 1	3.0 6.0			3.0 6.0		ns
t_w (H)	MR Pulse width, high	Waveform 2	3.5			3.5		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	4.5			5.5		ns

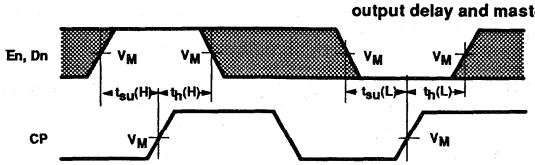
AC WAVEFORMS



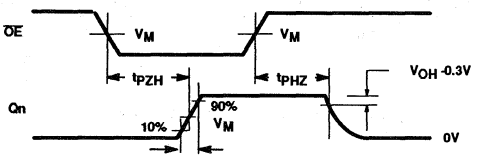
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



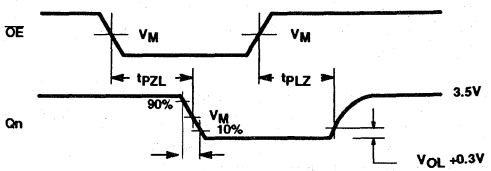
Waveform 2. Master reset pulse width, master reset to output delay and master resetf to clock recovery time



Waveform 3. Data and enable setup time and hold times



Waveform 4. 3-state output enable time to high level, output disable time from high level and transition time to high level



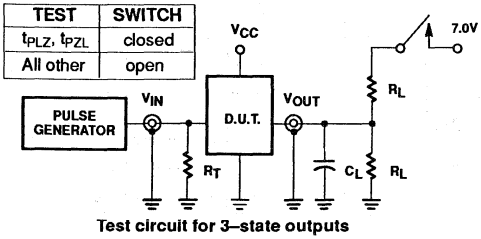
Waveform 5. 3-state output enable time to low level, output disable time from low level and transition time to low level

Notes to AC waveforms
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



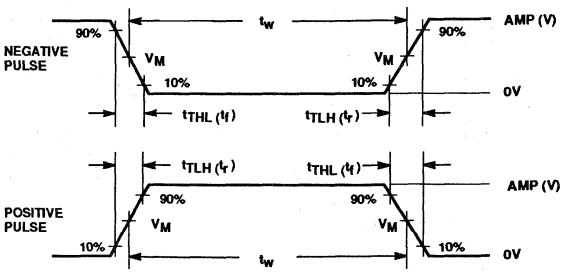
Test circuit for 3–state outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0060
ECN No.	94766
Date of issue	October 7, 1988
Status	Product Specification
FAST Products	

74F174
Flip-Flop

Hex D Flip-Flops

FEATURES

- **Six edge-triggered D-type flip-flops**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**

DESCRIPTION

The 74F174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where true outputs only are required, and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F174	100 MHz	35 mA

ORDERING INFORMATION

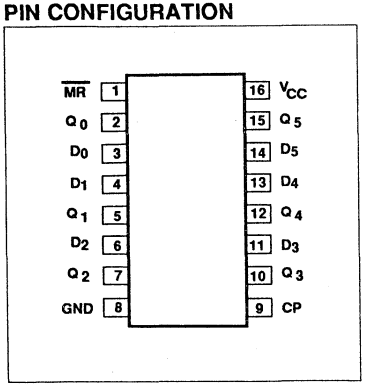
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F174N
16-Pin Plastic SO	N74F174D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

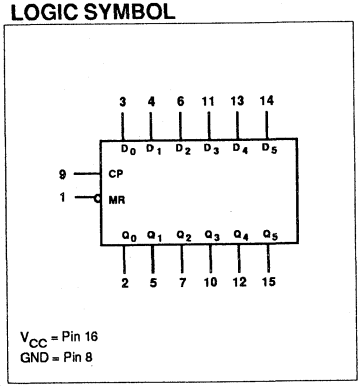
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_5	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.6mA
Q_0-Q_5	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

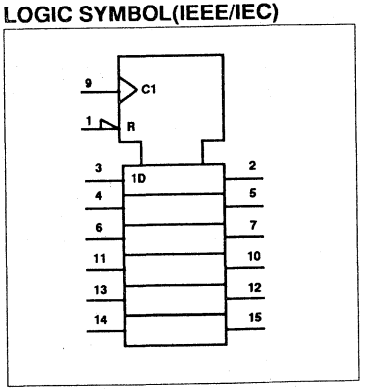
PIN CONFIGURATION



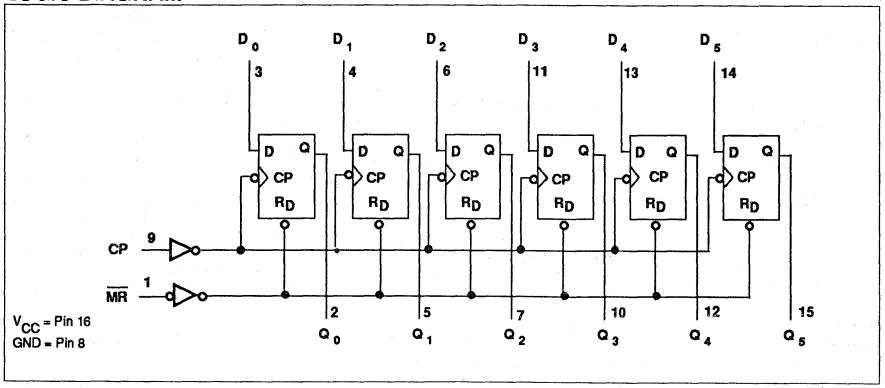
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	D	Q_n	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
L = Low voltage level
X = Don't care
↑= Low-to-High Clock transition
h =High voltage level one set-up time prior to the Low-to-High Clock transition.
l = Low voltage level one set-up time prior to the Low-to-High Clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, D_n=$\overline{MR}$=4.5V, CP=↑			35	45	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

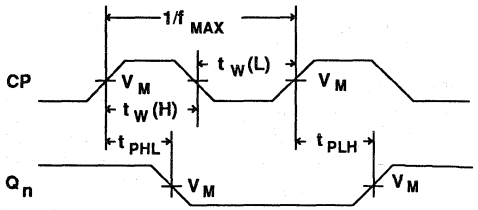
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.5 4.5	5.5 6.0	8.0 10.0	3.5 4.5	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.0	8.5	14.0	5.0	15.0	ns

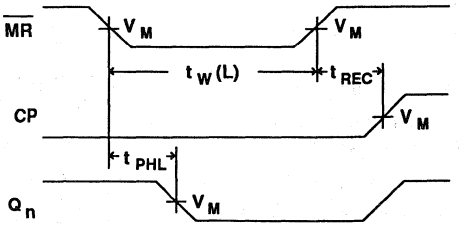
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 3	0 0			0 0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	5.0			5.0		ns

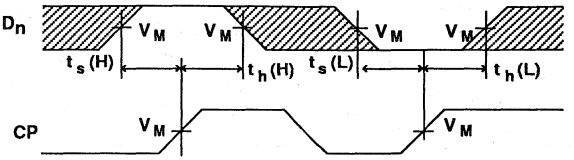
AC WAVEFORM



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



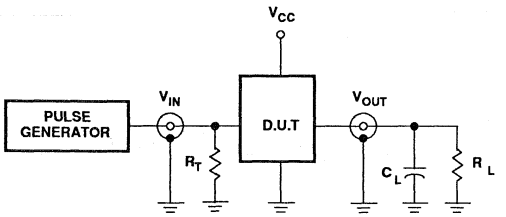
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



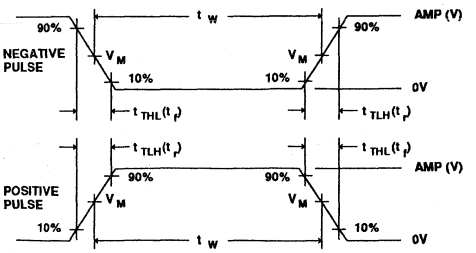
Waveform 3. Data Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Flip-flop

FAST 74F175/175A

Quad D flip-flop

FEATURES

- Four edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- True and complementary outputs
- Industrial temperature range available (-40°C to +85°C)
- PNP light loading inputs ('F175A)
- Improved AC, DC, and functional ('F175A)

DESCRIPTION

The 74F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. All Q outputs will be forced Low independently of clock or data inputs by Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complementary outputs are required and the CP and $\overline{MR}$ are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F175	140MHz	25mA
74F175A	160MHz	22mA

ORDERING INFORMATION

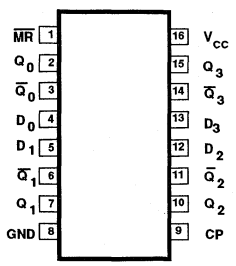
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10%, T_{amb} = -40°C to +85°C
16-pin plastic DIP	N74F175N	IN74F175N
16-pin plastic SO	N74F175D	IN74F175D
16-pin plastic DIP	N74F175AN	IN74F175AN
16-pin plastic SO	N74F175AD	IN74F175AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

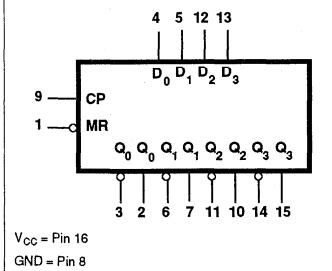
PINS	DESCRIPTION		74F(U.L) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	'F175	1.0/1.0	20µA/0.6mA
		'F175A	1.0/0.033	20µA/20µA
$\overline{MR}$	Master Reset input (active Low)	'F175	1.0/1.0	20µA/0.6mA
		'F175A	1.0/0.033	20µA/20µA
CP	Clock Pulse input (active rising edge)	'F175	1.0/1.0	20µA/0.6mA
		'F175A	1.0/0.033	20µA/20µA
Q_0 - Q_3	True outputs		50/33	1.0mA/20mA
$\overline{Q}_0$ - $\overline{Q}_3$	Complementary outputs		50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

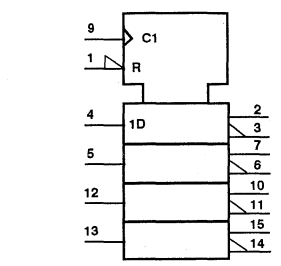
PIN CONFIGURATION



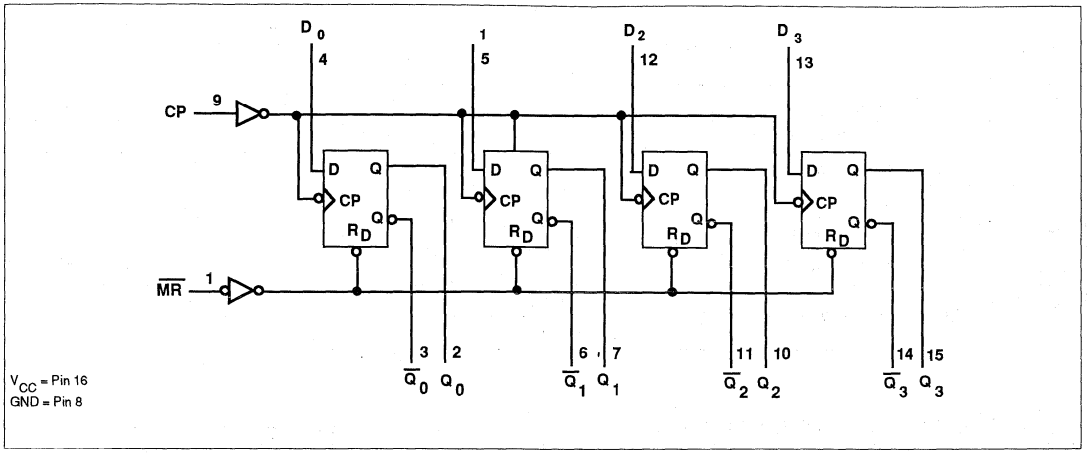
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
MR	CP	D	Q_n	$\overline{Q}_n$	
L	X	X	L	H	Reset (clear)
H	↑	h	H	L	Load "1"
H	↑	l	L	H	Load "0"

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	-40		85	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS [1]		LIMITS			UNIT
				Min	Typ [2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} =MIN, I_{OH} =MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} =MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.5	V
			±5%V_{CC}		0.30	0.5	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	'F175			-0.6	µA
			'F175A			-20	
I_{OS}	Short-circuit output current [3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	'F175		25	34	mA
			'F175A		22	31	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F175

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_{amb} = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	140		100		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$		4.0 4.0	5.0 6.5	6.5 8.5	4.0 4.0	7.5 9.5	3.5 4.0	8.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	4.5	9.0	11.5	4.5	13.0	4.5	13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 3	4.0	6.5	8.0	4.0	9.0	4.0	11.0	ns

AC ELECTRICAL CHARACTERISTICS FOR 74F175A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_{amb} = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	140	160		125		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.0 4.5	4.0 6.0	6.5 8.5	2.5 4.0	7.5 9.0	2.5 4.0	8.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	4.5	6.5	9.0	4.5	10.0	4.5	11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 3	4.5	6.0	8.0	4.0	9.0	4.0	10.0	ns

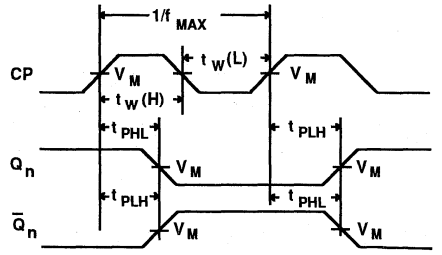
AC SETUP REQUIREMENTS FOR 74F175

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_{amb} = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		3.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	4.0 5.0			4.0 5.0		4.0 6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 3	5.0			5.0		5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		6.0		ns

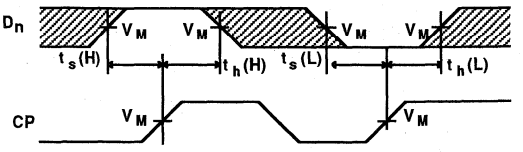
AC SETUP REQUIREMENTS FOR 74F175A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_{amb} = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	3.0 3.0			3.5 3.5		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	0.0 0.0			0.0 0.0		0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	3.0 4.0			3.5 5.0		4.0 5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 3	3.5			3.5		4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 3	4.0			4.5		5.0		ns

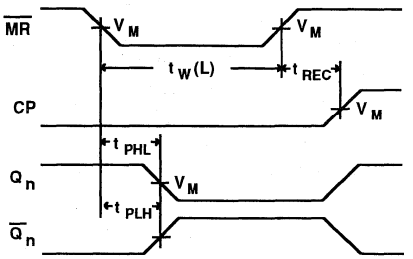
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



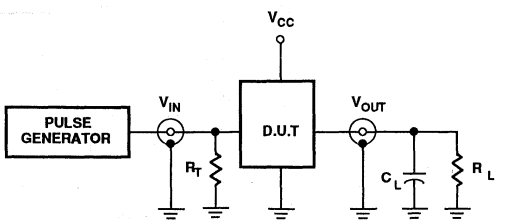
Waveform 2. Data Setup And Hold Times



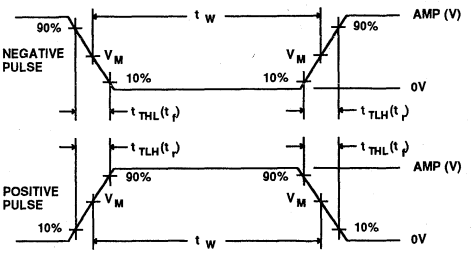
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0351
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Date of issue	August 8, 1989
Status	Product Specification
FAST Products	

FAST 74F181
Arithmetic Logic Unit

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F181	7.0 ns	43mA

FEATURES

- **Provides 16 arithmetic operations: add, subtract, compare, and double; plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables:Exclusive-OR, Compare, AND, NAND, NOR, OR plus 10 other logic operations**
- **Full look-ahead carry for high speed arithmetic operation on long words**
- **40% faster than 'S181 with only 30% 'S181 power consumption**
- **Available in 300 mil-wide Slim 24 pin Dip package**

DESCRIPTION

The 74F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0-S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-High or active-Low operands. The Function Table lists these operations.

ORDERING INFORMATION

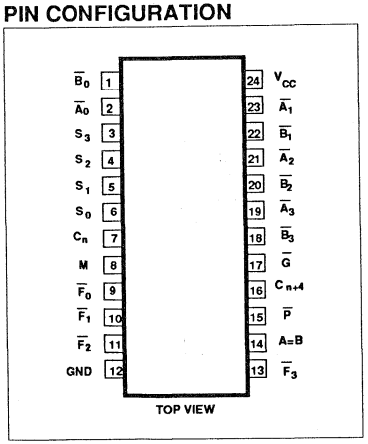
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F181N
24-Pin Plastic SOL	N74F181D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

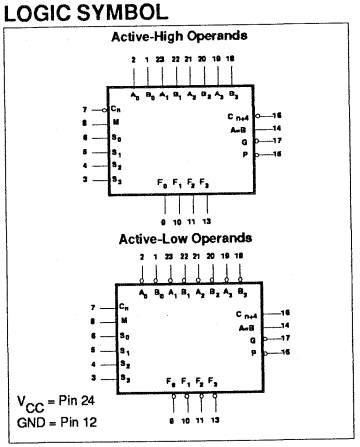
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{A}_0$-$\overline{A}_3$	A operand inputs	1.0/3.0	20µA/1.8mA
$\overline{B}_0$-$\overline{B}_3$	B operand inputs	1.0/3.0	20µA/1.8mA
M	Mode control input	1.0/1.0	20µA/0.6mA
S_0-S_3	Function select input	1.0/4.0	20µA/2.4mA
C_n	Carry input	1.0/5.0	20µA/3.0mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
$\overline{P}$	Carry Propagate output	50/33	1.0mA/20mA
$\overline{G}$	Carry Generate output	50/33	1.0mA/20mA
A=B	Compare output	OC/33	OC/20mA
$\overline{F}_0$-$\overline{F}_3$	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

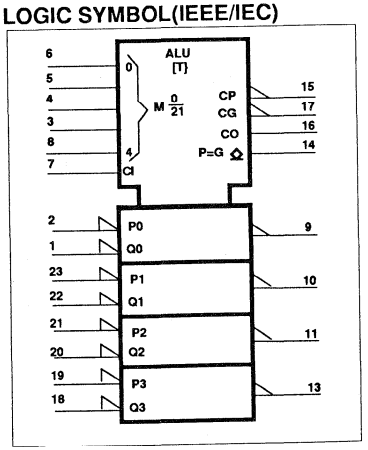
PIN CONFIGURATION



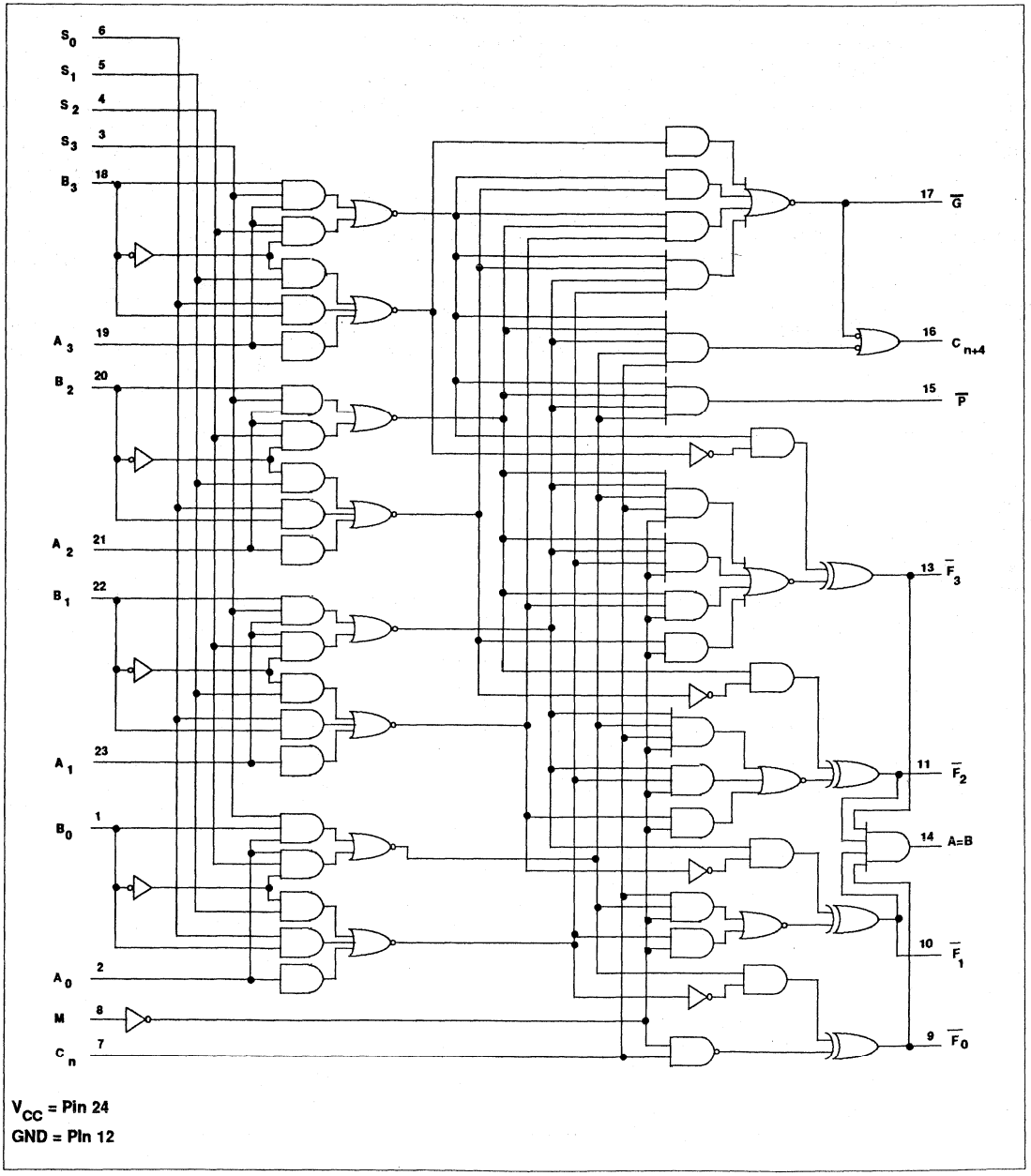
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

When the Mode Control input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry look-ahead and provides for either ripple carry between device using the C_{n+4} output, or for carry look-ahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input(C_n) of the next unit. For high-speed operation the device is used in conjunction with the 'F182 carry look-ahead circuit. One carry look-ahead package is required for each group of four 'F181 devices. Carry look-ahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A=B output from the device goes High when all four F outputs are High and can be used to indicate logic equivalence over 4-bits when the unit is in the subtract mode. The A=B output is open-collector and can be wired-AND with other A=B outputs to give a comparison for more than 4 bits. The A=B signal can also be used with the C_{n+4} signal to indicate A>B and A<B. The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus select code LHHL generates A minus B minus 1 (two's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (one's complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active-Low inputs producing active-Low outputs or with active-High inputs producing active High outputs. For either case, the table lists the operations that are performed to the operands labled inside the logic symbol.

MODE-SELECT FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS		ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M=H)	Arithmetic** (M=L) (C_n=H)	Logic (M=H)	Arithmetic** (M=L) (C_n=L)
L	L	L	L	$\overline{A}$	A	$\overline{A}$	A minus 1
L	L	L	H	$\overline{A+B}$	A+B	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}B$	$A+\overline{B}$	$\overline{A}+B$	$A\overline{B}$ minus 1
L	L	H	H	Logical 0	minus 1	Logical 1	minus 1
L	H	L	L	$\overline{AB}$	A plus $A\overline{B}$	$\overline{A+B}$	A plus $(A+\overline{B})$
L	H	L	H	$\overline{B}$	$(A+B)$ plus $A\overline{B}$	$\overline{B}$	AB plus $(A+\overline{B})$
L	H	H	L	$A \oplus B$	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	$A\overline{B}$	AB minus 1	$A+\overline{B}$	$A + \overline{B}$
H	L	L	L	$\overline{A}+B$	A plus AB	$\overline{A}B$	A plus (A+B)
H	L	L	H	$\overline{A \oplus B}$	A plus B	$A \oplus B$	A plus B
H	L	H	L	B	$(A+\overline{B})$ plus AB	B	$A\overline{B}$ plus (A+B)
H	L	H	H	AB	AB minus 1	A+ B	A+B
H	H	L	L	Logical 1	A plus A*	Logical 0	A plus A*
H	H	L	H	$A+\overline{B}$	(A+B) plus A	$A\overline{B}$	AB plus A
H	H	H	L	A+B	$(A+\overline{B})$ plus A	AB	$A\overline{B}$ plus A
H	H	H	H	A	A minus 1	A	A

H = High voltage level
L = Low voltage level
* = Each bit is shifted to the next more significant position.
** = Arithmetic operations expressed in two's complement notation.

SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0=S_3=4.5V$, $S_1=S_2=M=0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$,C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$,C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$,C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$,C_n	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$,C_n	C_{n+4}
t_{PLH}, t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1=S_2=4.5V$, $S_0=S_3=M=0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$,C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$,C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$, $\overline{B}$,C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$,C_n	A=B
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$,C_n	A=B
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$,C_n	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$,C_n	C_{n+4}
t_{PLH}, t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE III

FUNCTION INPUTS: $S_1=S_2=M=4.5V$, $S_0=S_3=0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$,C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$,C_n	$\overline{F}_i$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_K	Input clamp current				-18	mA
V_{OH}	High level output voltage	A=B only			4.5	V
I_{OH}	High-level output current	Any output except A=B			-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	A=B only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Any output except A=B	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	M	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{A}_0$-$\overline{A}_3$, $\overline{B}_0$-$\overline{B}_3$						-1.8	mA
		S_0-S_3						-2.4	mA
		C_n						-3.0	mA
I_{OS}	Short-circuit output current[3]	Any output except A=B	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	S_0-S_3=M=$\overline{A}_0$-$\overline{A}_3$=4.5V, $\overline{B}_0$-$\overline{B}_3$=C_n=GND			43	65	mA
		I_{CCL}		S_0-S_3=M=4.5V, $\overline{B}_0$-$\overline{B}_3$=C_n=$\overline{A}_0$-$\overline{A}_3$=GND			43	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

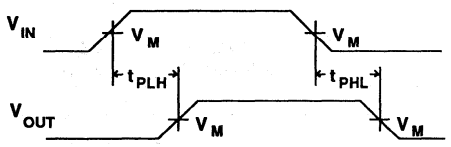
SYMBOL	PARAMETER	TEST CONDITIONS				LIMITS					UNIT
						T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
		Mode	Table	Wave form	Condition	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Sum Diff	I II	1	M=0V	3.0 2.5	5.0 5.0	8.0 8.0	3.0 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Sum	I	2	M=S_1=S_2=0V, S_0=S_3=4.5V	5.0 5.0	9.0 8.0	12.0 12.0	5.0 5.0	13.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Diff	II	2	M=S_0=S_3=0V, S_1=S_2=4.5V	5.0 5.0	9.5 8.0	13.0 12.0	5.0 5.0	14.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	Diff Sum	II I	1	M=0V	3.0 3.0	5.0 5.0	8.0 8.0	3.0 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Sum	I	1	M=S_1=S_2=0V, S_0=S_3=4.5V	3.0 3.0	5.0 5.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Diff	II	2	M=S_0=S_3=0V, S_1=S_2=4.5V	3.0 3.0	4.5 5.0	8.0 8.5	2.5 2.5	9.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Sum	I	2	M=S_1=S_2=0V, S_0=S_3=4.5V	2.5 3.0	4.0 4.5	7.0 7.5	2.0 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Diff	II	1, 2	M=S_0=S_3=0V, S_1=S_2=4.5V	2.5 3.0	4.0 5.0	7.5 8.5	2.0 2.5	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	I	1, 2	M=S_1=S_2=0V, S_0=S_3=4.5V	3.0 3.0	4.5 4.5	7.5 7.5	2.5 3.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Diff	II	1, 2	M=S_0=S_3=0V, S_1=S_2=4.5V	3.0 3.0	4.5 5.0	8.5 8.5	2.5 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to F_n	Sum		1, 2		3.5 3.5	6.0 5.5	10.0 9.5	3.0 3.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to F_n	Diff		1, 2		4.0 4.5	6.5 7.0	10.5 10.5	3.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Logic	III	1, 2	M=4.5V	3.5 3.5	5.5 5.5	9.0 10.0	3.0 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to A=B	Diff	II	1, 2	M=S_0=S_3=0V, S_1=S_2=4.5V	10.0 6.0	14.0 8.5	19.0 12.5	9.5 5.5	20.5 12.5	ns

NOTE: "$\overline{A}_n$ or $\overline{B}_n$ to F_n" means any $\overline{A}$ or any $\overline{B}$ to any $\overline{F}$ and "$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$" means $\overline{A}_1$, $\overline{B}_1$ to $\overline{F}_1$; $\overline{A}_2$, $\overline{B}_2$ to $\overline{F}_2$ (the subscripts must be the same).

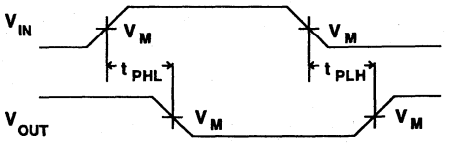
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
		Mode	Waveform	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{F}_i$ (Inv)		1	3.5 3.5	5.5 5.0	8.0 8.0	3.0 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{F}_i$ (Non-Inv)		2	3.0 3.0	5.5 5.5	8.5 8.5	3.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to A=B (Inv)		1	10.5 6.0	16.5 8.0	22.5 11.0	10.5 6.0	24.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to A=B (Non-Inv)		2	10.0 5.5	15.0 8.5	19.0 12.5	10.0 5.0	21.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to C_{n+4} (Inv)		1	3.5 3.0	7.0 5.5	11.0 10.0	3.0 2.5	12.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{G}$ (Non-Inv)		2	2.5 2.5	5.0 4.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{P}$ (Non-Inv)		2	2.5 2.5	4.0 4.5	6.5 7.0	2.5 2.5	7.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Inv)	Sum	1	3.5 3.5	6.0 6.0	8.5 8.5	3.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Non-Inv)	Sum	2	4.5 4.0	7.0 6.0	10.0 9.5	4.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Inv)	DIff	1	3.5 3.5	6.0 6.0	8.5 8.5	3.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Non-Inv)	Diff	2	4.0 4.0	7.0 6.0	10.0 9.5	4.0 4.0	11.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Inv)	Sum	1	12.0 6.5	16.0 8.0	20.0 11.0	11.0 6.0	22.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Non-Inv)	Sum	2	13.0 6.5	17.0 8.0	21.0 10.5	12.0 6.0	24.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Inv)	Diff	1	11.5 6.0	16.0 8.0	20.0 10.5	10.5 6.0	22.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Non-Inv)	Diff	2	13.0 6.0	17.0 8.0	21.5 11.0	12.5 6.0	24.0 11.5	ns

AC WAVEFORMS



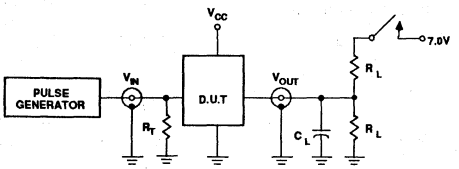
Waveform 1. Propagation Delay for Non-Inverting paths



Waveform 2. Propagation Delay for Inverting paths

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs

SWITCH POSITION

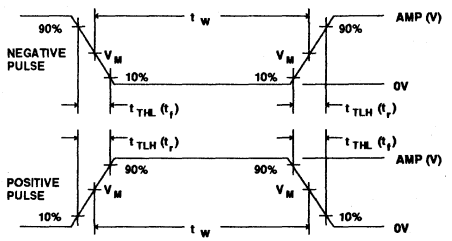
TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Look-ahead carry generator — FAST 74F182

FEATURES

- Provides carry look-ahead across a group of four ALU's
- Multi-level look-ahead for high speed arithmetic operation over long word lengths

DESCRIPTION

The 74F182 is a high speed carry look-ahead generator. It accepts up to four pairs of active-Low Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active-High Carry input (C_n) and provides anticipated active-High carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 'F182 also has active-Low Carry Propagate ($\overline{P}$) Carry Generate ($\overline{G}$) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$

$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$

$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$

$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$

$$\overline{P} = \overline{P_3P_2P_1P_0}$$

The 'F182 can also be used with binary ALU's in an active-Low or active-High input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F182	5.0ns	21mA

ORDERING INFORMATION

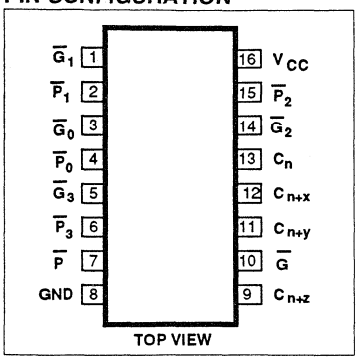
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C
16-pin Plastic DIP	N74F182N
16-pin Plastic SO	N74F182D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

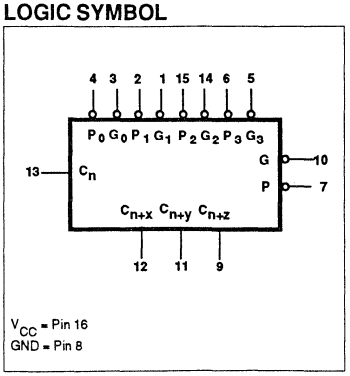
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
C_n	Carry input	2.5/2.0	50µA/1.2mA
$\overline{G}_0$, $\overline{G}_2$	Carry generate inputs (active-Low)	2.5/14.0	50µA/8.4mA
$\overline{G}_1$	Carry generate input (active-Low)	2.5/16.0	50µA/9.6mA
$\overline{G}_3$	Carry generate input (active-Low)	2.5/8.0	50µA/4.8mA
$\overline{P}_0$, $\overline{P}_1$	Carry propagate inputs (active-Low)	2.5/8.0	50µA/4.8mA
$\overline{P}_2$	Carry propagate input (active-Low)	2.5/6.0	50µA/3.6mA
$\overline{P}_3$	Carry propagate input (active-Low)	2.5/4.0	50µA/2.4mA
C_{n+x} - C_{n+z}	Carry outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry generate output (active-Low)	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output (active-Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

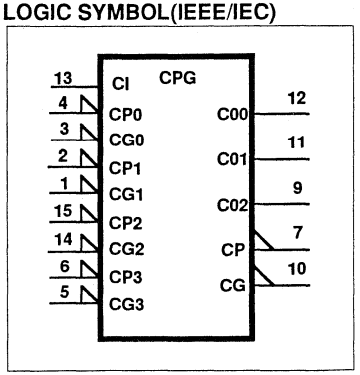
PIN CONFIGURATION



LOGIC SYMBOL

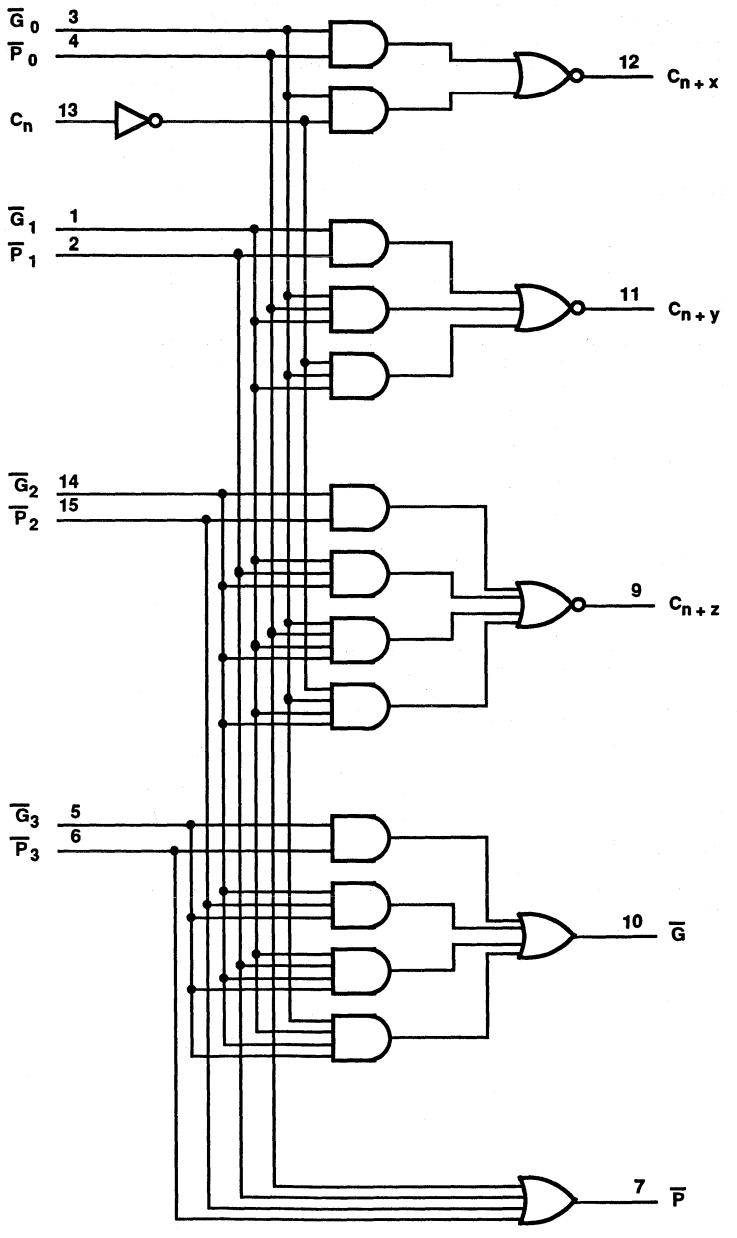


LOGIC SYMBOL(IEEE/IEC)



Look-ahead carry generator FAST 74F182

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

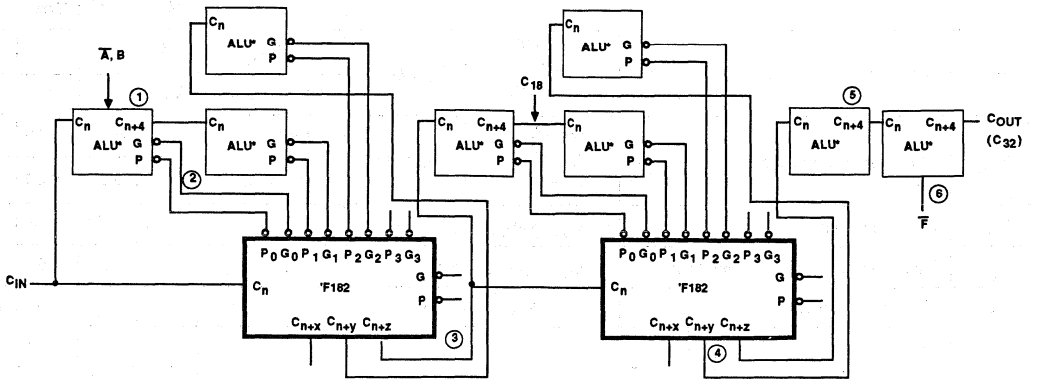
FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = High voltage level
L = Low voltage level
X = Don't care

Look-ahead carry generator FAST 74F182

APPLICATION



32-Bit ALU With Ripple Carry Between 16-Bit Look-Ahead ALUs
(*ALU's may be either 'F181 or 'F381)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					250	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					250	µA
I_{IL}	Low-level input current	C_n	V_{CC} = MAX, V_I = 0.5V					-1.2	mA
		$\overline{G}_0$, $\overline{G}_2$						-8.4	mA
		$\overline{G}_1$						-9.6	mA
		$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$						-4.8	mA
		$\overline{P}_2$						-3.6	mA
		$\overline{P}_3$						-2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				18	28	mA
		I_{CCL}					24	36	mA

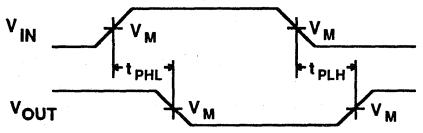
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

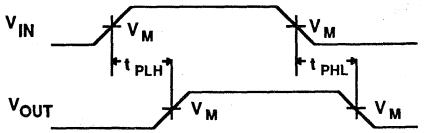
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 2	2.5 2.5	5.0 5.0	8.0 7.5	2.5 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_0$, $\overline{P}_1$ or $\overline{P}_2$ to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 1	2.0 1.5	5.0 3.5	7.0 5.0	1.5 1.5	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{G}_{0,1,2}$ to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 1	1.5 1.5	4.0 3.0	7.5 5.0	1.5 1.5	8.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_{1,2,3}$ to $\overline{G}$	Waveform 2	2.0 3.0	7.0 5.0	10.0 7.0	1.5 2.5	11.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{G}_n$ to $\overline{G}$	Waveform 2	1.5 3.0	5.0 5.0	7.0 7.0	1.5 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ or $\overline{P}$	Waveform 2	1.5 2.5	3.5 4.0	6.0 6.0	1.5 2.5	7.5 6.5	ns

AC WAVEFORMS



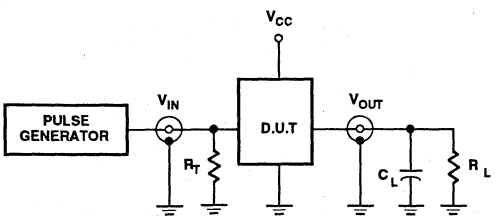
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



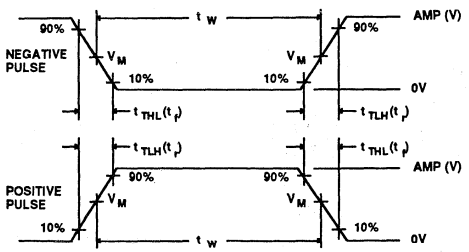
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

64-Bit TTL bipolar RAM, inverting (3-State) — 74F189A

FEATURES

- High speed performance
- Replaces 74F189
- Address access time: 8ns max vs 28ns for 74F189
- Power dissipation: 4.3mW/bit
- Schottky clamp TTL
- One chip enable
- Inverting outputs (for non-inverting outputs see 74F219A)
- 3-state outputs
- 74F189A in 150 mil wide SO is preferred options for new designs
- C3F189A in 300 mil wide SOL replaces 74F189 in existing designs

DESCRIPTION

The 74F189A is a high speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The outputs are in high impedance state whenever the chip enable ($\overline{CE}$) is high. The outputs are active only in the READ mode ($\overline{WE}$ = high) and the output data is the complement of the stored data.

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F189A	5.0ns	55mA

ORDERING INFORMATION

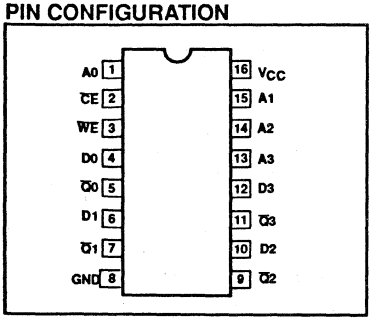
DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16–pin plastic DIP	N74F189AN
16–pin plastic SO (150mil)	N74F189AD
16–pin plastic SOL (300mil)	C3F189AD

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

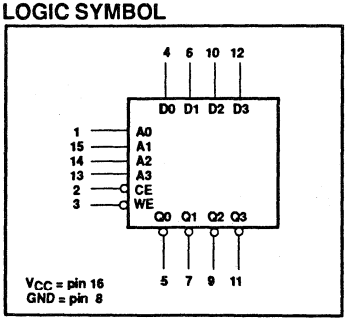
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
A0 – A3	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Chip enable input (active low)	1.0/2.0	20µA/1.2mA
$\overline{WE}$	Write enable input (active low)	1.0/2.0	20µA/1.2mA
$\overline{Q}0$ – $\overline{Q}3$	Data outputs	150/40	3mA/24mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

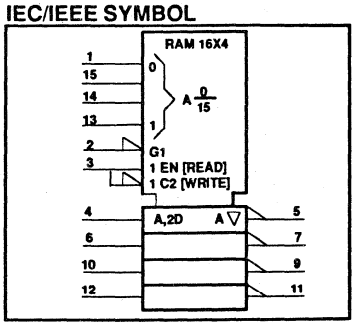
PIN CONFIGURATION



LOGIC SYMBOL

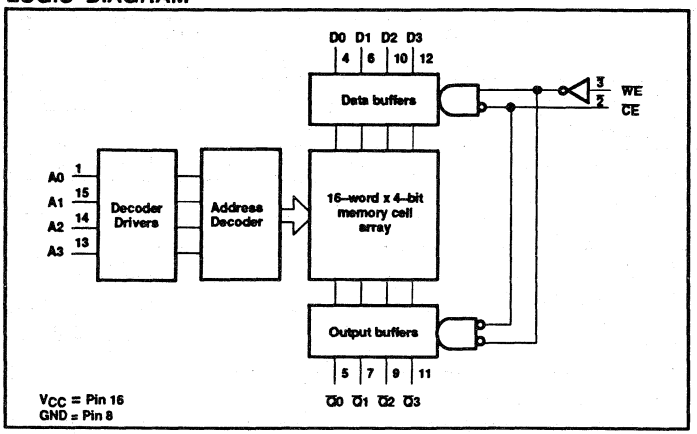


IEC/IEEE SYMBOL



64-Bit TTL bipolar RAM, inverting (3-State) 74F189A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING
$\overline{CE}$	$\overline{WE}$	D	$\overline{O}_n$	MODE
L	H	X	Complement of stored data	Read
L	L	L	High impedance	Write "0"
H	L	H	High imped-	Write "1"
H	X	X	High imped-	Disable input

NOTES:
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	48	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–3	mA
I_{OL}	Low–level output current			24	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current	others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CE}$, $\overline{WE}$					-1.2	mA
I_{OZH}	Offset output current, high–level voltage applied		V_{CC} = MAX, V_I = 2.7V				50	µA
I_{OZL}	Offset output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{CE}$ = $\overline{WE}$ = GND			55	80	mA
C_{IN}	Input capacitance		V_{CC} = 5V, V_{IN} = 2.0V			4		pF
C_{OUT}	Output capacitance		V_{CC} = 5V, V_{OUT} = 2.0V			7		pF

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

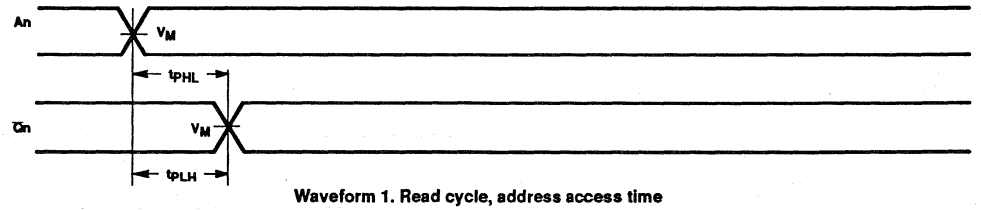
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Access time	Propagation delay An to $\overline{Q}$n	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	8.0 8.0	ns
t_{PZH} t_{PZL}		Enable time $\overline{CE}$ to $\overline{Q}$n	Waveform 2	2.0 2.0	3.5 4.0	6.0 7.0	1.5 2.0	7.0 7.5	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{CE}$ to $\overline{Q}$n		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.5	8.0 6.0	ns
t_{PZH} t_{PZL}	Write recovery time	Enable time $\overline{WE}$ to $\overline{Q}$n	Waveform 4	2.0 2.5	4.0 4.5	6.5 7.5	2.0 2.5	7.0 8.0	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{WE}$ to $\overline{Q}$n		Waveform 4	3.5 1.5	5.5 3.5	8.5 6.5	3.0 1.5	9.0 7.0	ns

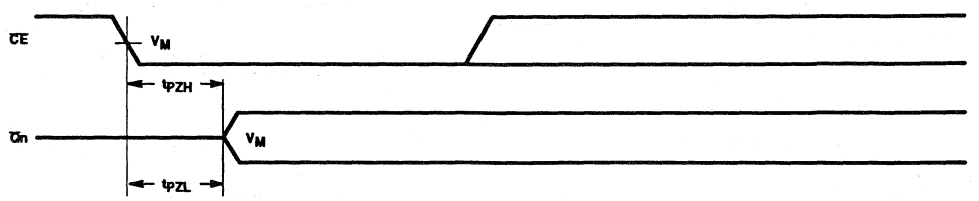
AC SETUP REQUIREMENT

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to $\overline{WE}$	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Dn to $\overline{WE}$	Waveform 4	7.5 6.5			9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Dn to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_{su}(L)$	Setup time, low $\overline{CE}$ (falling edge) to $\overline{WE}$ (falling edge)	Waveform 4	0			0		ns
$t_h(L)$	Hold time, low $\overline{WE}$ (falling edge) to $\overline{WE}$ (rising edge)	Waveform 4	6.5			7.5		ns
$t_w(L)$	Pulse width, low $\overline{WE}$	Waveform 4	7.0			8.0		ns

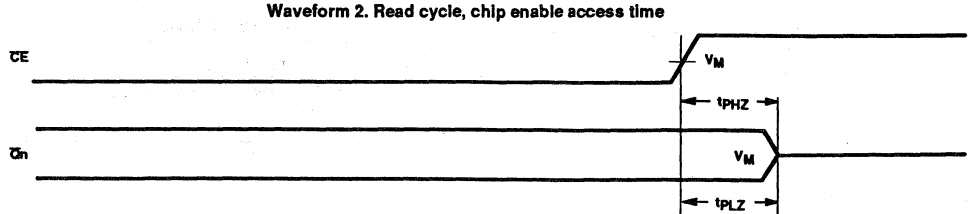
AC WAVEFORMS FOR READ CYCLES



Waveform 1. Read cycle, address access time



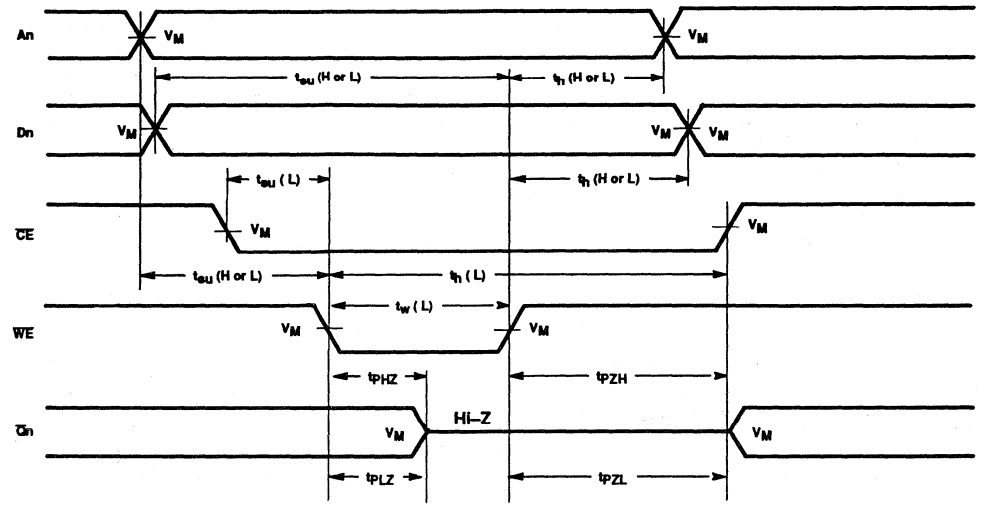
Waveform 2. Read cycle, chip enable access time



Waveform 3. Read cycle, chip disable time

NOTE: For all waveforms, V_M = 1.5V.

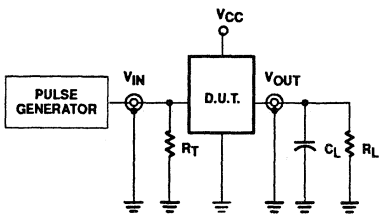
AC WAVEFORMS FOR WRITE CYCLE



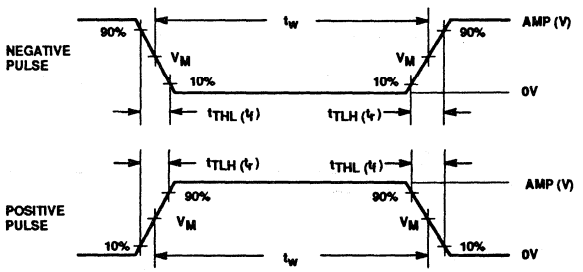
Waveform 3. Write cycle

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORM



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

Document No.	853-0352
ECN No.	94989
Date of issue	November 1, 1988
Status	Product Specification
FAST Products	

FAST 74F190, 74F191 Counters

'F190 Up/Down Decade Counter With Reset and Ripple Clock
'F191 Up/Down Binary Counter With Reset and Ripple Clock

FEATURES

- **High speed-125 MHz typical f_{MAX}**
- **Synchronous, reversible counting**
- **BCD/Decade-'F190**
  4-Bit Binary-'F191
- **Asynchronous parallel load capability**
- **Cascadable without external logic**
- **Single up/down control input**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F190	125MHz	40mA
74F191	125MHz	40mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F190N, N74F191N
16-Pin Plastic SO	N74F190D, N74F191D

DESCRIPTION

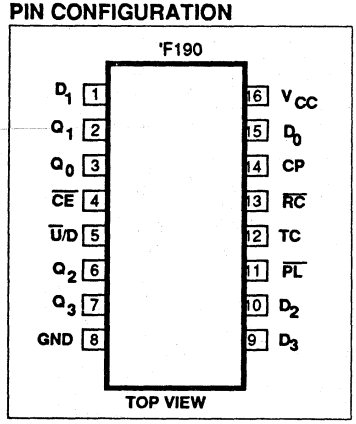
The 74F190 is a presettable Up/Down BCD Decade Counter. The 74F191 is a 4-bit Binary Counter. Both the 'F190 and the 'F191 contain four edge-triggered master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count up and count down operations. Asynchronous parallel load capability permits the counter to preset to any desired number. Information present on the parallel data inputs (D_0-D_3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is Low. This operation overrides the counting function. Counting is inhibited by a High level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is Low, internal state changes are initiated. Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$).

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

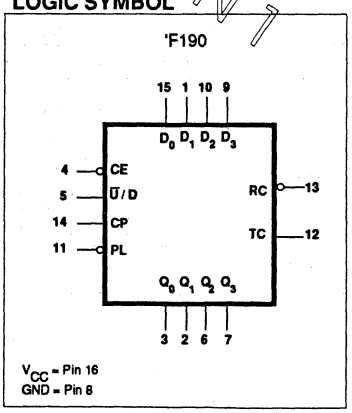
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Count enable input (active Low)	1.0/3.0	20µA/1.8mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{U}$/D	Up/Down count control input	1.0/1.0	20µA/0.6mA
Q_0 -Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{RC}$	Ripple clock output (active Low)	50/33	1.0mA/20mA
TC	Terminal count output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

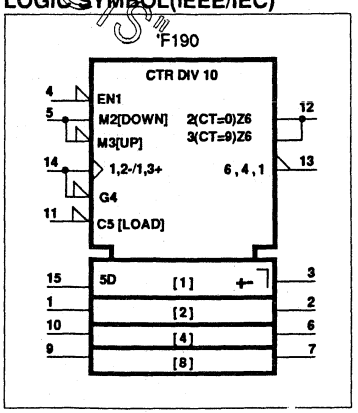
PIN CONFIGURATION



LOGIC SYMBOL

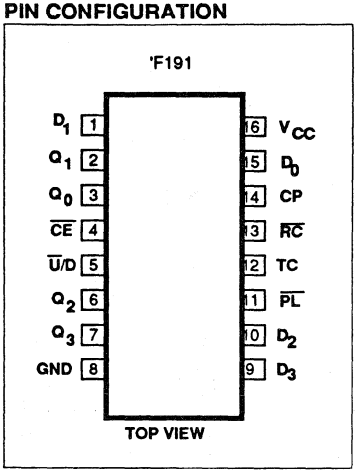


LOGIC SYMBOL(IEEE/IEC)

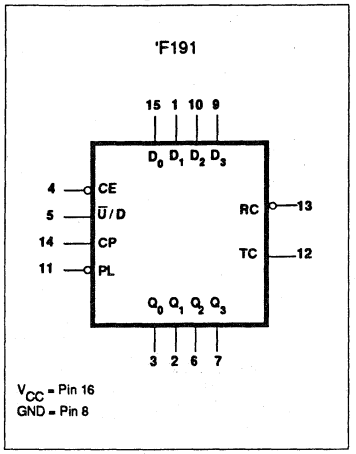


The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "9" for the 'F190 or "15" for the 'F191 in the count up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}/D$ is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output,. When TC is High and $\overline{CE}$ is Low, fthe $\overline{RC}$ follows the clock pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays.

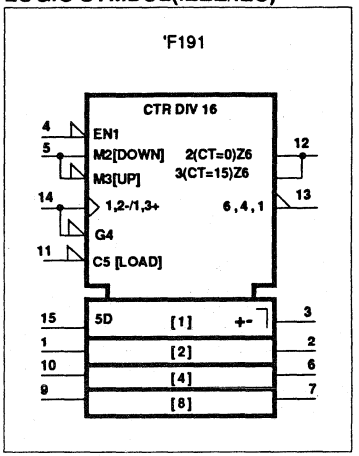
PIN CONFIGURATION



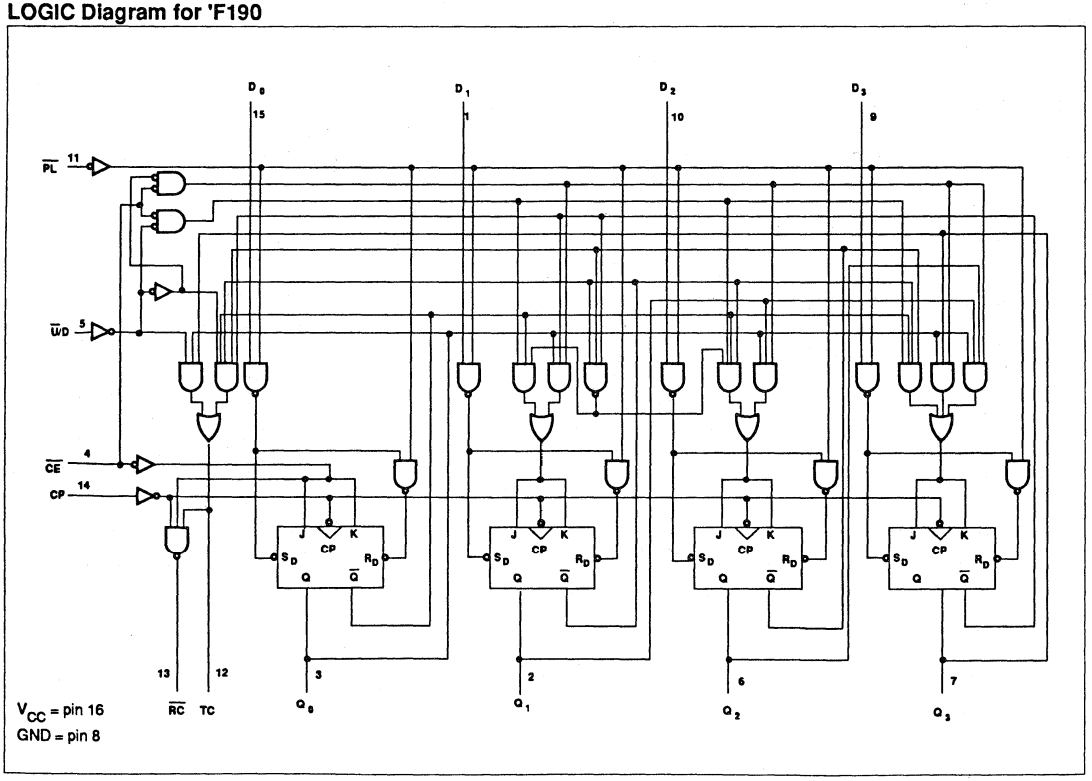
LOGIC SYMBOL



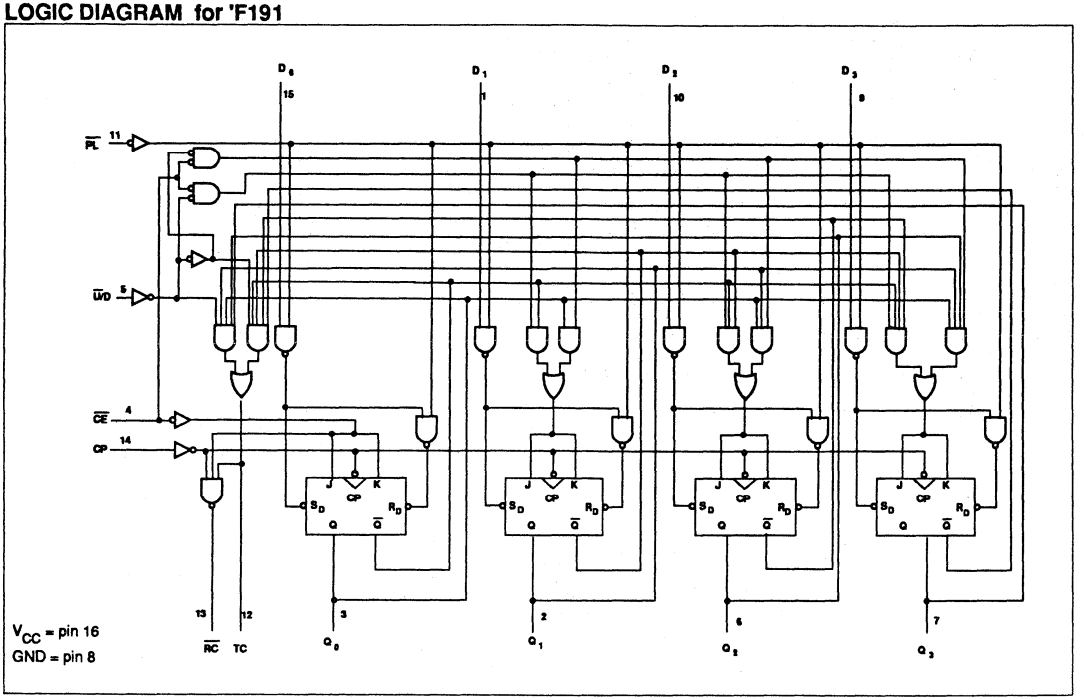
LOGIC SYMBOL(IEEE/IEC)



LOGIC Diagram for 'F190



LOGIC DIAGRAM for 'F191



MODE SELECTION FUNCTION TABLE

INPUTS					OUTPUT	OPERATING MODE
$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	D_n	Q_n	
L	X	X	X	L	L	Parallel load
L	X	X	X	H	H	
H	L	l	↑	X	Count up	Count up
H	H	l	↑	X	Count down	Count down
H	X	H	X	X	No change	Hold (do nothing)

TC and $\overline{RC}$ FUNCTION TABLE for 'F190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊔	H	X	X	H	H	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	H	⊔

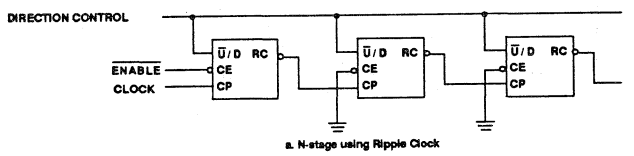
H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊔ = Low pulse

TC and $\overline{RC}$ FUNCTION TABLE for 'F191

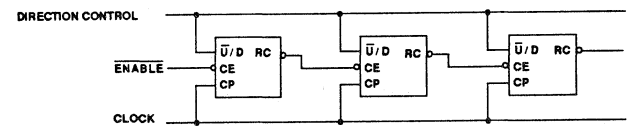
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	H	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	H	⊔

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊔ = Low pulse

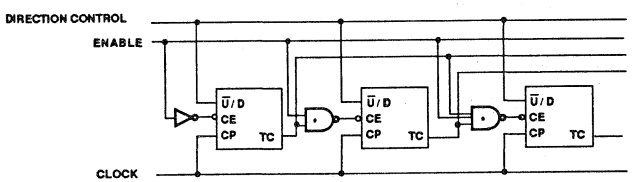
APPLICATIONS



a. N-stage using Ripple Clock



b. Synchronous N-stage Counter with Common Clock using Ripple /Clock



c. Synchronous N-stage Counter with Common Clock and Parrallel Gated Terminal Count

* = Carry Gate

Figure 1

The 'F 190/191 simplifies the design of multi-stage counters, as indicated in Figures 1a and 1b. In Figure 1a, each $\overline{RC}$ output is used as the clock input for the next higher stage. When the clock input source has limited drive capability this configuration is particulary advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first stage and the last stages is represented by the cumulative delay of the clock as it ripples-through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages.The $\overline{RC}$ output signals propagate in ripple fashion and all clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative going edge of the $\overline{RC}$ signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any packages goes High shortly after its clock input goes High, there is no restriction on the High state duration of the clock.

In the Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. The combined TC signals from all the preceding stages forms the $\overline{CE}$ input signal for given stage. An enable signal signal must also be included in each carry gate in order to inhibit counting. Since the TC output of a given stage is not affected by its own $\overline{CE}$, and therefore, the simple scheme of Figure 1a and 1b does not apply.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{CE}$	V_{CC} = MAX, V_I = 0.5V				-1.8	mA
		others					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			40	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} all inputs grounded and all outputs open.

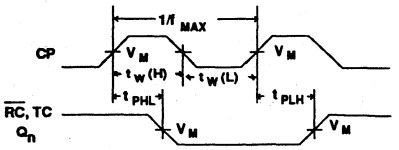
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	74F190, 74F191					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	to Q_n outputs	Waveform 1	100	125		90		MHz
		to $\overline{RC}$ output		85	95		75		
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	2.5 5.0	4.5 7.5	8.0 11.5	2.0 5.0	8.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	6.5 6.0	9.0 8.0	12.5 11.0	6.0 6.0	13.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		Waveform 2	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		Waveform 2	2.0 3.0	4.0 5.0	7.0 7.5	2.0 3.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to $\overline{RC}$		Waveform 2	8.0 4.5	11.0 7.5	16.0 10.5	8.0 4.0	17.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to TC		Waveform 4	4.0 3.0	6.5 6.0	9.5 9.5	3.0 3.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		Waveform 3	2.0 6.5	4.0 9.0	7.0 12.0	1.5 6.5	7.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		Waveform 3 Waveform 4	5.5 6.5	9.5 9.5	13.0 13.0	5.0 6.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		Waveform 3 Waveform 4	6.0 6.0	14.0 11.0	18.0 13.5	6.0 6.0	19.5 15.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		Waveform 5	4.5 5.5	6.5 8.0	9.5 11.5	4.0 5.0	10.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		Waveform 5	5.5 6.0	8.5 10.5	12.0 13.5	5.5 6.0	13.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		Waveform 5	8.5 7.5	16.0 10.0	18.5 13.0	8.5 7.0	21.0 13.5	ns

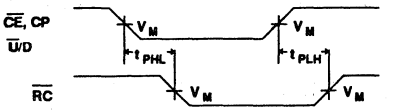
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74F190, 74F191					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns
$t_s(L)$	Setup time, Low $\overline{CE}$ to CP	Waveform 6	10.0			10.0		ns
$t_h(L)$	Hold time, Low $\overline{CE}$ to CP	Waveform 6	0			0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{U}/D$ to CP	Waveform 6	12.0 12.0			12.0 12.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}/D$ to CP	Waveform 6	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.5 6.0			3.5 6.0		ns
$t_w(L)$	$\overline{PL}$ Pulse width, Low	Waveform 5	6.0			6.0		ns
t_{REC}	Recovery time $\overline{PL}$ to CP	Waveform 5	6.0			6.0		ns

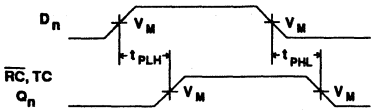
AC WAVEFORMS



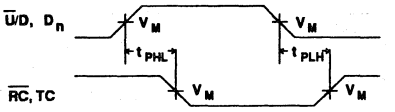
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



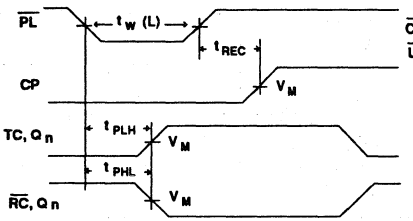
Waveform 2. Propagation Delay, Clock, Clock Enable or Up/Down to Ripple Clock Output



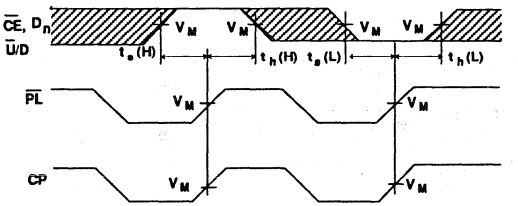
Waveform 3. Propagation Delay, Non-Inverting Path



Waveform 4. Propagation Delay, Inverting Path



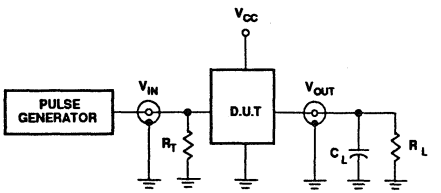
Waveform 5. Parallel Load Pulse Width,Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



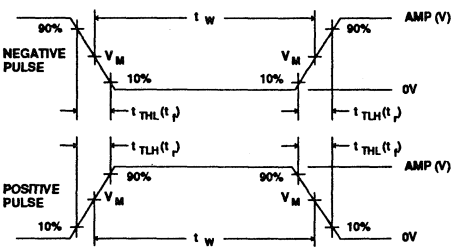
Waveform 6. Data Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0353
ECN No.	98486
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F192, 74F193 Counters

'F192 Up/Down Decade Counter With Separate Up/Down Clocks
'F193 Up/Down Binary Counter With Separate Up/Down Clocks

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F192	125MHz	32mA
74F193	125MHz	32mA

FEATURES

- **Synchronous, reversible 4-bit-counting**
- **Asynchronous parallel load capability**
- **Asynchronous reset (clear)**
- **Cascadable without external logic**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F192N, N74F193N
16-Pin Plastic SO	N74F192D, N74F193D

DESCRIPTION

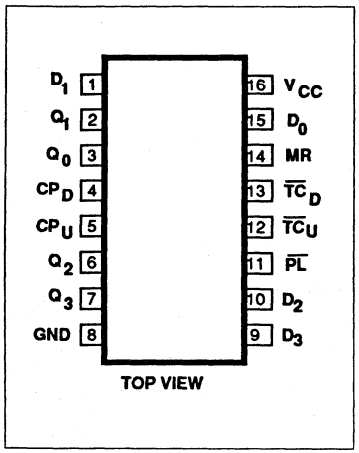
The 74F192 and 74F193 are 4-bit synchronous Up/Down Counters. The 74F192 counts in BCD mode and 74F193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D, respectively simplify operation. The outputs change state synchronously with the Low-to-High transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIgh, the device will count up. If the CP_D clock is pulsed while CP_U is held HIgh, the device will count down The device can be cleared at any time by the asynchronous reset pin. It may also be loaded in parallel by activating the asynchronous parallel load pin. Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, asynchronous preset, load, and synchronous count up and count down functions. Each flip-flop contains JK feedback from slave to master such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one. One clock should be held High while counting with the other, because the circuit will either count by twos or not at all depending on the state of the first JK flip-flop, which cannot toggle as long as either clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally High. When the circuit has reached the maximum count state (9 for the 'F192 and 15 for the 'F193), the next High-to-Low transition of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero state and CP_D goes Low. The $\overline{TC}$ outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous since there is a two-gate delay time difference added for each stage that is added. The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D_0-D_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both clock inputs, and sets all Q outputs Low. If one of the clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of the clock will be interpreted as legitimate signal and will be counted.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

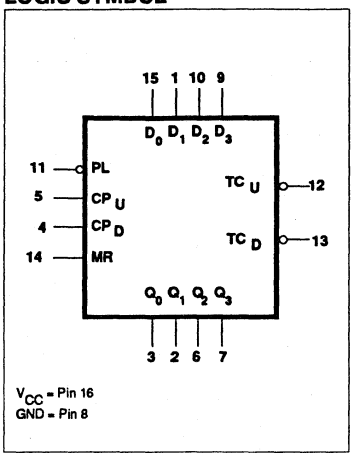
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
CP_U	Count up clock input (active rising edge)	1.0/3.0	20µA/1.8mA
CP_D	Count down clock input (active rising edge)	1.0/3.0	20µA/1.8mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.6mA
MR	Asynchronous Master Reset input	1.0/1.0	20µA/0.6mA
Q_0 -Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active Low)	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

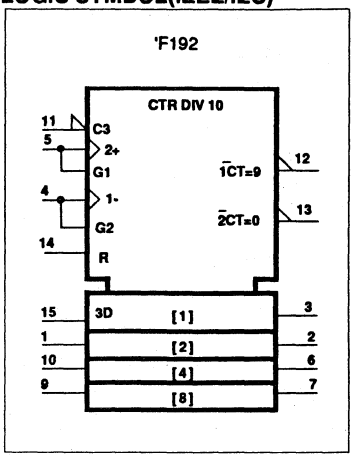
PIN CONFIGURATION



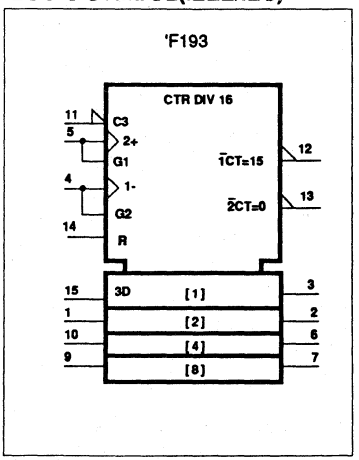
LOGIC SYMBOL



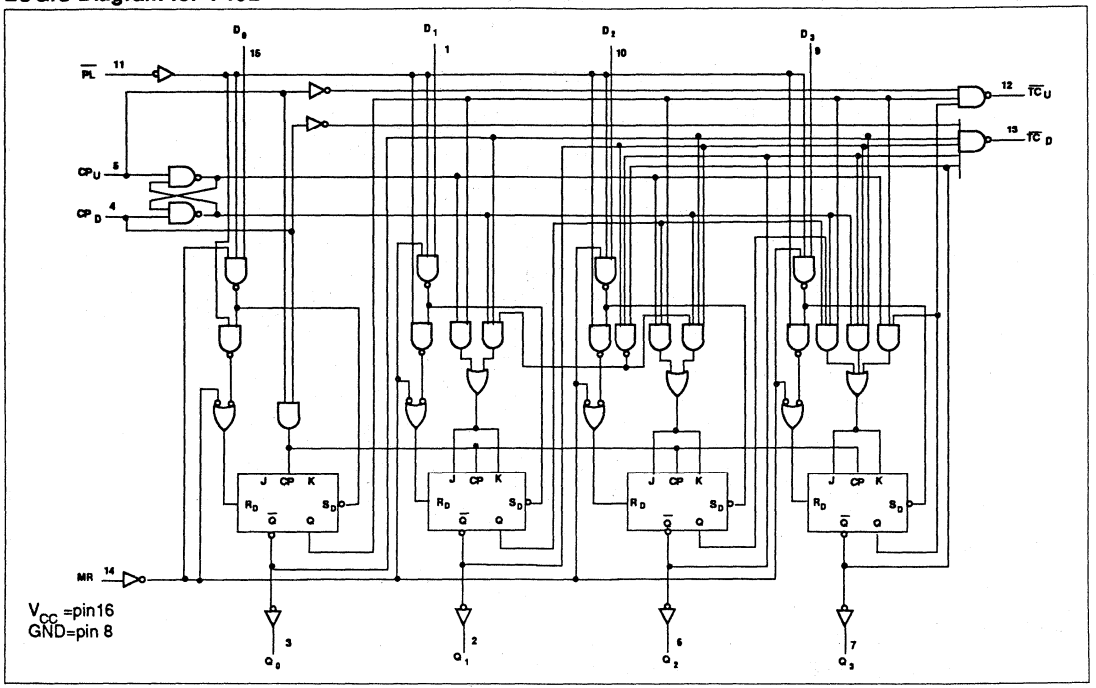
LOGIC SYMBOL(IEEE/IEC)



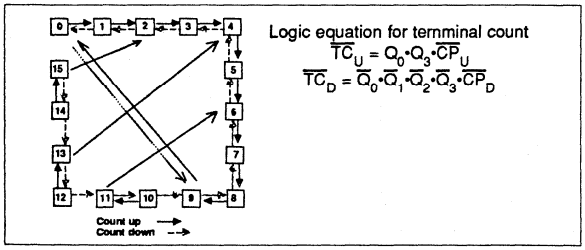
LOGIC SYMBOL(IEEE/IEC)



LOGIC Diagram for 'F192



STATE DIAGRAM for 'F192



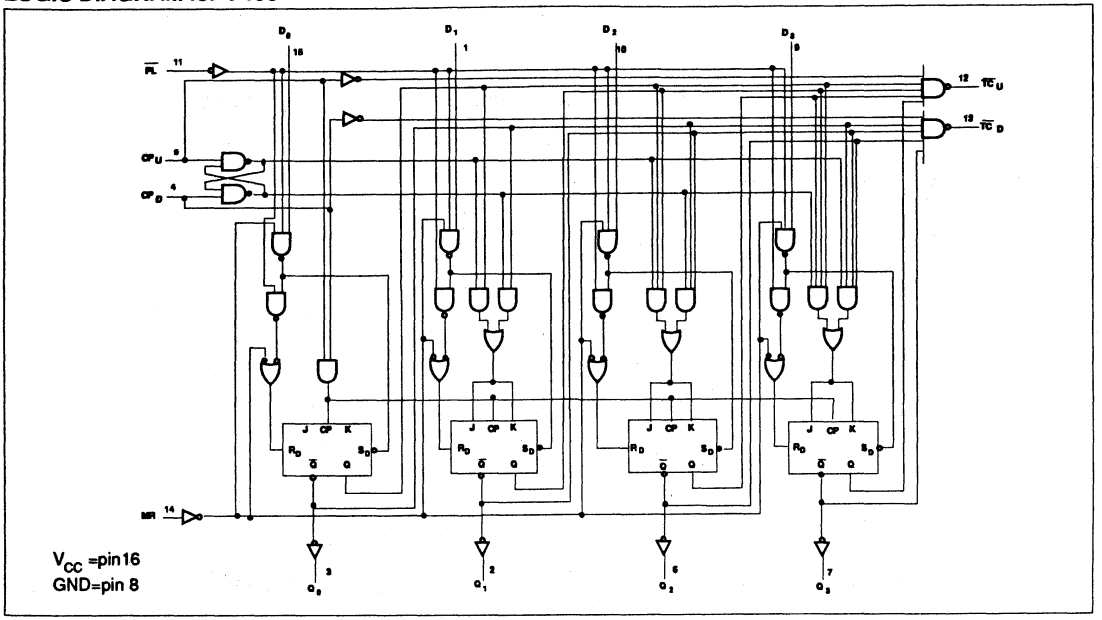
FUNCTION TABLE for ' F192

INPUTS								OUTPUTS						OPERATING MODE
MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$	
H	X	X	L	X	X	X	X	L	L	L	L	H	L	Reset
H	X	X	H	X	X	X	X	L	L	L	L	H	H	
L	L	X	L	L	L	L	L	L	L	L	L	H	L	Parallel load
L	L	X	H	L	L	L	L	L	L	L	L	H	H	
L	L	L	X	H	X	X	H	$Q_n=D_n$				L	H	
L	L	H	X	H	X	X	H	$Q_n=D_n$				H	H	
L	H	↑	H	X	X	X	X	Count up				H^1	H	Count up
L	H	H	↑	X	X	X	X	Count down				H	H^2	Count down

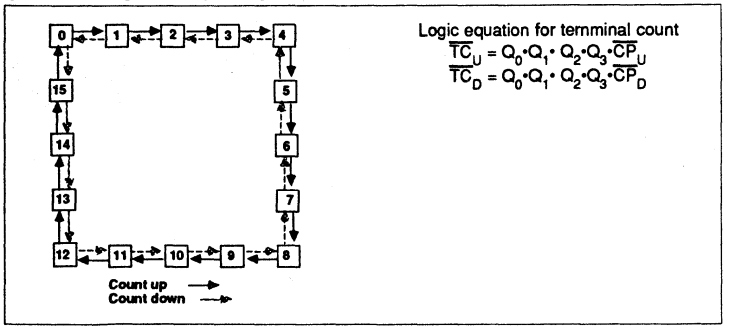
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

NOTES: 1. $\overline{TC}_U = CP_U$ at terminal count up (HLLH)
2. $\overline{TC}_D = CP_D$ at terminal count down (LLLL)

LOGIC DIAGRAM for 'F193



STATE DIAGRAM for 'F193



Logic equation for terminal count

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_D$

FUNCTION TABLE for ' F193

INPUTS								OUTPUTS						OPERATING MODE
MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$	
H	X	X	L	X	X	X	X	L	L	L	L	H	L	Reset
H	X	X	H	X	X	X	X	L	L	L	L	H	H	
L	L	X	L	L	L	L	L	L	L	L	L	H	L	Parallel load
L	L	X	H	L	L	L	L	L	L	L	L	H	H	
L	L	L	X	H	H	H	H	H	H	H	H	L	H	
L	L	H	X	H	H	H	H	H	H	H	H	H	H	
L	H	↑	H	X	X	X	X	Count up				H^1	H	Count up
L	H	H	↑	X	X	X	X	Count down				H	H^2	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

NOTES: 1. $\overline{TC}_U = CP_U$ at terminal count up (HHHH)
2. $\overline{TC}_D = CP_D$ at terminal count down (LLLL)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	CP_U, CP_D	V_{CC} = MAX, V_I = 0.5V					-1.8	mA
		others						-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX				32	50	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with parallel load and Master reset inputs grounded, all other inputs at 4.5V and and all outputs open.

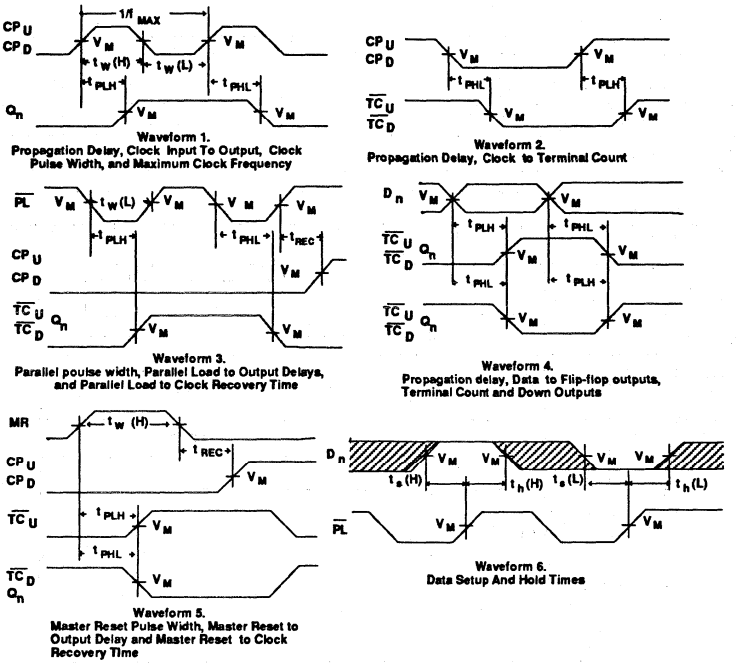
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 2	2.5 3.0	5.5 5.0	8.5 8.0	2.5 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n	Waveform 1	2.5 5.0	5.5 8.5	8.5 12.0	2.5 5.0	9.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 4	2.0 6.0	4.0 9.5	7.0 13.5	1.5 6.0	8.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 3	4.5 5.5	6.5 8.5	10.0 12.0	4.0 5.0	11.0 13.0	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t_{PLH}	Propagation delay MR to $\overline{TC}_U$	Waveform 5	6.0	8.5	12.0	5.5	13.0	ns
t_{PHL}	Propagation delay MR to $\overline{TC}_D$	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 3	6.0 6.0	9.5 9.0	13.5 12.0	6.0 6.0	15.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 4	5.5 4.5	9.0 8.5	13.0 12.5	5.0 4.5	14.0 13.5	ns

AC SETUP REQUIREMENTS

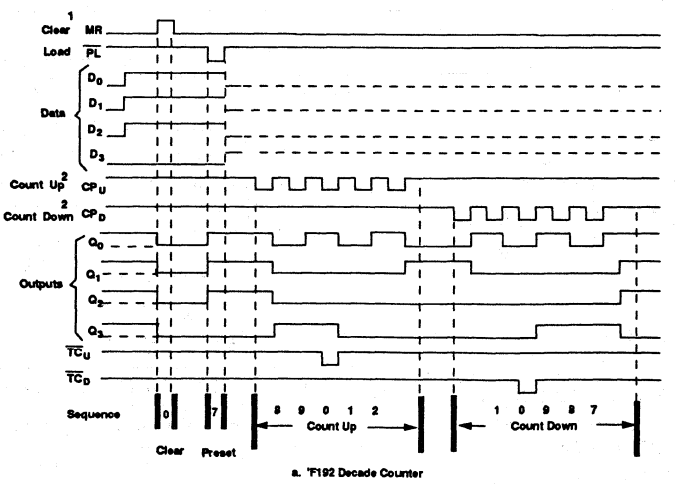
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns
$t_w(L)$	$\overline{PL}$ Pulse width Low	Waveform 3	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	CP_U or CP_D Pulse width High or Low	Waveform 1	3.5 5.0			3.5 5.0		ns
$t_w(L)$	CP_U or CP_D Pulse width, Low (Change of direction)	Waveform 1	10.0			10.0		ns
$t_w(H)$	MR Pulse width High	Waveform 5	6.0			6.0		ns
t_{REC}	Recovery time $\overline{PL}$ to CP_U or CP_D	Waveform 3	6.0			6.0		ns
t_{REC}	Recovery time MR to CP_U or CP_D	Waveform 5	4.0			4.0		ns

AC WAVEFORMS



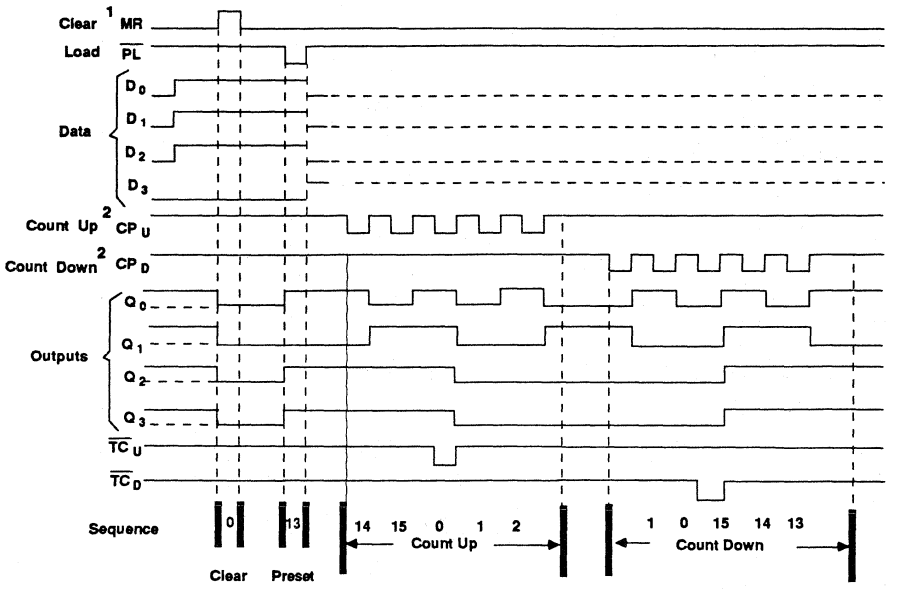
NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TIMING DIAGRAM (Typical clear, load, and count sequence) for 'F192



NOTES: 1. Clear overrides load data and count inputs.
2. When counting up, count down input must be High; when counting down, count up must be High.

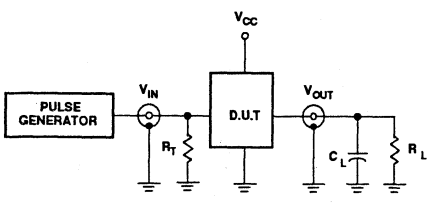
TIMING DIAGRAM (Typical clear, load, and count sequence) for 'F193



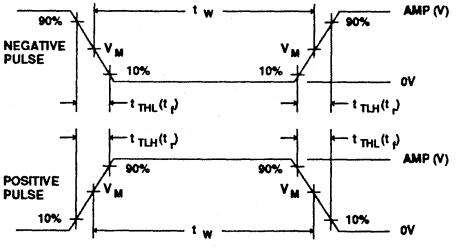
b. 'F193 Binary Counter

NOTES: 1. Clear overrides load data and count inputs.
2. When counting up, count down input must be High; whern counting down, count up must be High.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0354
ECN No.	96224
Date of issue	April 4, 1989
Status	Product Specification
FAST Products	

FAST 74F194
Shift Register

4-Bit Bidirectional Universal Shift Register

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F194	150MHz	33mA

FEATURES

- **Shift right and shift left capability**
- **Synchronous parallel and serial data transfer**
- **Easily expanded for both serial and parallel operation**
- **Asynchronous Master Reset**
- **Hold (do nothing) mode**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F194N
16-Pin Plastic SO	N74F194D

DESCRIPTION

The functional characteristics of the 74F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical) for 74F, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

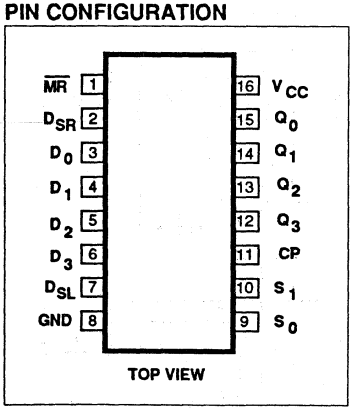
The 'F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select-Function Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.), or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are Low, existing data is retained in a hold (do

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20µA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20µA/0.6mA
S_0, S_1	Mode Select inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Data outputs	50/33	1.0mA/20mA

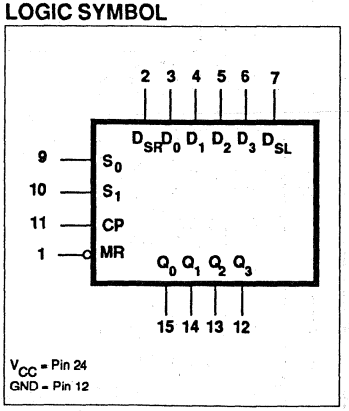
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

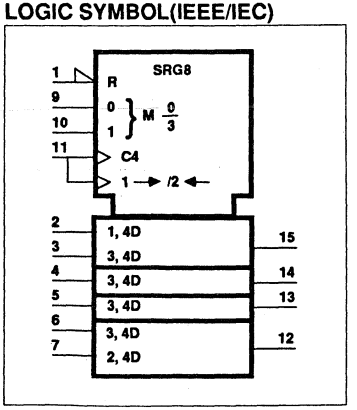


TOP VIEW

LOGIC SYMBOL

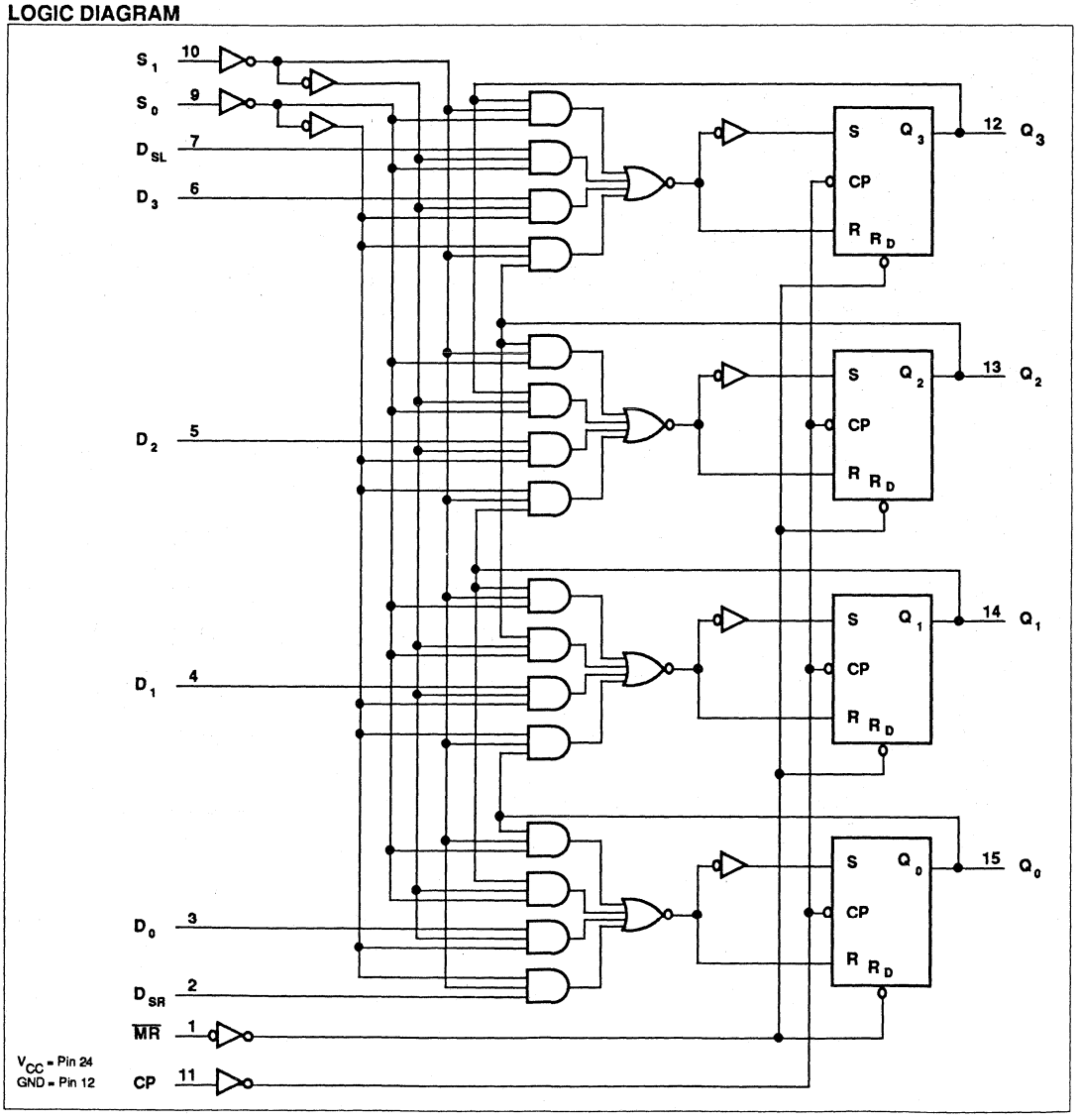


LOGIC SYMBOL(IEEE/IEC)



nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation. Mode Select and data inputs on the 'F194 are edge-triggered, responding only to the Low-to-High transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Select and selected data inputs must be stable one setup time prior to the Low-to-High transition of the clock pulse. Signals on the the Mode Select, Parallel Data (D_0 -D_3) and Serial Data (D_{SR}, D_{SL}) can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge, are observed. The four Parallel Data inputs (D_0 -D_3) are D-type inputs. Data appearing on (D_0-D_3) inputs when S_0 and S_1 are High is transferred to the Q_0-Q_3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				OPERATING MODES
CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3	
X	L	X	X	X	X	X	L	L	L	L	Reset (clear)
X	H	l	l	X	X	X	q_0	q_1	q_2	q_3	Hold (do nothing)
↑	H	h	l	X	l	X	q_1	q_2	q_3	L	Shift left
↑	H	h	l	X	h	X	q_1	q_2	q_3	H	
↑	H	l	h	l	X	X	L	q_0	q_1	q_2	Shift right
↑	H	l	h	h	X	X	H	q_0	q_1	q_2	
↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3	Parallel load

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage[3]	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[4]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[5] (total)	V_{CC} = MAX			33	46	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Output High state will change to Low state if an external voltage of less than 0.0V is applied.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
5. With all outputs open, D_i inputs grounded and a 4.5V applied to S_0, S_1, MR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

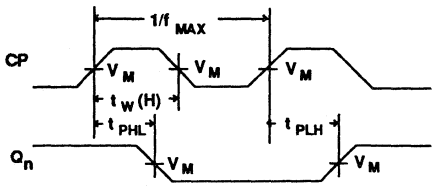
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	150		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.5 3.5	5.2 5.5	7.0 7.0	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5	8.6	12.0	4.5	14.0	ns

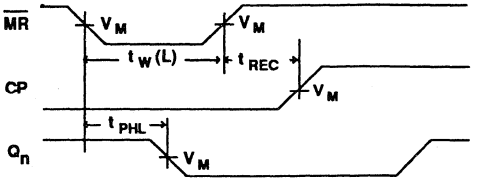
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n, D_{SL}, D_{SR} to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n, D_{SL}, D_{SR} to CP	Waveform 3	0 0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 3	8.0 8.0			9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$	CP Pulse width, High	Waveform 1	5.0			5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			8.0		ns

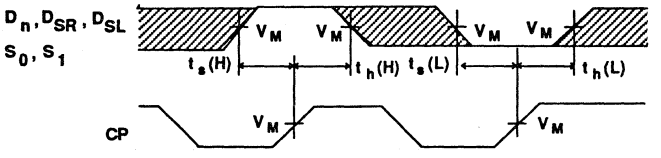
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



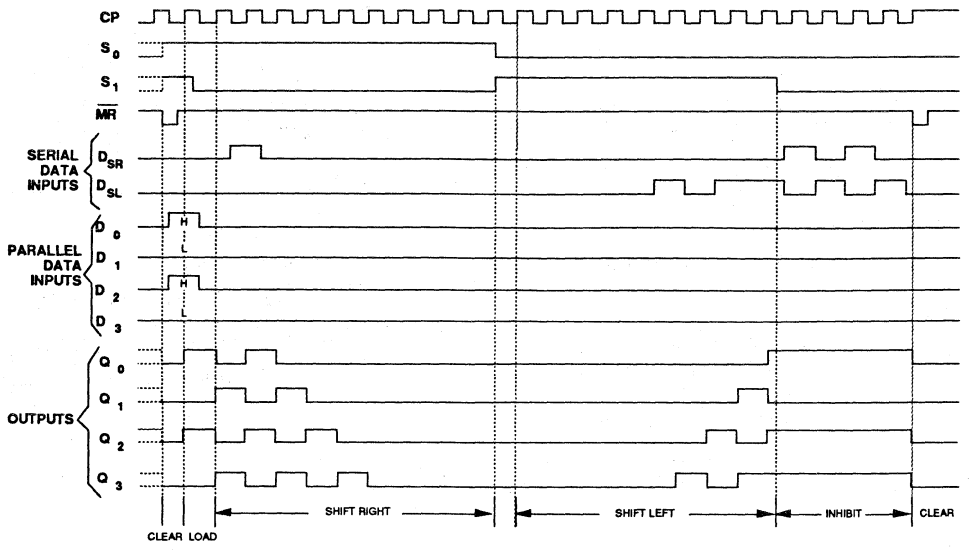
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



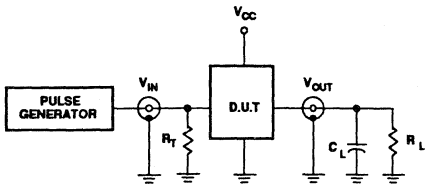
Waveform 3. Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

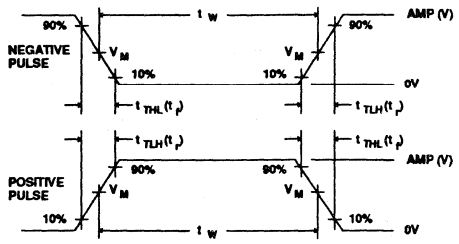
TIMING DIAGRAM (Typical Clear, Load, Shift-Right, Shift-Left and Inhibit Sequence)



TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Shift Register

FAST 74F195, 74F195A

4-Bit Parallel-Access Shift Register

FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in Low and High states) ('F195 only)
- Shift right and parallel load capability
- J - $\overline{K}$ (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset
- Diode inputs ('F195A only)
- Improved AC, DC and functional properties ('F195A only)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F195	115MHz	45mA
74F195A	180MHz	40mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%, T_{amb} = 0°C to +70°C
16-pin plastic DIP	N74F195N
16-pin plastic SO	N74F195D
16-pin plastic DIP	N74F195AN
16-pin plastic SO	N74F195AD

DESCRIPTION

The 74F195 and 74F195A are 4-bit Parallel Access Shift Registers and their functional characteristics are indicated in the Logic diagram and Function Table. These devices are useful in a variety of shifting, counting and storage applications. They perform serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F195 and 74F195A operate in two primary modes: shift right (Q0 → Q1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted one bit in the direction Q0 → Q1 → Q2 →Q3 following each Low -to-High clock transition.

The J and $\overline{K}$ inputs provide the flexibility of the J-$\overline{K}$ type input for special applications, and by tying the two together the

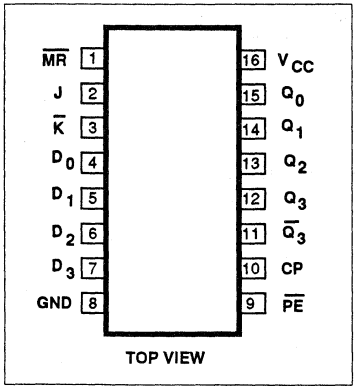
(continued)

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

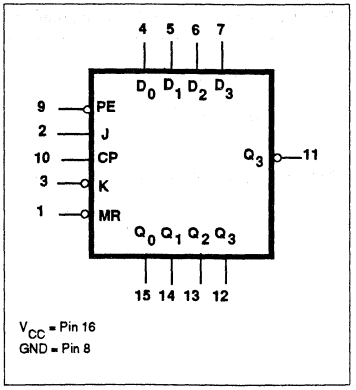
PINS	DESCRIPTION		74F(U.L) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	'F195	1.0/0.033	20μA/20μA
		'F195A	1.0/1.0	20μA/0.6mA
J, $\overline{K}$	J-K or D type serial inputs	'F195	1.0/0.033	20μA/20μA
		'F195A	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	'F195	1.0/0.033	20μA/20μA
		'F195A	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	'F195	2.0/0.066	40μA/40μA
		'F195A	1.0/1.0	20μA/0.6mA
Q0 - Q3, $\overline{Q3}$	Data outputs		50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

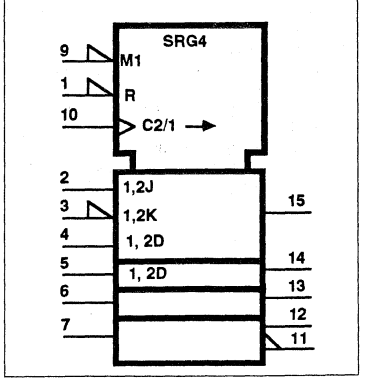
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



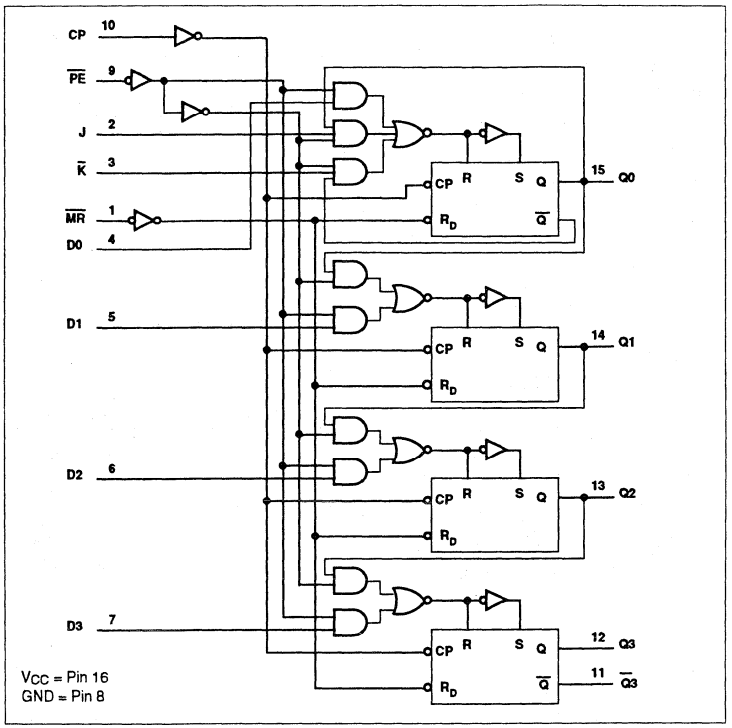
simple D-type input is made for general applications.

The device appears as four common clocked D flip-flops when the PE input is Low. After the Low-to-High clock transition, data on the parallel inputs (D0 - D3) is transferred to the respective Q0 - Q3 outputs. Shift left operation (Q3 - Q2) can be achieved by tying the Qn outputs to the Dn-1 inputs and holding the PE input Low.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 74F195 and 74F195A utilize edge-triggering, therefore there is no restriction on the activity of the J, K, Dn, and PE inputs for logic operation, other than the set-up and hold time requirements.

A Low on the asynchronous Master Reset (MR) input sets all Q outputs Low, independent of any other input condition.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS					OPERATING MODES
MR	CP	PE	J	K	Dn	Q0	Q1	Q2	Q3	Q3	
L	X	X	X	X	X	L	L	L	L	H	Reset (clear)
H	↑	h	h	h	X	H	q0	q1	q2	q2	Shift, set First stage
H	↑	h	l	l	X	L	q0	q1	q2	q2	Shift, reset First stage
H	↑	h	h	l	X	q0	q0	q1	q2	q2	Shift, toggle First stage
H	↑	h	l	h	X	q0	q0	q1	q2	q2	Shift, retain First stage

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
dn(qn) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS [1]		LIMITS			UNIT
				Min	Typ [2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} =MIN, I_{OH} =MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} =MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.5	V
			±5%V_{CC}		0.35	0.5	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V	'F195			100	µA
		V_{CC} = MAX, V_I = 7.0V	'F195A			100	
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	all others			20	µA
			MR ('F195)			40	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	others 'F195			-20	µA
			MR ('F195)			-40	
			'F195A			-600	
I_{OS}	Short-circuit output current [3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	'F195		45	58	mA
			'F195A		40	58	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F195

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Load mode	Waveform 1	120	130		110		MHz
		Shift mode		100	115		90		
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	4.0 4.0	6.5 6.5	9.5 9.0	4.0 4.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q3		Waveform 1	7.0 4.5	10.0 7.0	13.0 9.0	7.0 4.0	13.5 9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn		Waveform 2	5.0	7.5	10.5	5.0	11.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to Q3		Waveform 2	7.0	10.0	13.5	7.0	14.0	ns

AC ELECTRICAL CHARACTERISTICS FOR 74F195A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Load mode	Waveform 1	165	180		150		MHz
		Shift mode		180	190		170		
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.0 2.5	5.0 4.0	9.5 7.0	2.5 2.0	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q3		Waveform 1	2.0 2.0	5.5 4.0	9.5 6.5	2.5 2.0	9.5 7.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn		Waveform 2	2.0	4.0	7.0	2.0	7.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to Q3		Waveform 2	2.5	4.5	8.0	2.0	10.0	ns

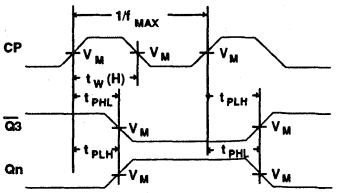
AC SETUP REQUIREMENTS FOR 74F195

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ and Dn to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ and Dn to CP	Waveform3	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	3.0 4.0			3.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_w(H)$	CP Pulse width High	Waveform 1	6.0			6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	6.0			6.0		ns

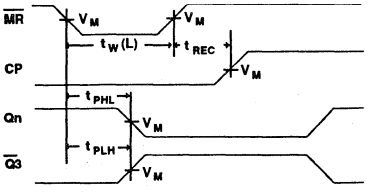
AC SETUP REQUIREMENTS FOR 74F195A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ and Dn to CP	Waveform 3	2.5 2.5			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ and Dn to CP	Waveform3	0.0 1.0			0.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	2.0 2.5			2.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_w(H)$	CP Pulse width High	Waveform 1	4.5			4.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	2.5			3.0		ns

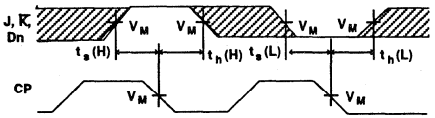
AC WAVEFORMS



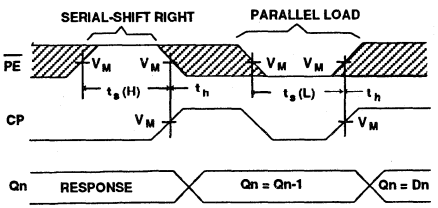
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



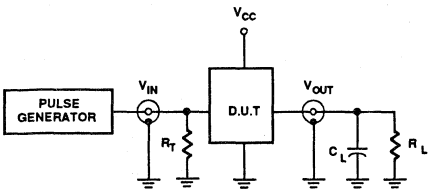
Waveform 3. Data Setup And Hold Times



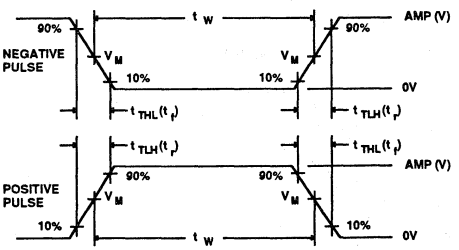
Waveform 4. Setup And Hold Times, Parallel Enable To Clock

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0089
ECN No.	90746
Date of issue	October 2, 1987
Status	Product Specification
FAST Products	

FAST 74F198
Shift Register

8-Bit Bidirectional Universal Shift Register

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F198	95MHz	73mA

FEATURES

- **Buffered clock and control inputs**
- **Shift right, shift left, and parallel load capability**
- **Asynchronous Master Reset**

DESCRIPTION

The 74F198, Bidirectional Universal Shift Register is designed to incorporate virtually all of the features a system designer may want in a shift register. This circuit features parallel inputs and outputs, shift right and shift left serial inputs, operating mode select inputs, and a direct overriding master reset input. The register has four distinct modes of operation:

Parallel (broadside) load
Shift right (in the direction Q_0 toward Q_7)
Shift left (in the direction Q_7 toward Q_0)
Inhibit clock (do nothing)

ORDERING INFORMATION

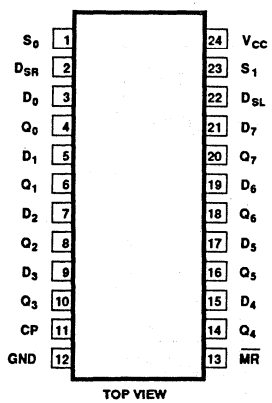
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F198N
24-Pin Plastic SOL	N74F198D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

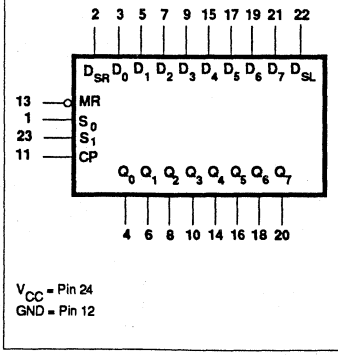
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20µA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20µA/0.6mA
S_0 - S_1	Mode Select inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

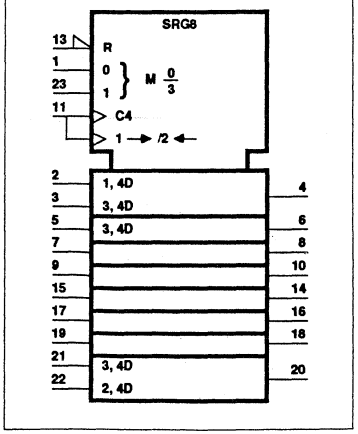
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

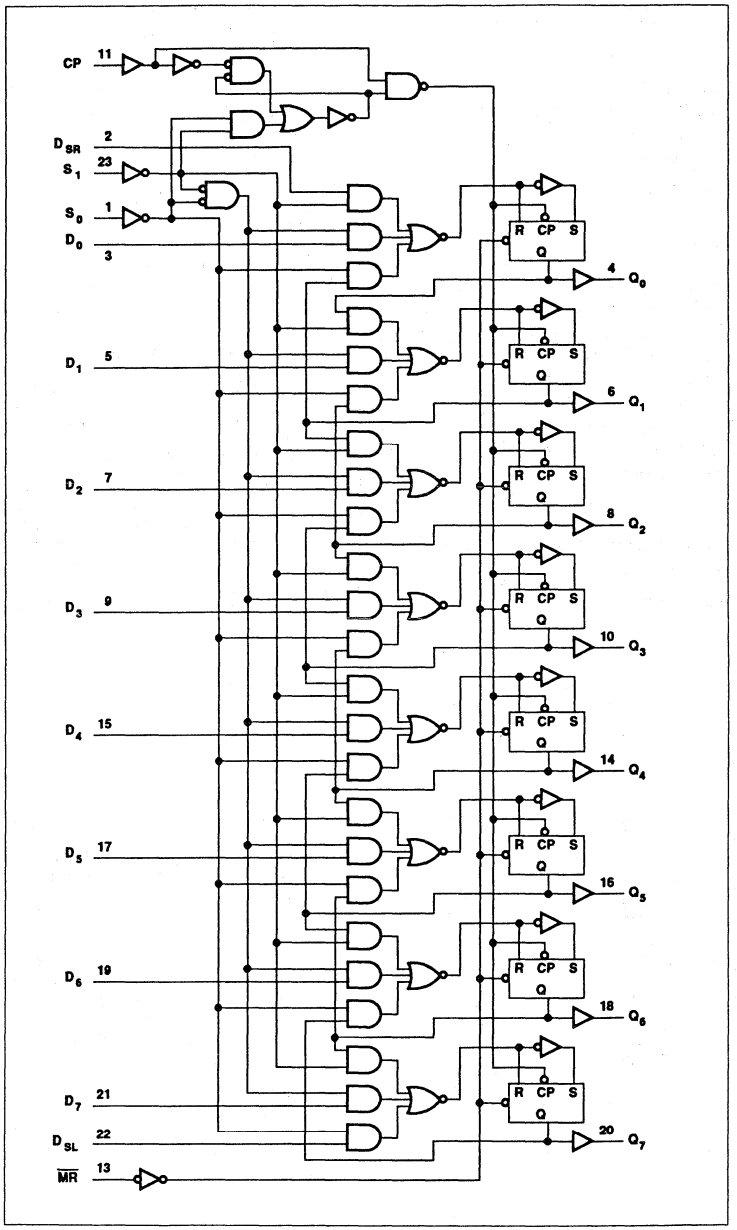


Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, High. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously, with the rising edge of the clock pulse when S_0 is High and S_1 is Low. Serial data for this mode is entered at the right data input (D_{SR}). When S_0 is Low and S_1 is High, data shifts left synchronously and new data is entered at the shift-left serial input (D_{SL}).

Clocking of the flip-flops is inhibited when both mode control inputs are Low.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				
$\overline{MR}$	Mode		CP	Serial		Parallel	Q_0	Q_1	...	Q_6	Q_7
	S_0	S_1		Left	Right	0...7					
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q_{00}	Q_{10}		Q_{60}	Q_{70}
H	H	H	↑	X	X	0...7	0	1		6	7
H	H	L	↑	X	H	X	H	Q_{0n}		Q_{5n}	Q_{6n}
H	H	L	↑	X	L	X	L	Q_{0n}		Q_{5n}	Q_{6n}
H	L	H	↑	H	X	X	Q_{1n}	Q_{2n}		Q_{7n}	H
H	L	H	↑	L	X	X	Q_{1n}	Q_{2n}		Q_{7n}	L
H	L	L	X	X	X	X	Q_{00}	Q_{10}		Q_{60}	Q_{70}

H = High voltage level
L = Low voltage level
X = Don't care

↑ = Low-to-High transition of designated input
0...7 = The level of steady input at inputs 0 through 7, respectively.
Q_{00}, Q_{10}, Q_{60}, Q_{70} = The level of Q_0, Q_1, Q_6, Q_7, respectively, before the indicated steady state input conditions were established.
Q_{0n}, Q_{1n}, Q_{6n}, Q_{7n} = The level of Q_0, Q_1, Q_6, Q_7, respectively, before the most recent Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS

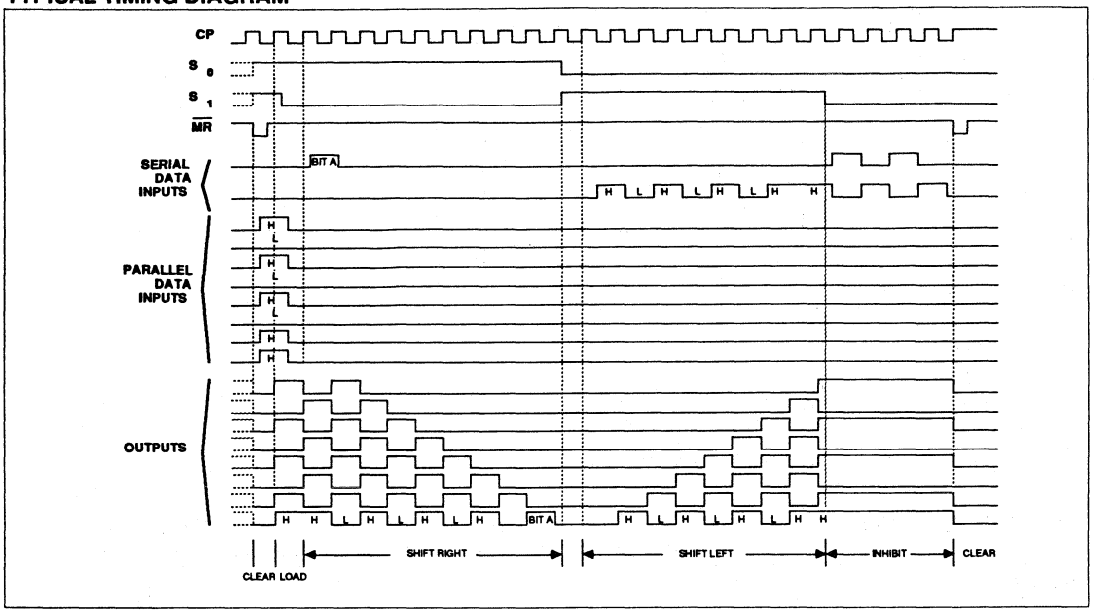
(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

TYPICAL TIMING DIAGRAM



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}				75	110	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

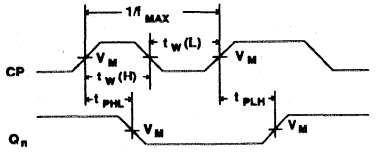
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	5.0 6.0	7.5 8.5	10.0 11.0	4.5 5.5	11.0 12.0	ns
t_{PHL}	Propagation delay	Waveform 3	5.0	7.5	10.0	4.5	11.0	ns

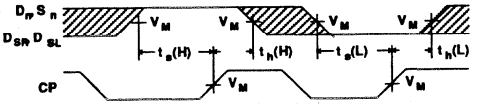
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	0.0 3.0			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	0.0 3.5			1.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 3.0			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 2.5			0.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 2	9.0 6.0			10.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	5.0 5.0			6.0 6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			6.0		ns

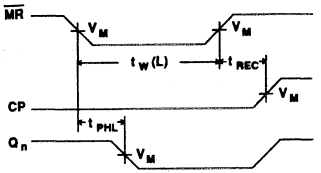
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



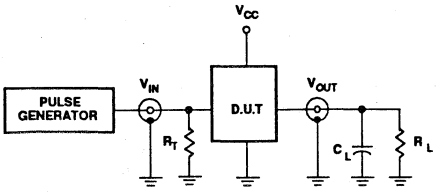
Waveform 2. Setup Time and Hold Time



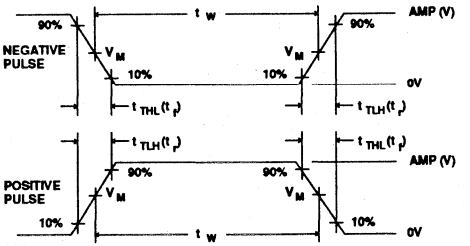
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0082
ECN No.	93568
Date of issue	June 15, 1988
Status	Product Specification
FAST Products	

FAST 74F199
Shift Register

8-Bit Parallel-Access Shift Register

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F199	95MHz	70mA

FEATURES

- **Buffered clock and control inputs**
- **Shift right and parallel load capability**
- **Fully synchronous data transfers**
- **J-$\overline{K}$(D) inputs to first stage**
- **Clock enable for hold (do nothing) mode**
- **Asynchronous Master Reset**

DESCRIPTION

The 74F199 is an 8-bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic diagram and Function Table. The device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F199 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data

ORDERING INFORMATION

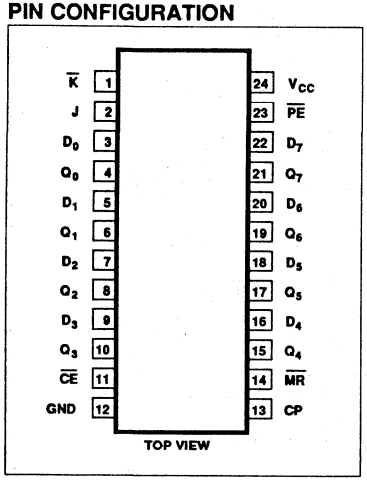
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F199N
24-Pin Plastic SOL	N74F199D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

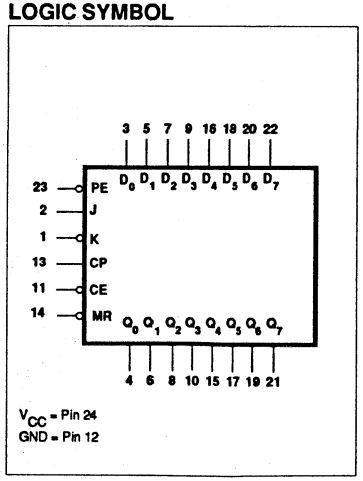
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Parallel data inputs	1.0/1.0	20µA/0.6mA
J, $\overline{K}$	J and K inputs	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Clock Enable input	1.0/1.0	20µA/0.6mA
CP	Clock Pulse inputs (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

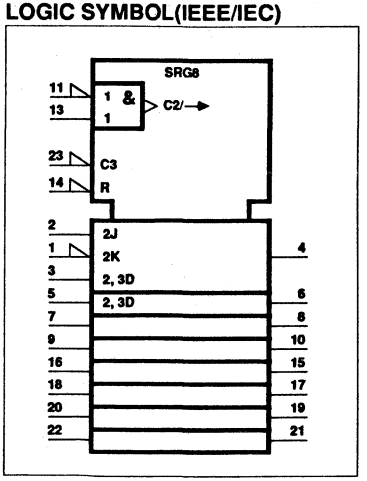
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2$ following each Low -to-High clock transition.

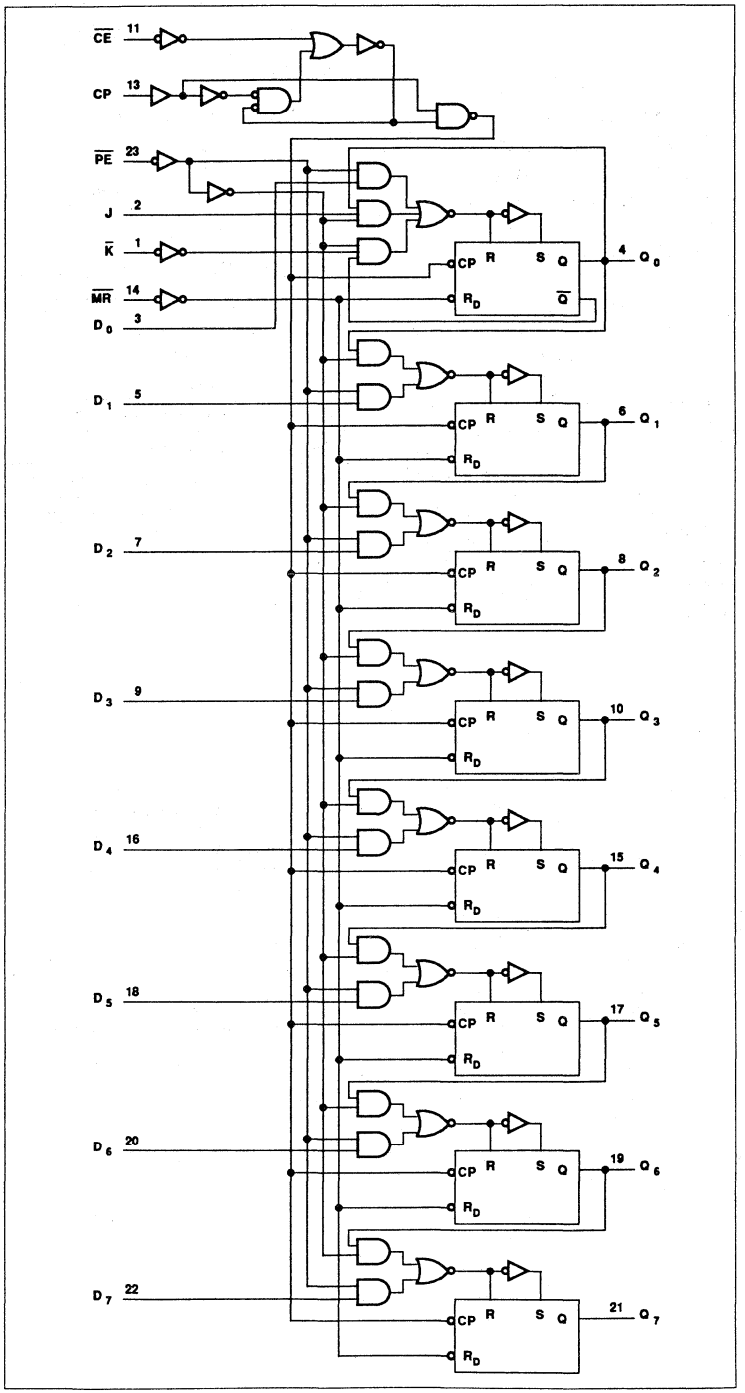
The J and $\overline{K}$ inputs provide the flexibility of the J-$\overline{K}$ type input for special applications, and by tying the two together the simple D-type input is made for general applications.

The device appears as eight common clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low-to-High clock transition, data on the parallel inputs (D_0 - D_7) is transferred to the respective Q_0 - Q_7 outputs.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 74F199 utilizes edge-triggered, therefore there is no restriction on the activity of the J, $\overline{K}$, Dn, and $\overline{PE}$ inputs for logic operation, other than the set-up and hold time requirements.

A Low on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously forcing all bit positions to a Low state.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS					OPERATING MODES
$\overline{MR}$	CP	$\overline{CE}$	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	...	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	...	L	L	Reset (clear)
H	↑	l	h	h	h	X	H	q_0	...	q_5	q_6	Shift, set First stage
H	↑	l	h	l	l	X	L	q_0	...	q_5	q_6	Shift, reset First stage
H	↑	l	h	h	l	X	$\overline{q}_0$	q_0	...	q_5	q_6	Shift, toggle First stage
H	↑	l	h	l	h	X	q_0	q_0	...	q_5	q_6	Shift, retain First stage
H	↑	l	l	X	X	d_n	d_0	d_1	...	d_6	d_7	Parallel load
H	↑	h	X	X	X	X	q_0	q_1	...	q_6	q_7	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

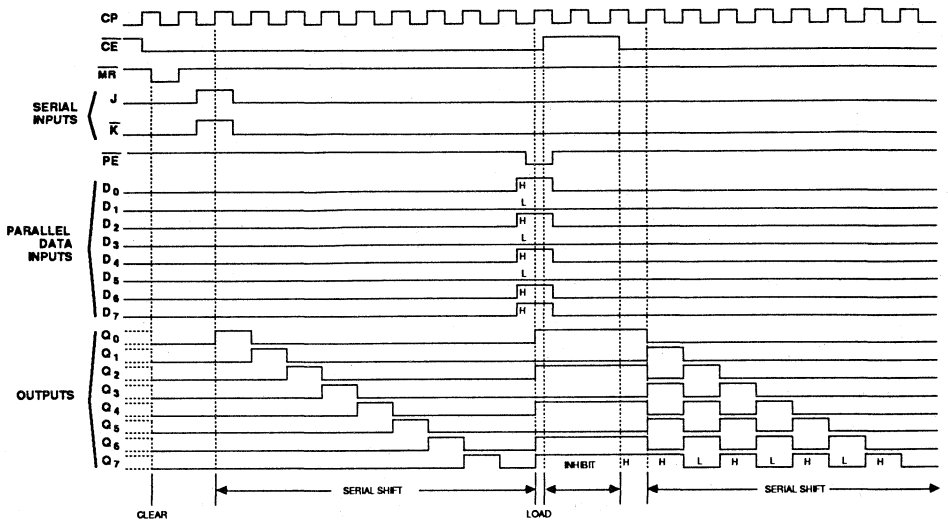
(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

TYPICAL TIMING DIAGRAM



Typical Load, Serial-Shift, Inhibit And Clear Sequences

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			65	90	mA
		I_{CCL}				75	105	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

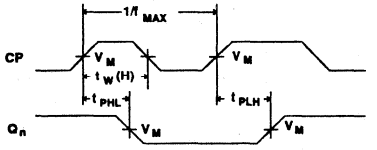
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	5.5 6.5	8.0 9.5	11.0 12.5	4.5 3.5	12.0 13.5	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q_n	Waveform 2	5.5	8.0	10.5	5.0	12.0	ns

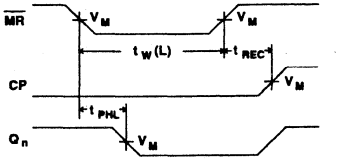
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	0.0 1.5			0.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	2.0 4.5			2.5 5.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ to CP	Waveform 3	0.0 2.5			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ to CP	Waveform 3	0.0 3.5			0.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	Waveform 3	0.0 2.5			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP	Waveform 3	0.0 4.5			0.0 5.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 3	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(H)$	CP Pulse width, High	Waveform 1	4.5			5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.0			4.5		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	5.5			6.5		ns

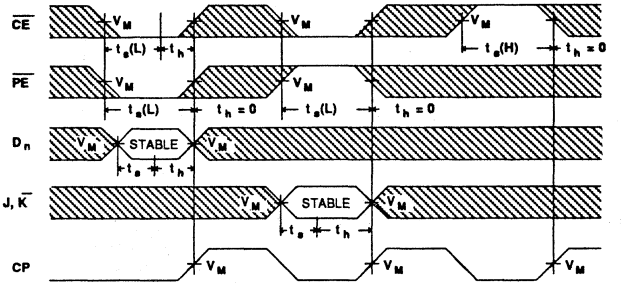
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

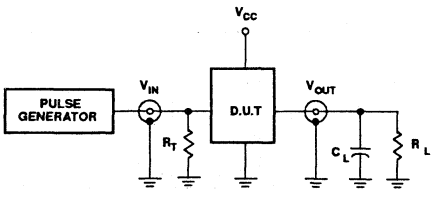


Waveform 3. Setup Time and Hold Time

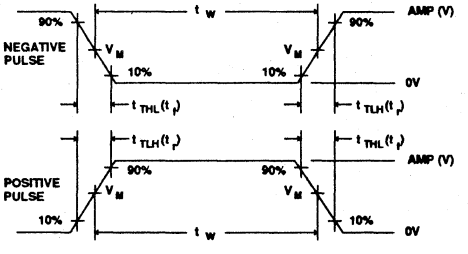
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

64-Bit TTL bipolar RAM, non-inverting (3-State) 74F219A

FEATURES

- High speed performance
- Replaces 74F219
- Address access time: 8ns max vs 28ns for 74F219
- Power dissipation: 4.3mW/bit typ
- Schottky clamp TTL
- One chip enable
- Non–Inverting outputs (for inverting outputs see 74F189A)
- 3–state outputs
- 74F219A in 150 mil wide SO is preferred options for new designs
- C3F219A in 300 mil wide SOL replaces 74F219 in existing designs

DESCRIPTION

The 74F219A is a high speed, 64–bit RAM organized as a 16–word by 4–bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The outputs are in high impedance state whenever the chip enable ($\overline{CE}$) is high. The outputs are active only in the READ mode ($\overline{WE}$ = high) and the output data is the complement of the stored data.

APPLICATIONS

- Scratch pad memory
- Buffer memory
- Push down stacks
- Control store

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT(TOTAL)
74F219A	5.0ns	55mA

ORDERING INFORMATION

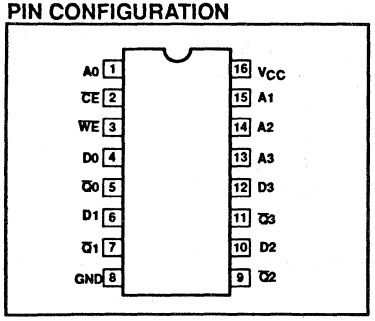
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16–pin plastic DIP	N74F219AN
16–pin plastic SO (150mil)	N74F219AD
16–pin plastic SOL (300mil)	C3F219AD

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

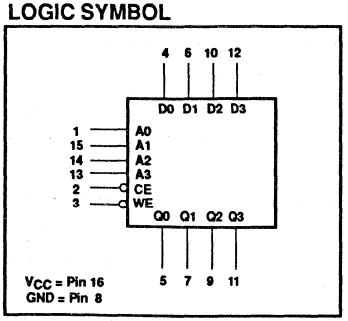
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
A0 – A3	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Chip enable input (active low)	1.0/2.0	20µA/1.2mA
$\overline{WE}$	Write enable input (active low)	1.0/2.0	20µA/1.2mA
Q0 – Q3	Data outputs	150/40	3mA/24mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

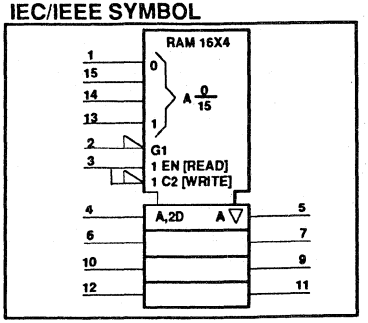
PIN CONFIGURATION



LOGIC SYMBOL

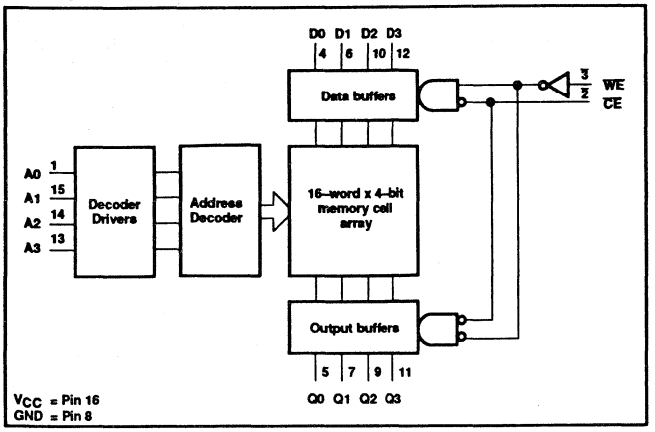


IEC/IEEE SYMBOL



64-Bit TTL bipolar RAM, non-inverting (3-State) 74F219A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
$\overline{C}$	$\overline{W}$	D	Q_n	
L	H	X	Stored data	Read
L	L	L	High impedance	Write "0"
H	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable input

NOTES:
4. H = High voltage level
5. L = Low voltage level
6. X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	48	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High–level output current			–3	mA
I_{OL}	Low–level output current			24	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current	others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CE}$, $\overline{WE}$					-1.2	mA
I_{OZH}	Offset output current, high–level voltage applied		V_{CC} = MAX, V_I = 2.7V				50	µA
I_{OZL}	Offset output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{CE}$ = $\overline{WE}$ = GND			55	80	mA
C_{IN}	Input capacitance		V_{CC} = 5V, V_{IN} = 2.0V			4		pF
C_{OUT}	Output capacitance		V_{CC} = 5V, V_{OUT} = 2.0V			7		pF

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

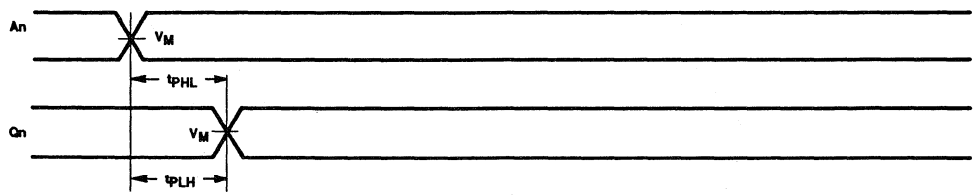
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Access time	Propagation delay An to Qn	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	8.0 8.0	ns
t_{PZH} t_{PZL}		Enable time $\overline{CE}$ to Qn	Waveform 2	1.5 2.5	3.0 4.0	6.0 7.0	1.5 2.0	7.0 7.5	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{CE}$ to Qn		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.0	8.0 6.0	ns
t_{PZH} t_{PZL}	Write recovery time	Enable time $\overline{WE}$ to Qn	Waveform 4	2.0 3.0	3.5 4.5	6.5 7.5	1.5 2.5	7.0 8.0	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{WE}$ to Qn		Waveform 4	3.0 1.5	5.0 3.5	8.0 6.0	2.5 1.5	9.0 7.0	ns

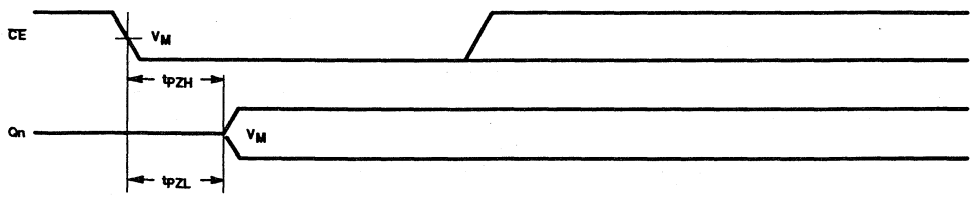
AC SETUP REQUIREMENT

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to $\overline{WE}$	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Dn to $\overline{WE}$	Waveform 4	8.0 7.5			9.0 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Dn to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_{su}(L)$	Setup time, low $\overline{CE}$ (falling edge) to $\overline{WE}$ (falling edge)	Waveform 4	0			0		ns
$t_h(L)$	Hold time, low $\overline{WE}$ (falling edge) to $\overline{WE}$ (rising edge)	Waveform 4	6.5			7.5		ns
$t_w(L)$	Pulse width, low $\overline{WE}$	Waveform 4	7.0			8.0		ns

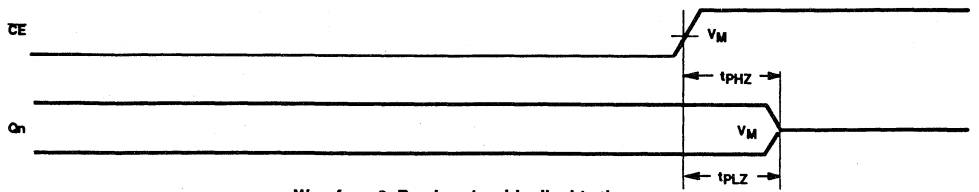
AC WAVEFORMS FOR READ CYCLES



Waveform 1. Read cycle, address access time



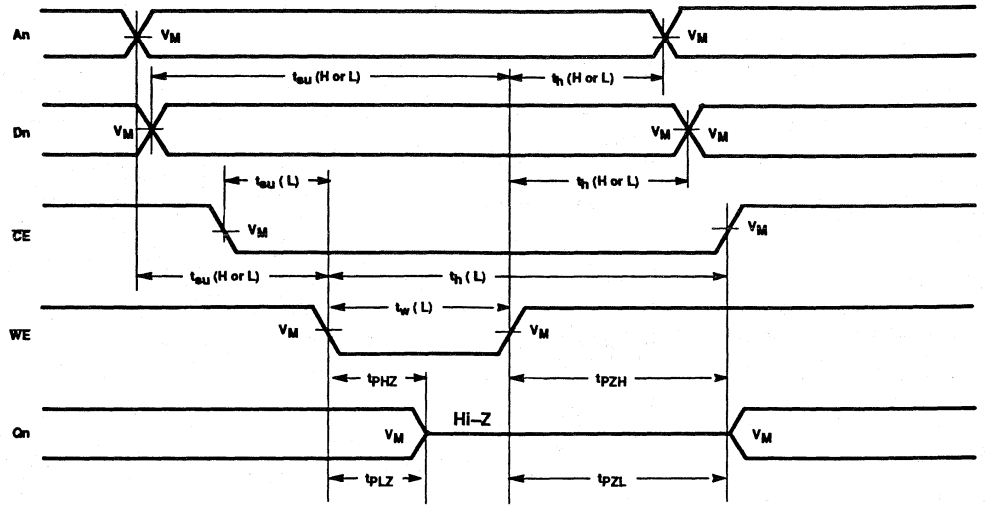
Waveform 2. Read cycle, chip enable access time



Waveform 3. Read cycle, chip disable time

NOTE: For all waveforms, V_M = 1.5V.

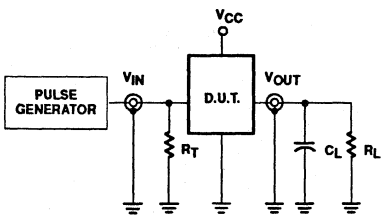
AC WAVEFORMS FOR WRITE CYCLE



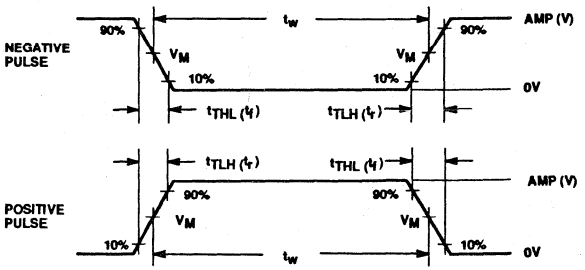
Waveform 4. Write cycle

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORM



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Document No.	
ECN No.	
Date of Issue	September 7, 1990
Status	Preliminary specification
FAST products	

FAST 74F222

16X4 Synchronous FIFO with ready enables (3–state)

FEATURES

- Independent synchronous inputs and outputs
- Organized as 16 words of 4 bits
- DC to 50MHz data rate
- 3–state outputs
- Cascadable in word–width and depth direction

DESCRIPTION

This 64–bit active element first–in–first–out (FIFO) is a monolithic Schottky–clamped transistor–transistor logic (STLL) array organized as 16 words of 5–bit s each. A memory system using the 74F222 can be easily expanded in multiples of 15m+1 words or of 4n bits, or both, (where n is number of packages in the vertical array) and no external gating is featured. The 3–state outputs controlled by a single input (OE) make bus connection and multiplexing easy. The 74F222 processes data in a parallel format at any desired clock rate from DC to 50MHz.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F222	50MHz	90mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20–pin plastic DIP	N74F222N
20–pin plastic SOL	N74F222D

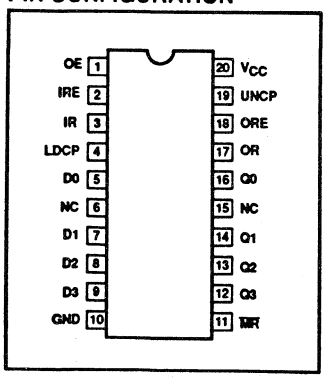
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
LDCP	Load clock input	1.0/1.0	20µA/0.6mA
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
OE	Output enable input (active high)	1.0/1.0	20µA/0.6mA
UNCP	Unload clock input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master reset input (active low)	1.0/1.0	20µA/0.6mA
IR	Input ready output	50/33	1.0mA/20mA
Q0 – Q3	Data outputs	50/33	1.0mA/20mA
OR	Output ready output	50/33	1.0mA/20mA

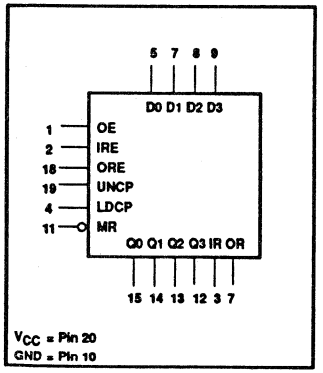
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

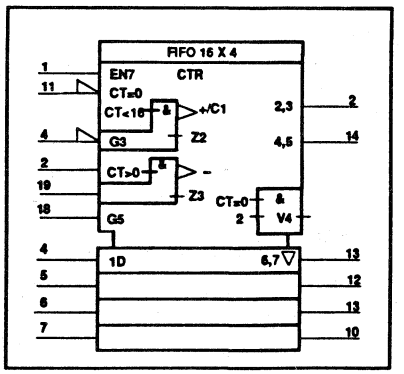
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



Document No.	
ECN No.	
Date of Issue	September 7, 1990
Status	Preliminary specification
FAST products	

FAST 74F224

16X4 Synchronous FIFO (3–state)

FEATURES

- Independent synchronous inputs and outputs
- Organized as 16 words of 4 bits
- DC to 50MHz data rate
- 3–state outputs
- Cascadable in word–width and depth direction

DESCRIPTION

This 64–bit active element First–In–First–Out (FIFO) is a monolithic Schottky–clamped transistor–transistor logic (STLL) array organized as 16 words of 4–bits each. A memory system using the 74F224 can be easily expanded in multiples of 15m+1 words or of 4n bits, or both (where n is the number of packages in the horizontal array). However, an external gating is required (see Figure 1). For longer words using 74F224, the IR signals of the first–rank packages and OR signals of the last–rank packages must be ANDed for proper synchronization.The 3–state outputs controlled by a single input (OE) make bus connection and multiplexing easy.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F224	50MHz	90mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16–pin plastic DIP	N74F224N
16–pin plastic SOL	N74F224D

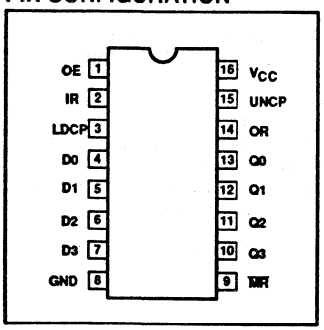
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
LDCP	Load clock input	1.0/1.0	20µA/0.6mA
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
OE	Output enable input (active high)	1.0/1.0	20µA/0.6mA
UNCP	Unload clock input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master reset input (active low)	1.0/1.0	20µA/0.6mA
IR	Input ready output	50/33	1.0mA/20mA
Q0 – Q3	Data outputs	50/33	1.0mA/20mA
OR	Output ready output	50/33	1.0mA/20mA

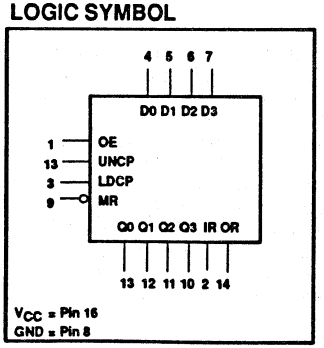
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

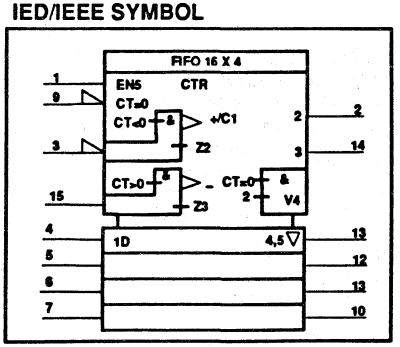
PIN CONFIGURATION



LOGIC SYMBOL



IED/IEEE SYMBOL



16X5 asynchronous FIFO (3–State) 74F225

FEATURES

- Independent synchronous inputs and outputs
- Organized as 16 words of 5 bits
- DC to 25MHz data rate
- 3–State outputs
- Cascadable in word–width and depth direction

DESCRIPTION

This 80–bit active element First–In–First–Out (FIFO) is a monolithic Schottky–clamped transistor–transistor logic (STTL) array organized as 16–words of 5–bits each. A memory system using the 'F225 can be easily expanded in multiples of 16–words of 5–bits as shown in Figure 1. The 3–State outputs controlled by a single enable input ($\overline{OE}$) make bus connection and multiplexing simple. The 'F225 processes data in a parallel format at any desired clock rate from DC to 25MHz. Status of the 'F225 is provided by three outputs, Input Ready (IR), Unload Clock Output (UNCPOUT) and Output Ready (OR). The data outputs are non–inverting with respect to the data inputs and are disabled when the $\overline{OE}$ input is High. When $\overline{OE}$ is Low, the data outputs are enabled to function as totem–pole outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F225	25MHz	65mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20–pin plastic DIP	N74F225N
20–pin plastic SOL	N74F225D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CPA, CPB	Load clock A and load clock B inputs	1.0/0.033	20µA/20µA
D0 – D4	Data inputs	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input (active–Low)	1.0/0.033	20µA/20µA
UNCPIN	Unload clock input	1.0/0.033	20µA/20µA
$\overline{MR}$	Master reset input (active–Low)	1.0/0.033	20µA/20µA
IR	Input ready output	50/33	1.0mA/20mA
UNCPOUT	Unload clock output (active–Low)	50/33	1.0mA/20mA
Q0 – Q4	Data outputs	150/40	3.0mA/24mA
OR	Output ready output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

RESET MODE

A High–to–Low transition on the Master Reset ($\overline{MR}$) input invalidates all data stored in the FIFO by clearing the control logic and setting OR Low. This High–to–Low transition on the $\overline{MR}$ input does not effect the data outputs but since OR is driven Low, it signifies invalid data on the outputs.

WRITE MODE

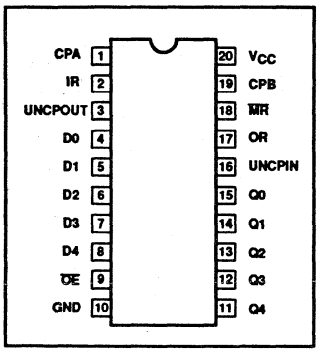
Data may be written into the array on the Low–to–High transition of either load clock (CPA or CPB) input. When writing data into the FIFO, one of the load clock inputs must be held High while the other strobes data into the FIFO. This arrangement allows either load clock to function as an inhibit for the other. Input Ready (IR) monitors the status of the last word location and signifies when the FIFO is full. This output is High whenever the FIFO is available to accept new data. The unload clock output (UNCPOUT) also monitors the last word location. This output generates a Low–logic–level pulse (synchronized to the internal clock pulse) when the last word location is vacant

READ MODE

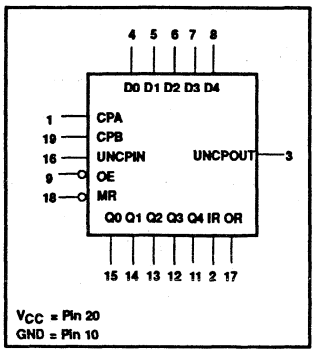
The Output Ready (OR) output is High when valid data is present on the data outputs. Data in the array is shifted on the Low–to–High transition of the Unload Clock Input (UNCPIN). In order for Output Ready (OR) to go High, Unload Clock Input (UNCPIN) must also be High.

16X5 asynchronous FIFO (3–State) 74F225

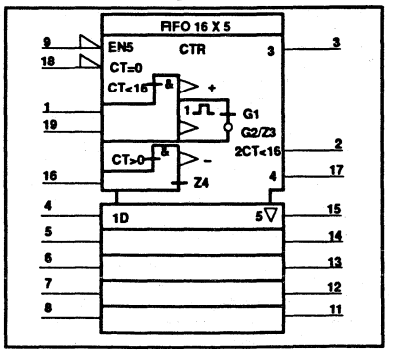
PIN CONFIGURATION



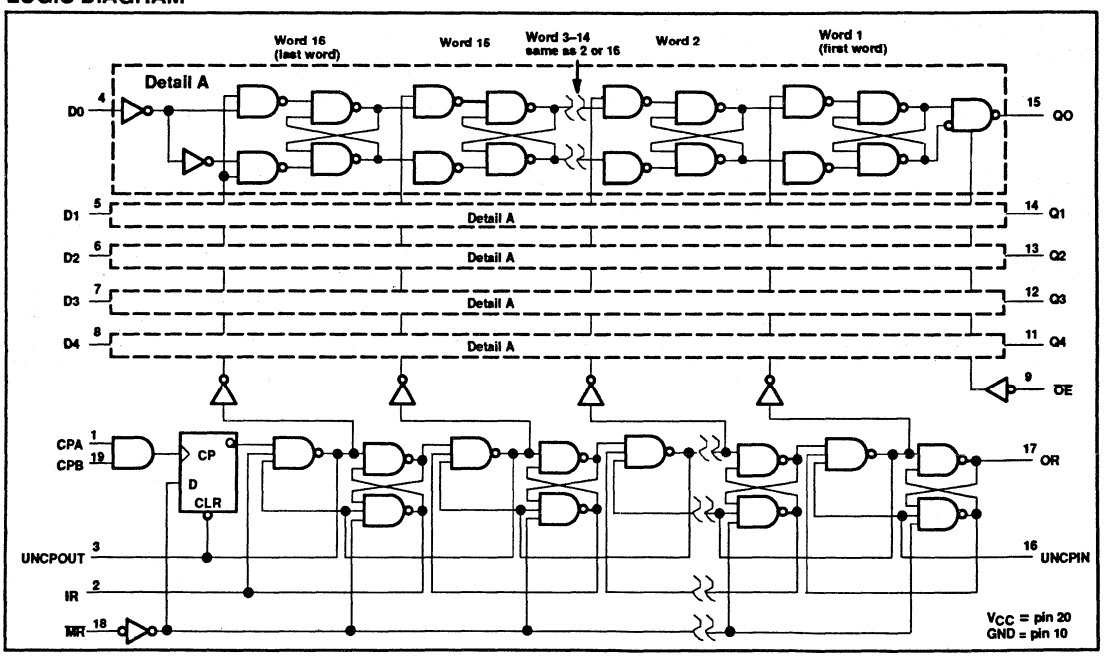
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	IR, OR, UNCPOUT	40	mA
	Current applied to output in Low output state	Data outputs	48	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current	IR, OR, UNCPOUT			–1	mA
		Data outputs			–3	mA
I_{OL}	Low–level output current	IR, OR, UNCPOUT			20	mA
		Data outputs			24	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	IR, OR, UNCPOUT	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
		Data outputs	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OZH}	Offset–output current, High–level voltage applied		V_{CC} = MAX, V_I = 2.7V				50	µA
I_{OZL}	Offset–output current, Low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			65	95	mA

NOTES:

4. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
5. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
6. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

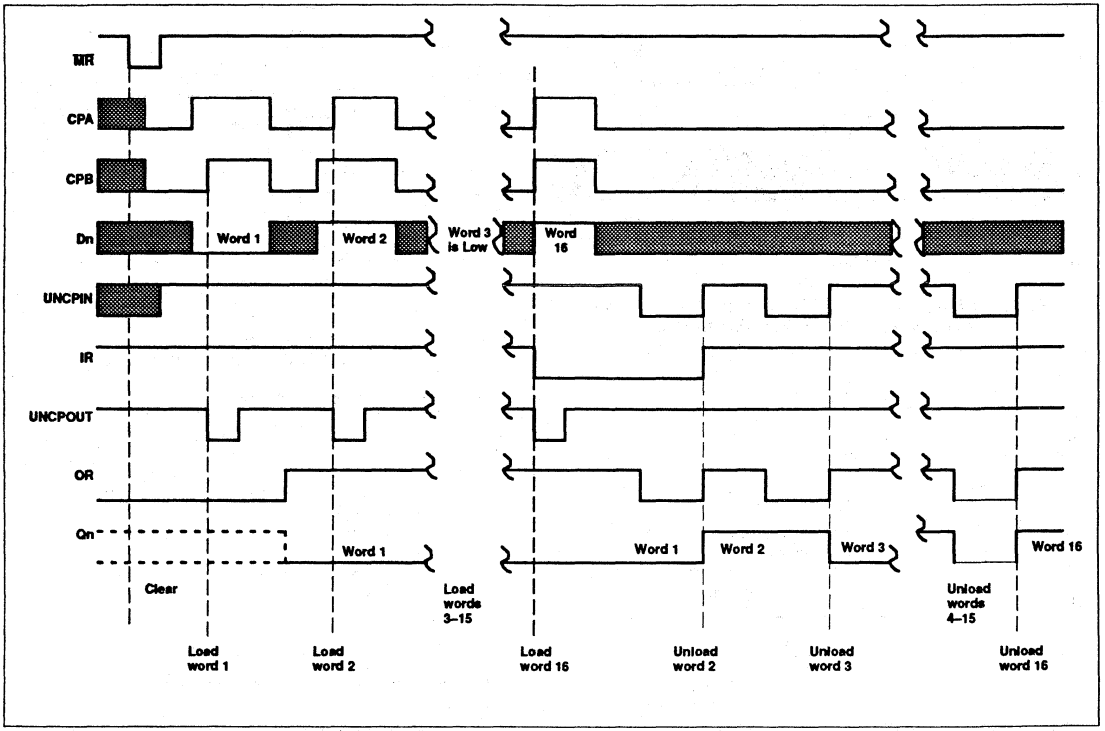
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency, Cascade mode	Waveform 2 and 3	25			25		MHz
t_{PLH} t_{PHL}	Propagation delay UNCPIN to Qn	Waveform 2	10.0 9.5	13.0 12.0	19.5 16.0	9.0 8.5	22.0 19.0	ns
t_{PLH} t_{PHL}	Propagation delay UNCPIN to OR	Waveform 2	16.0 6.0	20.0 8.5	25.0 11.0	14.0 5.0	29.0 12.0	ns
t_{SK}	Output skew Qn to OR ↑	Waveform 4	2.0		12.0	0.0	15.0	ns
t_{PLH}	Propagation delay UNCPIN to IR	Waveform 2	50	60	70	50	85	ns
t_{PLH}	Propagation delay CPA or CPB to OR	Waveform 4	55	65	75	50	90	ns
t_{PLH} t_{PHL}	Propagation delay CPA or CPB to UNCPOUT	Waveform 4	20.0 8.5	23.0 11.5	27.0 15.0	17.0 7.5	29.0 16.0	ns
$t_w(L)$	Pulse width, Low UNCPOUT	Waveform 4		12.0				ns
t_{PHL}	Propagation delay CPA or CPB to IR	Waveform 3	11.0	13.5	17.0	9.0	19.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to OR	Waveform 3	5.5	8.5	11.5	5.0	13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to IR	Waveform 3	2.0	4.0	7.0	1.5	7.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 5 Waveform 6	1.5 2.5	3.5 4.5	6.5 7.5	1.0 2.0	7.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 5 Waveform 6	1.5 2.0	3.5 4.0	7.0 7.0	1.0 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS

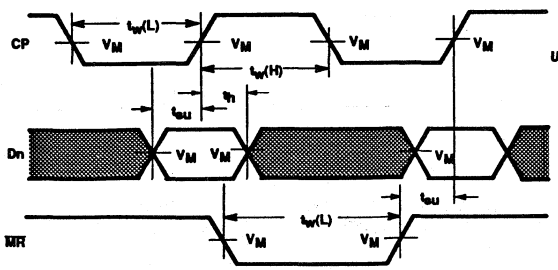
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CPA or CPB	Waveform 1	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CPA or CPB	Waveform 1	14.0 12.5			16.5 14.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CPA or CPB	Waveform 1	0.0			0.0		ns
$t_w(H)$ $t_w(L)$	CPA or CPB pulse width, High or Low	Waveform 1	6.5 3.0			8.5 3.5		ns
$t_w(L)$	UNCPIN pulse width, High or Low	Waveform 2	24.0 3.5			28.0 4.0		ns
$t_w(L)$	$\overline{MR}$ pulse width, Low	Waveform 1	3.5			4.5		ns

TYPICAL TIMING DIAGRAM

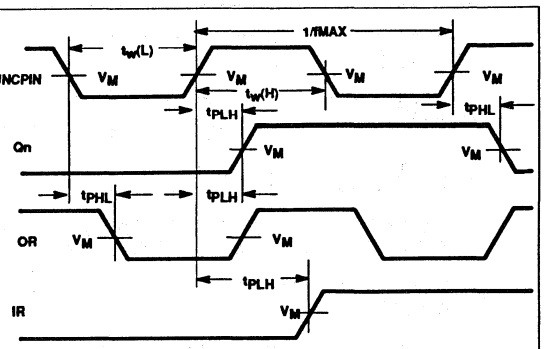


NOTE: Shaded areas Indicates irrelevant input conditions.

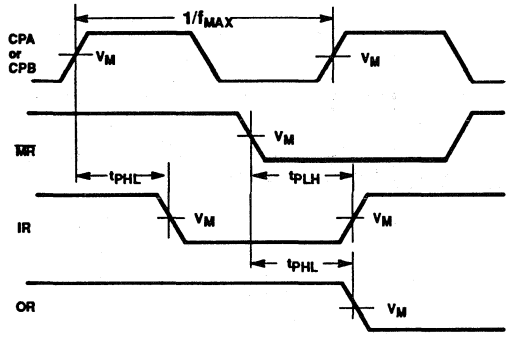
AC WAVEFORMS



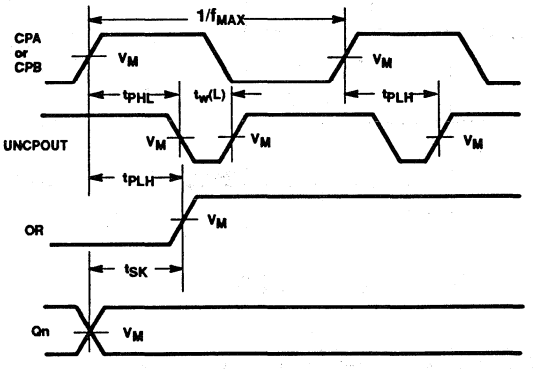
Waveform 1. $\overline{MR}$ and Clock Pulse Widths, Data Setup and Hold Times and $\overline{MR}$ to Clock Setup Time



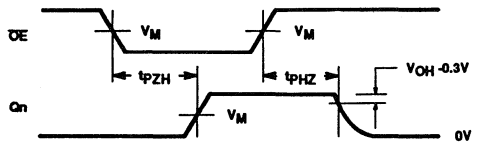
Waveform 2. UNCPIN to Output Delays



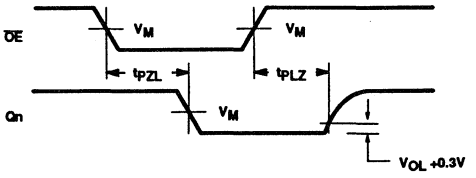
Waveform 3. CPA or CPB to IR Delay and $\overline{MR}$ to IR and OR Delay



Waveform 4. CPA or CPB to UNCPOUT and OR Delay, UNCPOUT Pulse Width and Qn to OR Skew



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION

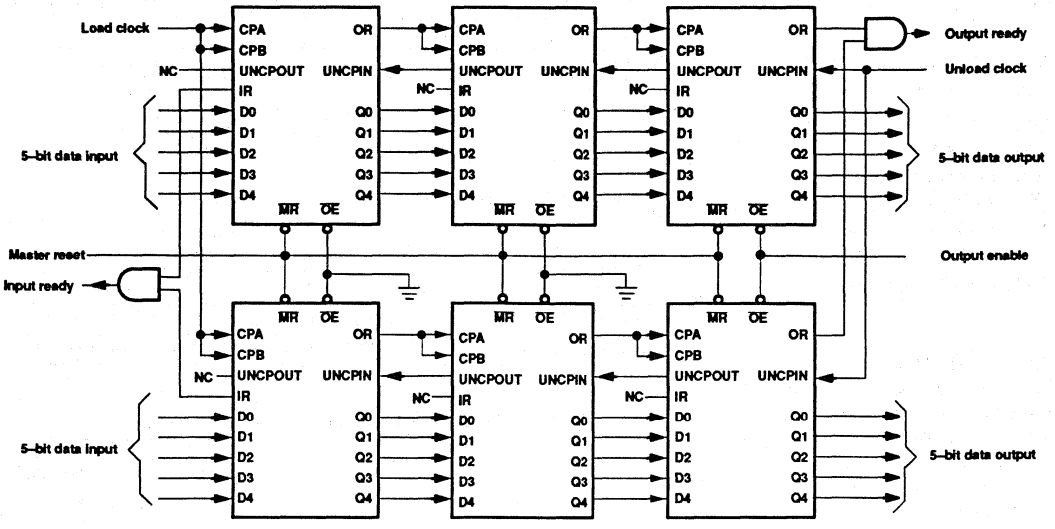
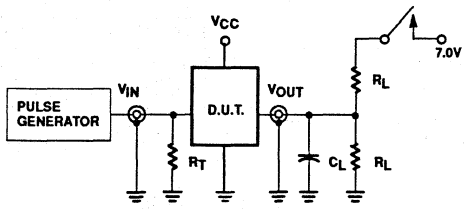


Figure 1. Expanding the 74F225 FIFO (48 words of 10 bits)

TEST CIRCUIT AND WAVEFORM



Test circuit for 3–state outputs

SWITCH POSITION

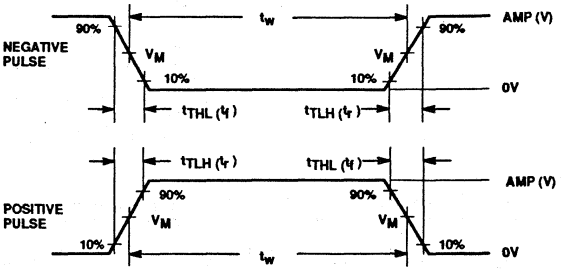
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Buffers

74F240/74F240A
74F241/74F241A

74F240/240A Octal inverter buffer (3–state)
74F241/241A Octal buffer (3–state)

FEATURES

- Octal bus interface
- 3–state buffer outputs sink 64mA
- 15mA source current
- Guaranteed output skew less than 2.0ns (74F240A/74F241A)
- Reduced ground bounce (74F240A/74F241A)
- Reduced I_{CC} (74F241A only)
- Reduced loading (74F240A I_{IL} = 100μA, 74F241A I_{IL} = 40μA)

DESCRIPTION

The 74F240 and 74F241 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA. The device features two output enables, each controlling four of the 3–state outputs.

The 74F240A and 74F241A are functionally equivalent to their non–A counterparts. They have been designed to reduce effects of ground noise. Other advantages are noted in the features.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F240	4.3ns	37mA
74F240A	3.8ns	40mA
74F241	5.0ns	53mA
74F241A	4.5ns	32mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20–pin plastic DIP	N74F240N, N74F240AN, N74F241N, N74F241AN
20–pin plastic SOL	N74F240D, N74F240AD, N74F241D, N74F241AD

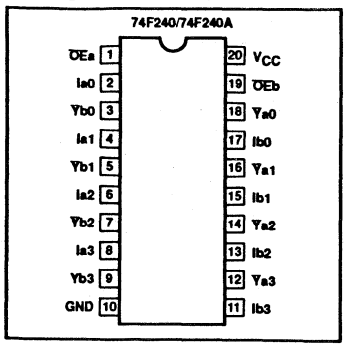
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs (74F240)	1.0/1.67	20μA/1.0mA
	Data inputs (74F240A)	1.0/0.167	20μA/100μA
	Data inputs (74F241)	1.0/2.67	20μA/1.6mA
	Data inputs (74F241A)	1.0/0.067	20μA/40μA
$\overline{OE}$a, $\overline{OE}$b	Output enable inputs (active low) (74F240)	1.0/0.33	20μA/0.2mA
	Output enable inputs (active low) (74F240A)	1.0/0.167	20μA/100μA
$\overline{OE}$a, OEb	Output enable input (74F241)	1.0/1.67	20μA/1.0mA
	Output enable input (74F241A)	1.0/0.067	20μA/40μA
Yan, Ybn	Data outputs (74F241, 74F241A)	750/106.7	15mA/64mA
$\overline{Y}$an, $\overline{Y}$bn	Data outputs (74F240, 74F240A)	750/106.7	15mA/64mA

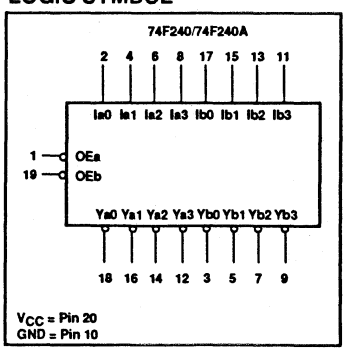
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

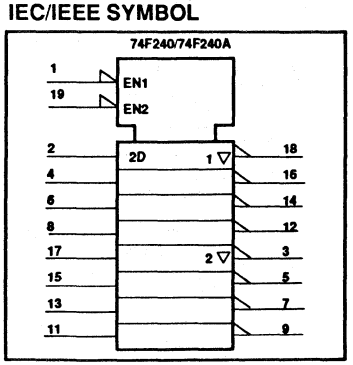
PIN CONFIGURATION



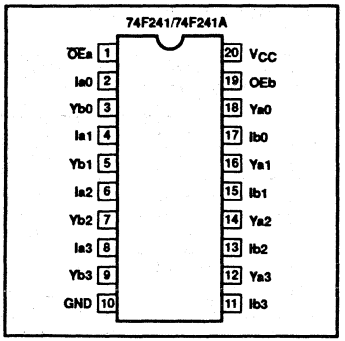
LOGIC SYMBOL



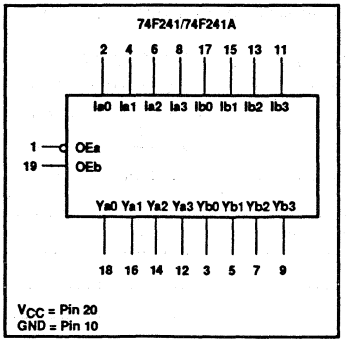
IEC/IEEE SYMBOL



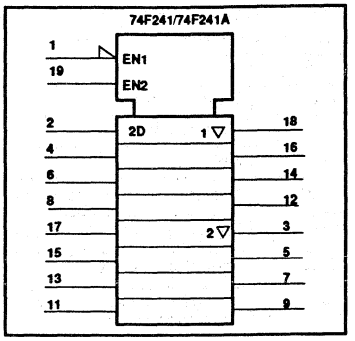
PIN CONFIGURATION



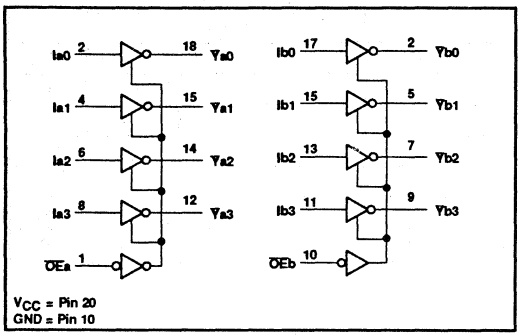
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM FOR 74F240/74F240A



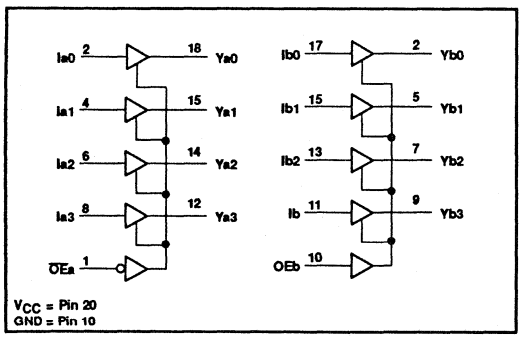
FUNCTION TABLE FOR 74F240/74F240A

INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	$\overline{OEb}$	Ib	Ya	Yb
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

Notes to function table for 74F240/74F240A

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

LOGIC DIAGRAM FOR 74F241/74F241A



FUNCTION TABLE FOR 74F241/74F241A

INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

Notes to function table for 74F241/74F241A

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	128	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High–level output current			–15	mA
I_{OL}	Low–level output current			64	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}			0.50	V
			V_{IH} = MIN,		±5%V_{CC}		0.42	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	74F240 all inputs	V_{CC} = MAX, V_I = 0.5V					–1.0	mA
		74F240A all inputs						–100	µA
		74F241 $\overline{OE}$a, OEb						–1.0	mA
		74F241 Ian, Ibn						–1.6	mA
		74F241A all inputs						–40	µA
I_{OZH}	Off–state output current, high–level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F240	I_{CCH}	V_{CC} = MAX			12	18	mA
			I_{CCL}				50	70	mA
			I_{CCZ}				35	45	mA
		74F240A	I_{CCH}				28	37	mA
			I_{CCL}				58	75	mA
			I_{CCZ}				34	50	mA
		74F241	I_{CCH}	V_{CC} = MAX			40	60	mA
			I_{CCL}				60	90	mA
			I_{CCZ}				65	90	mA
		74F241A	I_{CCH}				20	30	mA
			I_{CCL}				49	65	mA
			I_{CCZ}				26	40	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

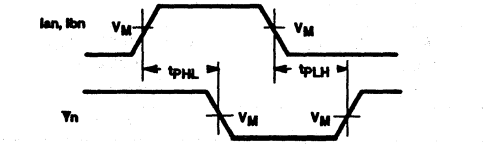
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to $\overline{Y}$n	74F240	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	3.0 4.5	5.0 6.5	7.5 8.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	3.0 3.0	5.5 5.0	7.0 7.0	3.0 3.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to $\overline{Y}$n	74F240A	Waveform 1	2.5 2.0	4.0 3.5	5.5 5.5	2.0 2.0	6.5 6.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	2.0 3.5	4.0 5.0	6.5 7.5	2.0 3.0	7.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.5	3.5 2.5	6.0 5.0	1.5 1.0	6.5 5.5	ns
$t_{sk(0)}$	Output skew[1,2]		Waveform 5			1.5		2.0	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	74F241	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	74F241A	Waveform 2	2.5 2.5	4.5 4.5	5.8 5.8	2.5 2.5	6.5 6.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	2.5 3.5	4.5 5.0	6.0 7.0	2.0 3.0	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	6.0 5.5	1.5 1.0	6.5 6.0	ns
$t_{sk(0)}$	Output skew[1,2]		Waveform 5			1.5		2.0	ns

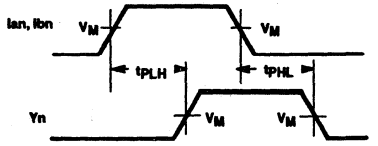
Notes to AC electrical characteristics

1. $|t_{PN}$ actual – t_{PM} actual| for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

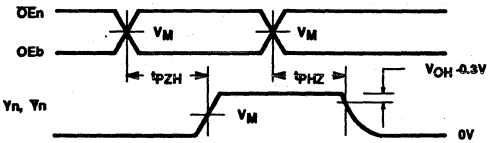
AC WAVEFORMS



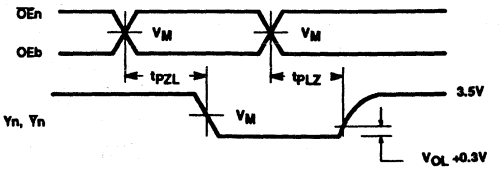
Waveform 1. Propagation delay for inverting outputs



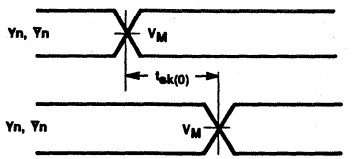
Waveform 2. Propagation delay for non–inverting outputs



Waveform 3. 3-state output enable time to high level and output disable time from high level



Waveform 4. 3-state output enable time to low level and output disable time from low level



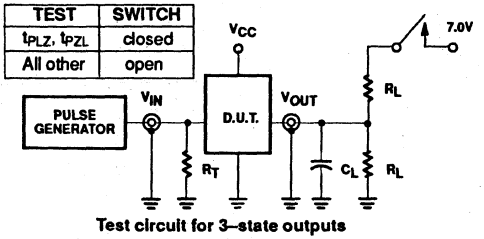
Waveform 5. Output skew

Notes to AC waveforms
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



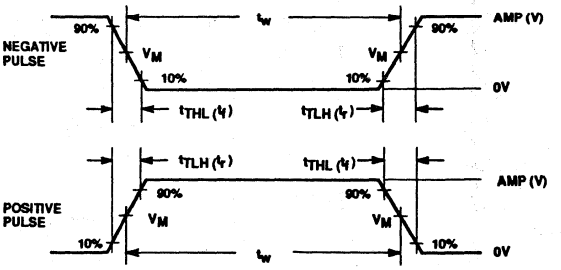
Test circuit for 3–state outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0356
ECN No.	00285
Date of issue	August 31, 1990
Status	Product Specification
FAST Products	

FAST 74F242, 74F243 Transceivers

74F242 Quad Transceiver, Inverting (3-State)
74F243 Quad Transceiver (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F242	4.3ns	31.2mA
74F243	4.0ns	66mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F242N, N74F243N
14-Pin Plastic SO	N74F242D, N74F243D

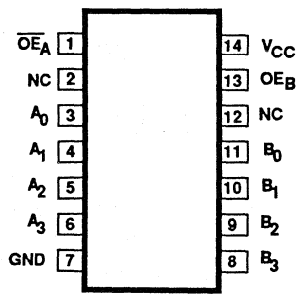
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs ('F242)	3.5/1.67	70μA/1.0mA
A_n, B_n	Data inputs ('F243)	3.5/2.67	70μA/1.6mA
$\overline{OE}_A$	Output enable input (active Low)	1.0/1.67	20μA/1.0mA
OE_B	Output enable input	1.0/1.67	20μA/1.0mA
A_n, B_n	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

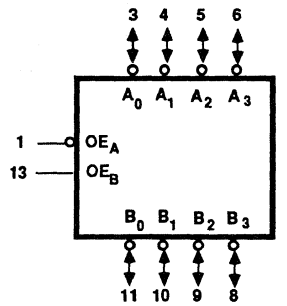
74F242



TOP VIEW

LOGIC SYMBOL

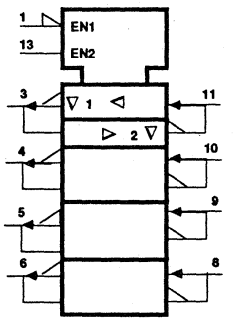
74F242



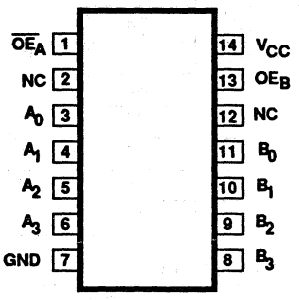
V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL(IEEE/IEC)

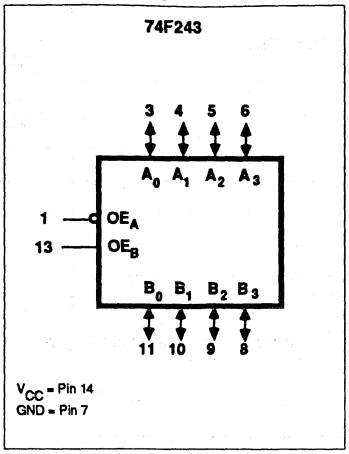
74F242



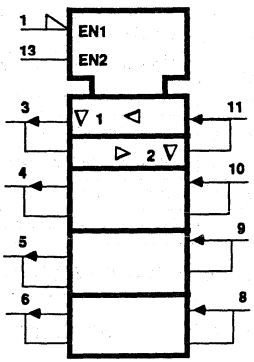
PIN CONFIGURATION



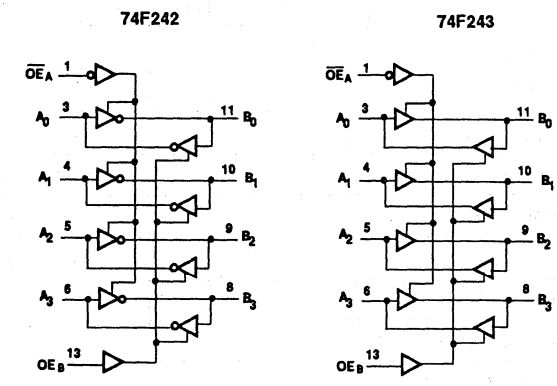
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE, 74F242

INPUTS		OUTPUTS	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	$B=\overline{A}$
H	L	Z	Z
L	H	a	a
H	H	$A=\overline{B}$	INPUT

FUNCTION TABLE, 74F243

INPUTS		OUTPUTS	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	B=A
H	L	Z	Z
L	H	a	a
H	H	A=B	INPUT

H = High voltage level
L = Low voltage level
Z = High impedance "off" state
a = This condition is not allowed due to excessive currents

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.0	3.2		V
					±5%V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} =MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	A_0-A_3, B_0-B_3	V_{CC} =MAX, V_I = 5.5V					1	mA
		$\overline{OE}_A$, OE_B	V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	$\overline{OE}_A$, OE_B only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-1	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	'F242	V_{CC} = MAX, V_O= 0.5V					-1.0	mA
		'F243						-1.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F242 I_{CCH}	V_{CC} = MAX				22	35	mA
		'F242 I_{CCL}					40	55	mA
		'F242 I_{CCZ}					32	45	mA
		'F243 I_{CCH}	V_{CC} = MAX				64	80	mA
		'F243 I_{CCL}					64	90	mA
		'F243 I_{CCZ}					71	90	mA

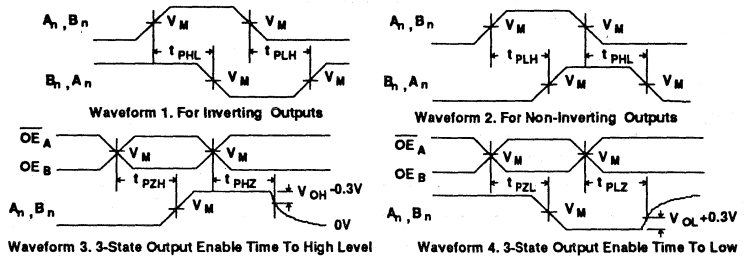
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	74F242	Waveform 1	2.5 2.0	3.5 3.0	6.0 4.5	2.5 2.0	7.0 4.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 3.5	4.0 6.5	7.0 9.0	3.0 3.5	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	3.5 3.5	5.5 6.0	8.5 9.5	3.5 3.5	9.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	74F243	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.5 5.0	5.7 7.5	2.0 2.0	6.7 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.5	6.0 6.0	2.0 2.0	7.0 7.0	ns

AC WAVEFORMS



Waveform 1. For Inverting Outputs

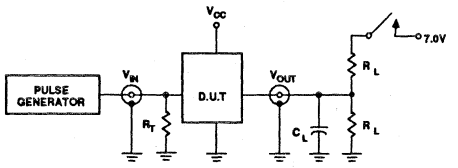
Waveform 2. For Non-Inverting Outputs

Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

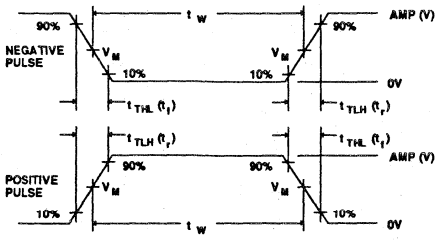
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal buffers (3-State) — 74F244/74F244B

FEATURES

- Octal bus interface
- 3–State output buffer sink 64mA
- 15mA source current
- Guaranteed output skew less than 2.0ns (74F244B)
- Reduced ground bounce (74F244B)
- Reduced I_{CC} (74F244B)
- Reduced loading (74F244B I_{IL} = 40μA)
- Split lead frame offers increased noise immunity (74F244B)
- Industrial temperature range available (–40°C to +85°C) for 74F244

DESCRIPTION

The 74F244 is an octal buffer that is ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two output enables, $\overline{OE}a$ and $\overline{OE}b$, each controlling four of the 3–State outputs.

The 74F244B is functionally equivalent to the 74F244. It has been designed to reduce effects of ground noise. Other advantages are noted in the features.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F244	4.0ns	53mA
74F244B	4.0ns	33mA

ORDERING INFORMATION

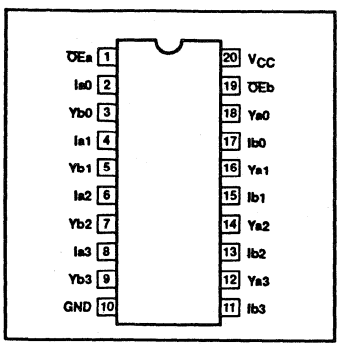
DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
20–pin plastic DIP	N74F244N, N74F244BN	I74F244N
20–pin plastic SOL	N74F244D, N74F244BD	I74F244D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

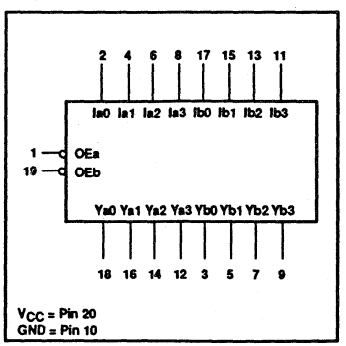
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs (74F244)	1.0/2.67	20μA/1.6mA
	Data inputs (74F244B)	1.0/0.067	20μA/40μA
$\overline{OE}a$, $\overline{OE}b$	Output enable inputs (active low) (74F244)	1.0/1.67	20μA/1.0mA
	Output enable inputs (active low) (74F244B)	1.0/0.067	20μA/40μA
Yan, Ybn	Data outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

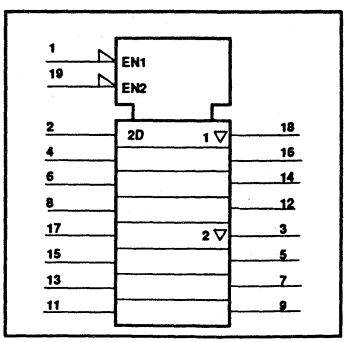
PIN CONFIGURATION



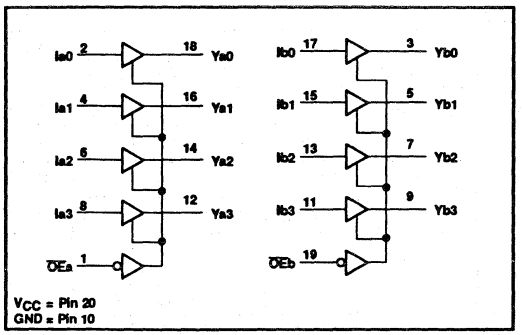
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	Ya	Yb
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

NOTES:
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		128	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range ('F244 only)	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current				–15	mA
I_{OL}	Low–level output current				64	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range ('F244 only)	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.5			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = –15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}			0.55	V
				V_{IH} = MIN,		±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	74F244 $\overline{OE}$a, $\overline{OE}$b		V_{CC} = MAX, V_I = 0.5V					–1.0	mA
		74F244 Ian, Ibn							–1.6	mA
		74F244B all inputs							–40	µA
I_{OZH}	Off–state output current, high–level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied			V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short–circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F244	I_{CCH}	V_{CC} = MAX				40	60	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					60	90	mA
		74F244B	I_{CCH}	V_{CC} = MAX				20	30	mA
			I_{CCL}					50	70	mA
			I_{CCZ}					29	40	mA

NOTES:

3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
4. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F244

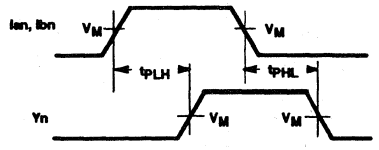
SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	Waveform 1	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	1.5 2.0	7.0 7.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low	Waveform 3 Waveform 4	2.0 2.0	4.3 5.0	5.7 7.0	2.0 2.0	6.7 8.0	2.0 2.0	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low	Waveform 3 Waveform 4	1.5 1.5	2.5 2.5	5.5 5.5	1.0 1.0	6.0 5.5	1.0 1.0	6.0 5.5	ns

AC ELECTRICAL CHARACTERISTICS FOR 74F244B

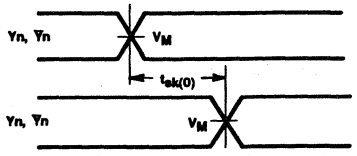
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	Waveform 1	2.5 2.5	4.5 4.5	5.7 6.0	2.0 2.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	Waveform 3 Waveform 4	2.0 3.0	4.0 5.5	6.0 7.5	2.0 3.0	6.5 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 3 Waveform 4	1.5 1.5	2.5 2.5	5.5 5.5	1.0 1.0	6.0 5.5	ns
$t_{sk(0)}$	Output skew[1, 2]	Waveform 2			1.5		2.0	ns

NOTES:
1. $|t_{PN}$ actual – t_{PM} actual| for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

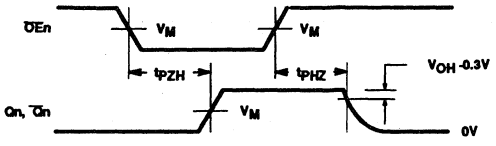
AC WAVEFORMS



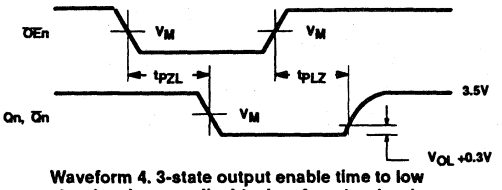
Waveform 1. Propagation delay for data to outputs



Waveform 2. Output skew



Waveform 3. 3-state output enable time to high level and output disable time from high level



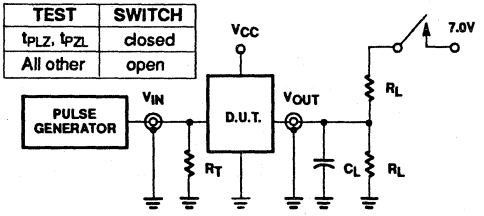
Waveform 4. 3-state output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



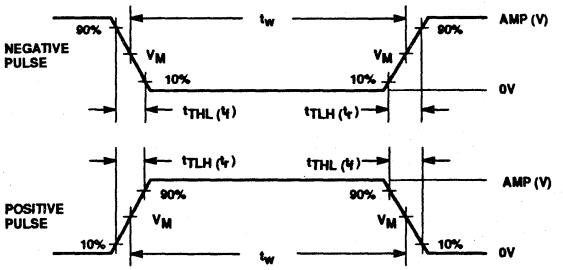
Test circuit for 3-State outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0025
ECN No.	95304
Date of issue	December 8, 1988
Status	Product Specification
FAST Products	

FAST 74F245 Transceiver

Octal Transceiver (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F245	4.0ns	70mA

FEATURES

- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 64mA**
- **15 mA source current**
- **Outputs are placed in high impedance state during power-off conditions**

DESCRIPTION

The 74F245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing 15mA, producing very good capacitive drive characteristics.The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive($T/\overline{R}$) input for direction control. The 3-state outputs, B_0-B_7, have been designed to prevent output bus loading if the power is removed from the device.

ORDERING INFORMATION

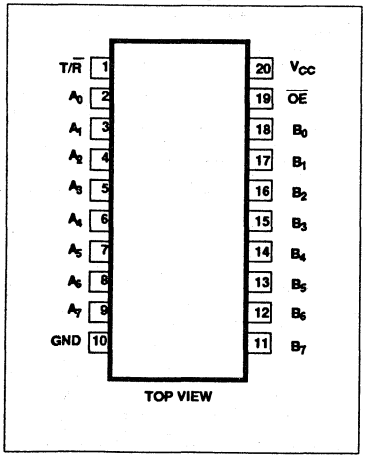
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F245N
20-Pin Plastic SOL	N74F245D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

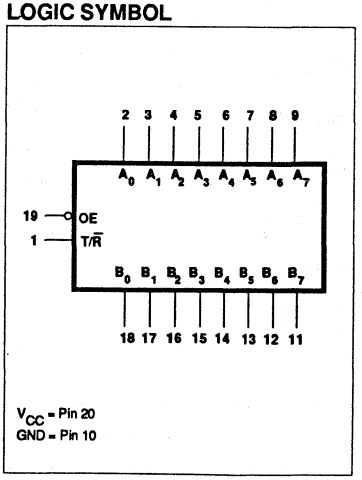
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	3.5/1.0	70μA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/2.0	20μA/1.2mA
$T/\overline{R}$	Transmit/Receive input	1.0/2.0	20μA/1.2mA
A_0- A_7	A port outputs	150/40	3.0mA/24mA
B_0- B_7	B Port outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

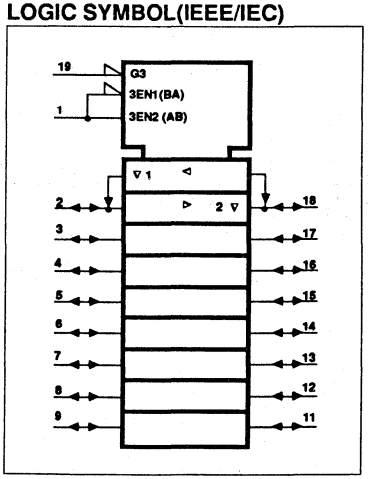
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

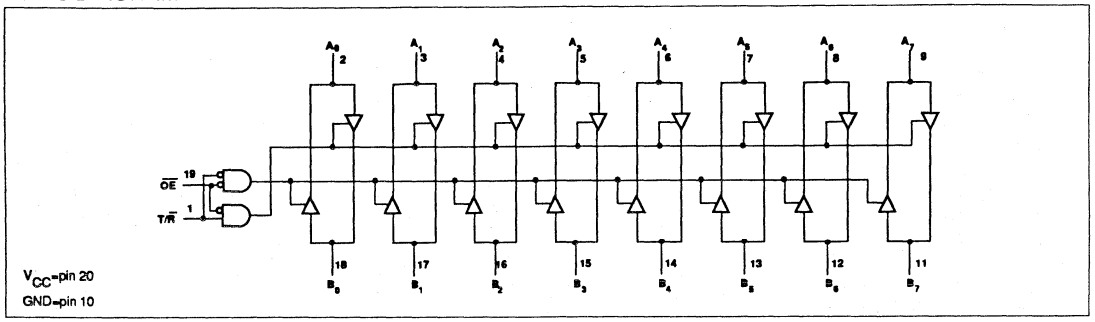


FUNCTION TABLE

INTPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=20mA	±10%V_{CC}		0.30	0.50	V
				I_{OL}=24mA	±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					-1.2	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				60	87	mA
		I_{CCL}					70	100	mA
		I_{CCZ}					75	110	mA

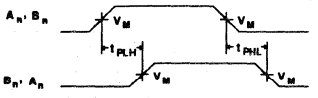
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

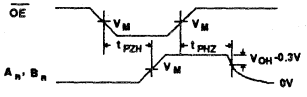
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.5 2.5	3.5 4.0	6.0 6.0	2.5 2.5	7.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.0 3.5	4.5 5.5	7.0 8.0	2.0 3.5	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 1.0	5.0 3.5	6.5 6.0	2.0 1.0	7.5 7.0	ns

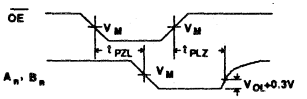
AC WAVEFORMS



Waveform 1. Propagation Delay For Non-Inverting Output



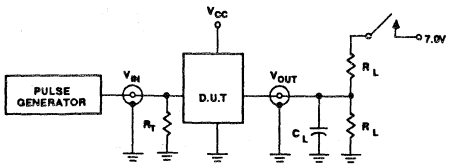
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

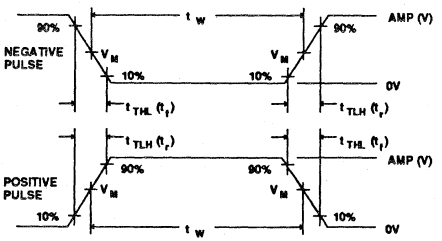
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0358
ECN No.	99143
Date of issue	March 19, 1990
Status	Product Specification
FAST Products	

FAST 74F251, 74F251A Multiplexers

74F251 8-Input Multiplexer (3-State)
74F251A 8-Input Multiplexer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F251	5.5ns	15mA
74F251A	4.5ns	19mA

FEATURES

- **High speed 8-to-1 multiplexing**
- **On chip decoding**
- **Multifunction capability**
- **Inverting and Non-inverting outputs**
- **Both outputs are 3-state for further multiplexer expansion**

DESCRIPTION

The 74F251 and 74F251A are logic implementation of a single 8- position switch with the switch position controlled by the state of three Select (S_0,S_1,S_2) inputs. True(Y) and complementary ($\overline{Y}$) outputs are both provided. The output Enable ($\overline{OE}$) is active Low. When $\overline{OE}$ is High, both outputs are in high impedance state, allowing multiple output connections to a common bus without driving nor loading the bus significantly. All but one device must be in high impedance state to avoid high currents that would exceed the maximum ratings when the outputs of the 3-state devices are tied together. When the output of more than one device is tied together the user must ensure that there is no overlap in the active Low portion of the output enable voltages.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F251N, N74F251AN
16-Pin Plastic SO	N74F251D, N74F251AD

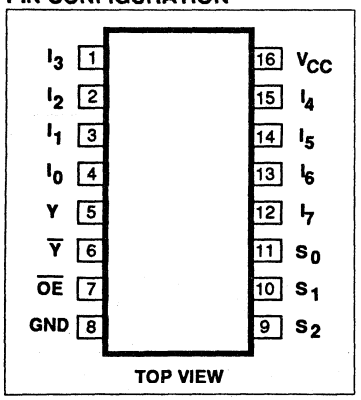
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0-I_7	Data inputs	1.0/1.0	20µA/0.6mA
S_0-S_2	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Y, $\overline{Y}$	Data outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

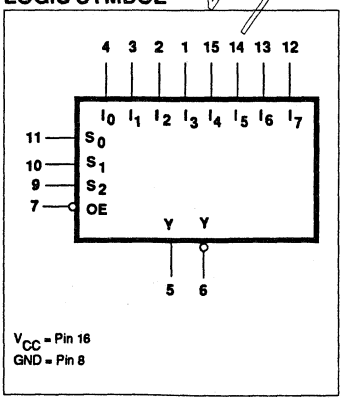
74F251A is the faster version of 74F251.

PIN CONFIGURATION

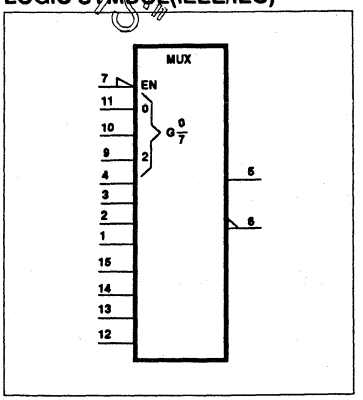


TOP VIEW

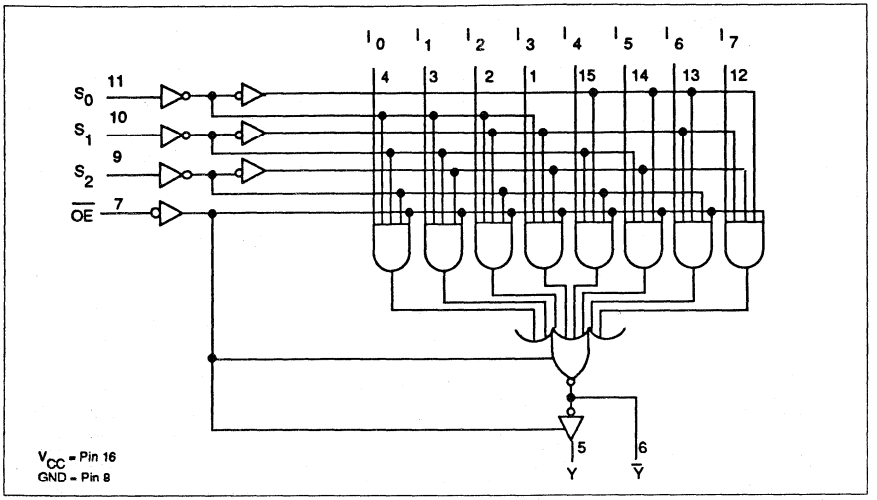
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_I = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_I = 0.5V				-50	µA
I_{OS}	Short-circuitoutput current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F251	V_{CC} = MAX			14	22	mA
		I_{CCL}					14	22	mA
		I_{CCZ}					16	24	mA
		I_{CCH}	74F251A	V_{CC} = MAX			20	27	mA
		I_{CCL}					17	24	mA
		I_{CCZ}					21	29	mA

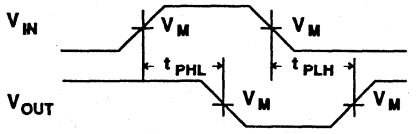
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

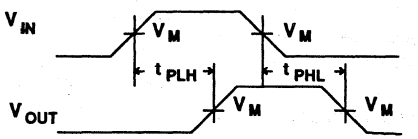
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F251	Waveform 2	3.0 3.0	4.0 4.5	6.0 6.5	2.5 3.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$		Waveform 1	2.5 1.0	4.0 2.0	6.0 4.0	2.0 1.0	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y		Waveform 1, 2	4.0 4.0	7.0 7.0	9.5 9.0	3.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$		Waveform 1, 2	3.5 1.5	6.0 5.0	9.0 7.5	3.5 1.5	10.0 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Y		Waveform 3 Waveform 4	4.0 4.0	6.5 5.5	10.0 8.0	4.0 3.5	11.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Y		Waveform 3 Waveform 4	2.5 3.0	4.0 4,0	6.5 6.5	2.0 2.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{Y}$		Waveform 3 Waveform 4	4.0 4.0	5.5 5.5	8.0 8.0	3.5 3.5	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to $\overline{Y}$		Waveform 3 Waveform 4	2.5 2.0	4.0 4.0	6.0 6.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F251A	Waveform 2	3.0 3.0	5.0 5.0	7.0 7.0	2.5 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$		Waveform 1	2.5 1.0	4.5 2.5	7.0 5.0	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y		Waveform 1, 2	4.5 4.0	6.5 5.5	10.0 9.0	4.0 3.5	11.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$		Waveform 1, 2	3.5 2.5	6.0 4.5	9.0 7.0	3.5 2.5	9.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Y		Waveform 3 Waveform 4	3.5 3.5	5.5 5.0	7.5 7.5	3.0 3.0	8.5 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Y		Waveform 3 Waveform 4	2.5 1.0	4.0 4.0	6.5 6.0	2.0 1.0	7.0 6.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{Y}$		Waveform 3 Waveform 4	2.5 2.5	4.0 4.0	6.5 6.5	2.0 2.5	7.0 7.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to $\overline{Y}$		Waveform 3 Waveform 4	3.5 1.0	5.0 2.0	7.5 4.5	3.0 1.0	8.0 4.5	ns

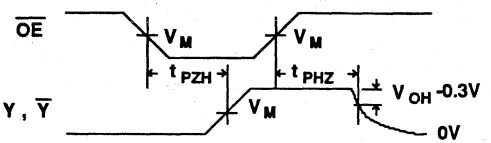
AC WAVEFORMS



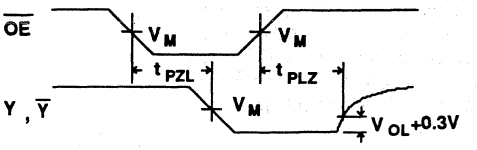
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs

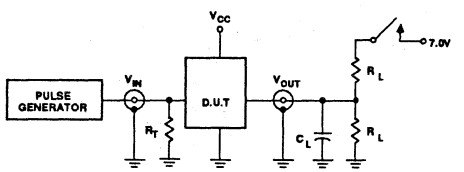


Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

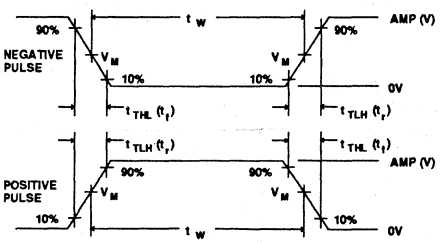
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0101
ECN No.	95206
Date of issue	November 29, 1988
Status	Product Specification
FAST Products	

FAST 74F253 Multiplexer

Dual 4-Input Multiplexer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F253	7.0ns	12mA

FEATURES

- **3-state outputs for bus interface and multiplex expansion**
- **Common select inputs**
- **Separate Output Enable inputs**

DESCRIPTION

The 74F253 has two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common Select inputs (S_0,S_1). When the individual Output Enable ($\overline{OE}_a$,$\overline{OE}_b$) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance (Hi-Z) state.

The 'F253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two common Select inputs.

To avoid exceeding the maximum current ratings when the outputs of the 3-state devices are tied together, all but one device must be in the high-impedance state. Therefore, only one Output Enable must be active at a time.

ORDERING INFORMATION

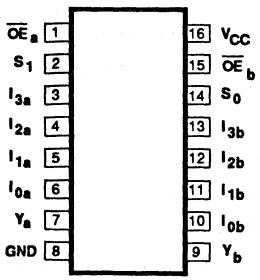
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F253N
16-Pin Plastic SO	N74F253D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

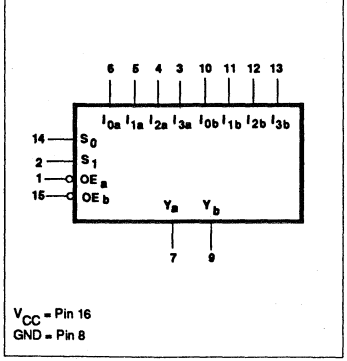
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}- I_{3a}	Port A data inputs	1.0/1.0	20µA/0.6mA
I_{0b}- I_{3b}	Port B data inputs	1.0/1.0	20µA/0.6mA
S_0, S_1	Common Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}_a$	Port A Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_b$	Port B Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Y_a, Y_b	3-state outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

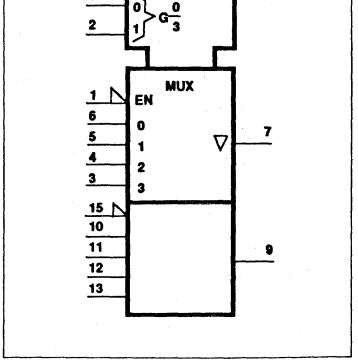
PIN CONFIGURATION



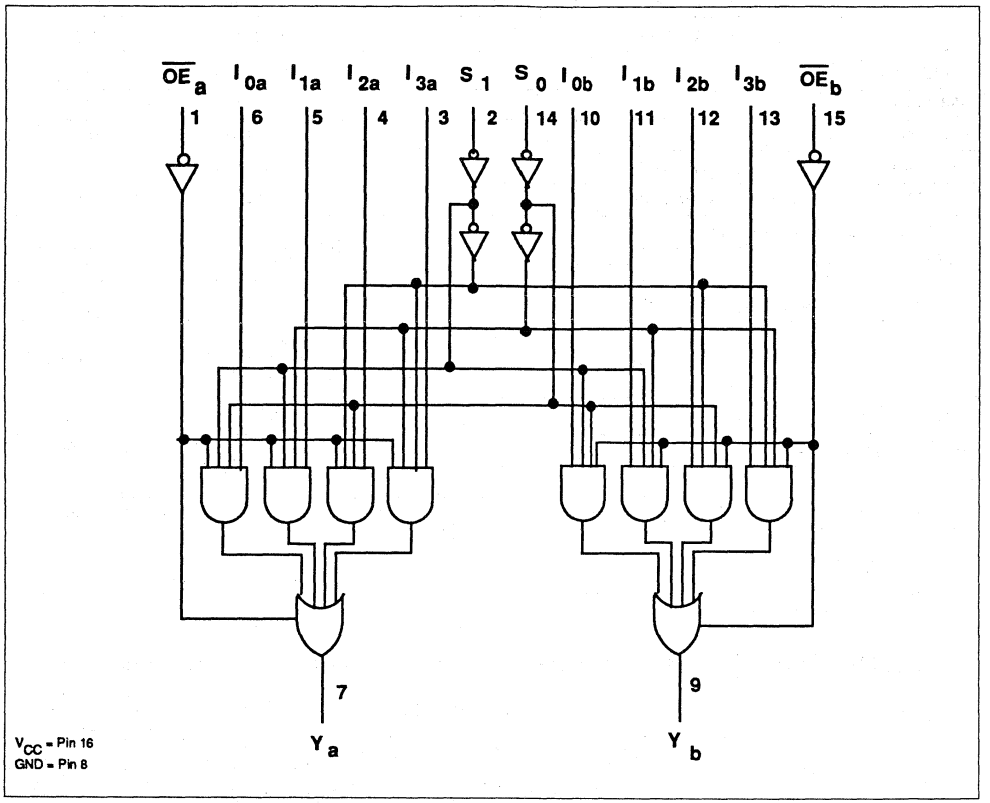
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{OE}_n$=GND, S_n=I_n=4.5V		10	16	mA
		I_{CCL}		$\overline{OE}_n$=S_n=I_n=GND		12	23	mA
		I_{CCZ}		$\overline{OE}_n$=4.5V, S_n=I_n=GND		14	23	mA

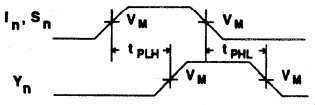
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

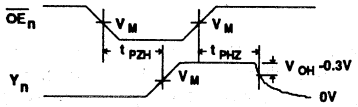
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.0	3.0 3.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 1	4.5 5.0	7.5 8.5	10.5 11.0	4.5 4.5	11.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	3.0 3.0	6.5 6.5	8.0 8.0	3.0 3.0	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 2.0	3.5 3.0	5.0 5.0	2.0 1.5	6.0 6.0	ns

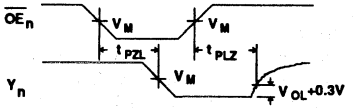
AC WAVEFORMS



Waveform 1. Propagation Delay, Data and Select to Output



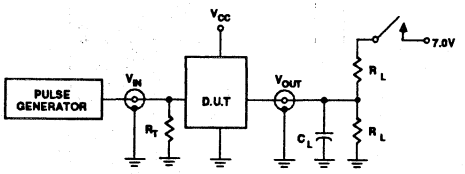
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

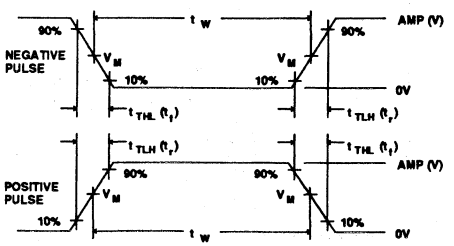
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0359
ECN No.	95207
Date of issue	November 29, 1988
Status	Product Specification
FAST Products	

FAST 74F256 Latch

Dual Addressable Latch

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F256	7.0ns	28mA

FEATURES

- **Combines dual demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common reset input**
- **Useful as dual 1-of-4 active-High decoder**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F256N
16-Pin Plastic SO	N74F256D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

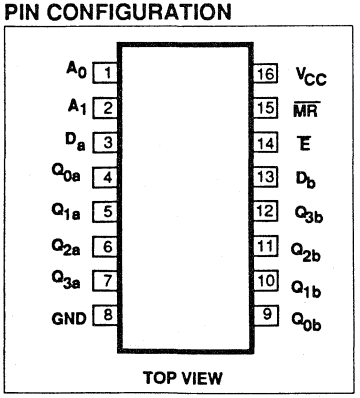
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_a, D_b	Port A, port B inputs	1.0/1.0	20µA/0.6mA
A_0, A_1	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable (active Low)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset inputs (active Low)	1.0/1.0	20µA/0.6mA
Q_{0a} - Q_{3a}	Port A outputs	50/33	1.0mA/20mA
Q_{0b} - Q_{3b}	Port B outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

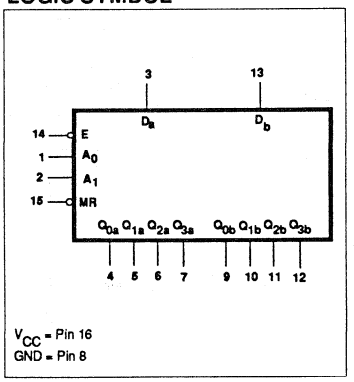
The 74F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset ($\overline{MR}$) and Enable ($\overline{E}$) inputs (see Function Table). In the addressable latch mode, data at the Data inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states. and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held High (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR}$=$\overline{E}$=Low), addressed outputs will follow the level of the Data inputs, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

PIN CONFIGURATION

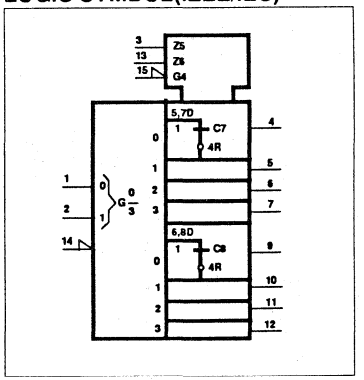


TOP VIEW

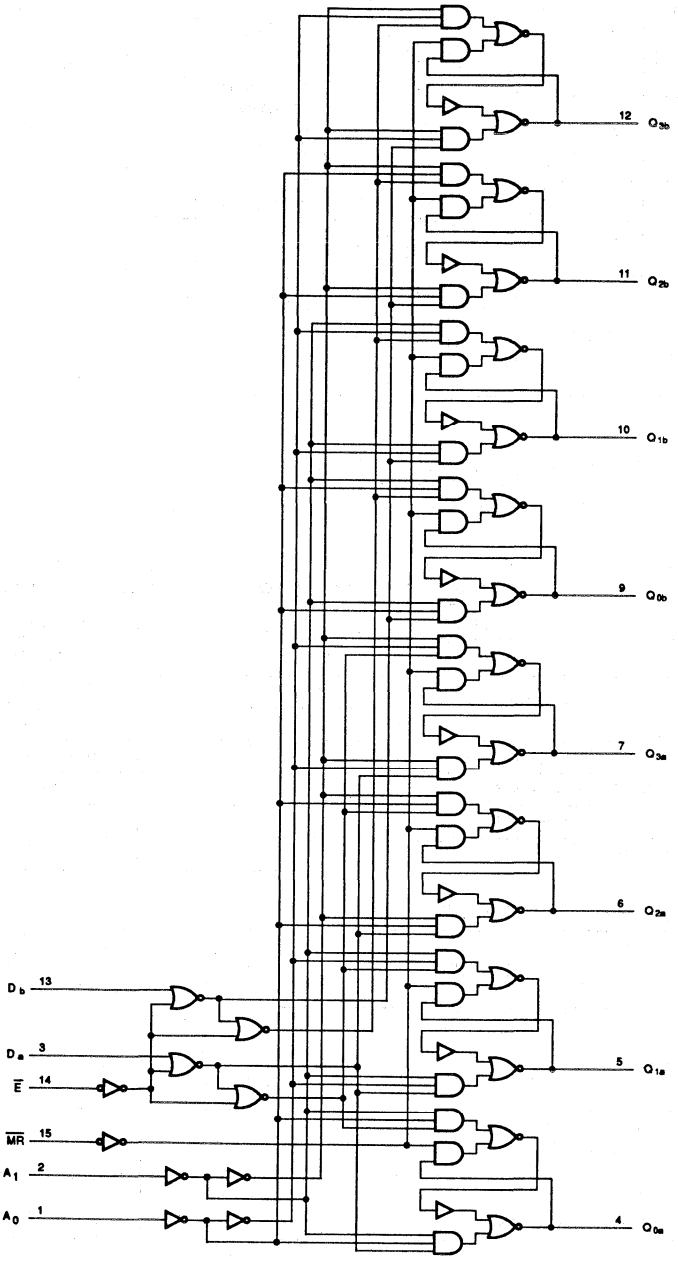
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS					OUTPUTS				OPERATING MODE
$\overline{MR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	
L	H	X	X	X	L	L	L	L	Master Reset
L	L	d	L	L	Q=d	L	L	L	Demultiplex (active-High decoder when D=H)
L	L	d	H	L	L	Q=d	L	L	
L	L	d	L	H	L	L	Q=d	L	
L	L	d	H	H	L	L	L	Q=d	
H	H	X	X	X	q_0	q_1	q_2	q_3	Store (do nothing)
H	L	d	L	L	Q=d	q_1	q_2	q_3	Addressable Latch
H	L	d	H	L	q_0	Q=d	q_2	q_3	
H	L	d	L	H	q_0	q_1	Q=d	q_3	
H	L	d	H	H	q_0	q_1	q_2	Q=d	

H = High voltage level
L = Low voltage level
X = Don't care
d = High or Low data one setup time prior to the Low-to-High Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			21	42	mA
		I_{CCL}				33	60	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	4.0 3.0	7.0 5.0	9.5 7.0	4.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 3	5.0 4.5	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 4	5.0	7.0	9.0	4.5	10.0	ns

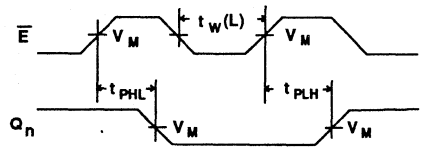
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{E}$	Waveform 5	3.0 6.5			3.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{E}$	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to $\overline{E}$[1]	Waveform 6	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to $\overline{E}$[2]	Waveform 6	0 0			0 0		ns
$t_w(L)$	$\overline{E}$ Pulse width, Low	Waveform 1	7.5			8.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 4	3.0			3.0		ns

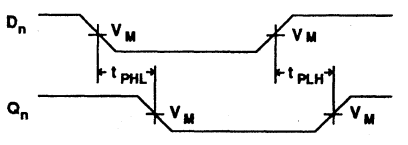
NOTES:

1. The Address to Enable setup time is the time before the High-to -Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time before the Low-to -High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

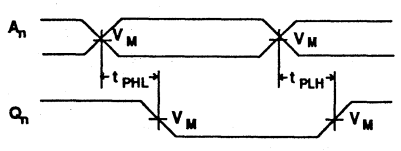
AC WAVEFORMS



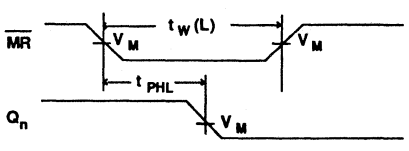
Waveform 1. Propagation Delay, Enable Input To Output, Enable Pulse Width



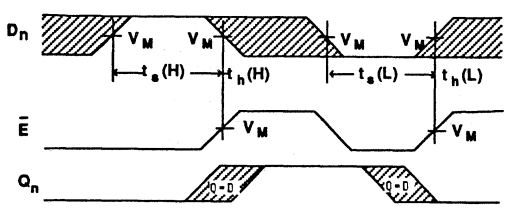
Waveform 2. Propagation Delay, Data To Output



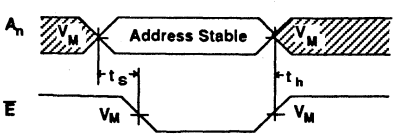
Waveform 3. Propagation Delay Address To Output



Waveform 4. Master Reset Pulse Width And Master Reset to Output Delay



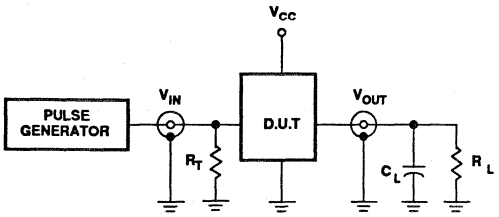
Waveform 5. Data Setup And Hold Times



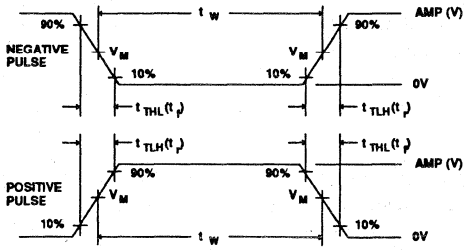
Waveform 6. Address Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0360
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Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F257, 74F257A
Data Selectors/Multiplexers

74F257 Quad 2-Line To 1-Line Selector/Multiplexer, Non-Inverting (3-State)
74F257A Quad 2-Line To 1-Line Selector/Multiplexer, Non-Inverting (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F257	4.3ns	12mA
74F257A	4.3ns	12mA

FEATURE

- **Multifunction capability**
- **Non-inverting data path**
- **3-state outputs**
- **See 'F258A for inverting version**

DESCRIPTION

The 74F257/74F257A has four identical 2-input multiplexers with 3-state outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I_{0n} inputs are selected when the common Select input is Low and the I_{1n} inputs are selected when the common Select input is High. Data appears at the outputs in true non-inverted form from the selected inputs. The 'F257/'F257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the common Select input. Outputs are forced to a high impedance "off" state when the Output Enable ($\overline{OE}$) is High. All but one device must be in high impedance state to avoid currents that would exceed the maximum ratings if the outputs were tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices were tied together.

The 74F257A is the faster version of 74F257.

ORDERING INFORMATION

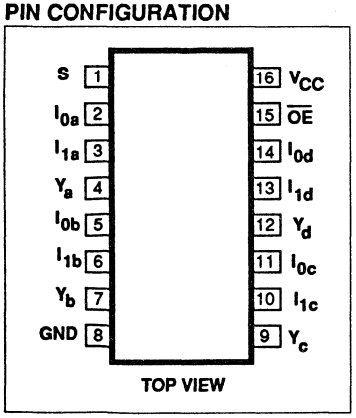
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F257N, N74F257AN
16-Pin Plastic SO	N74F257D, N74F257AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

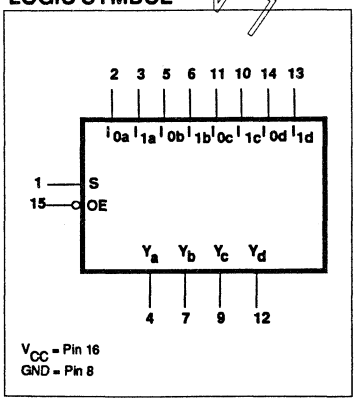
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20µA/0.6mA
S	Common Select input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs	150/33	3.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

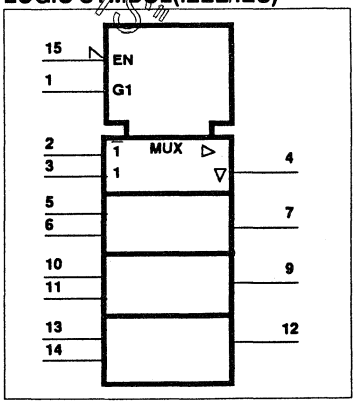
PIN CONFIGURATION



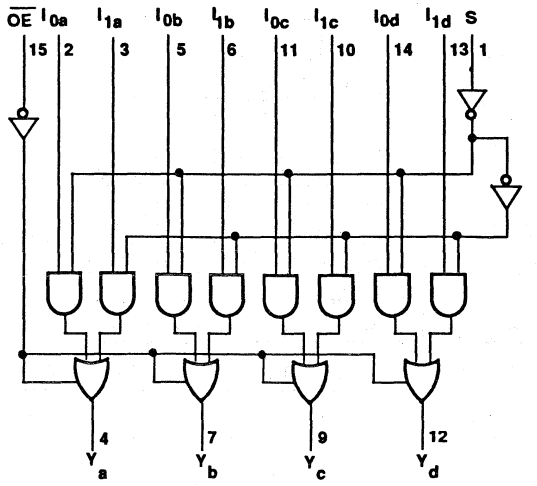
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



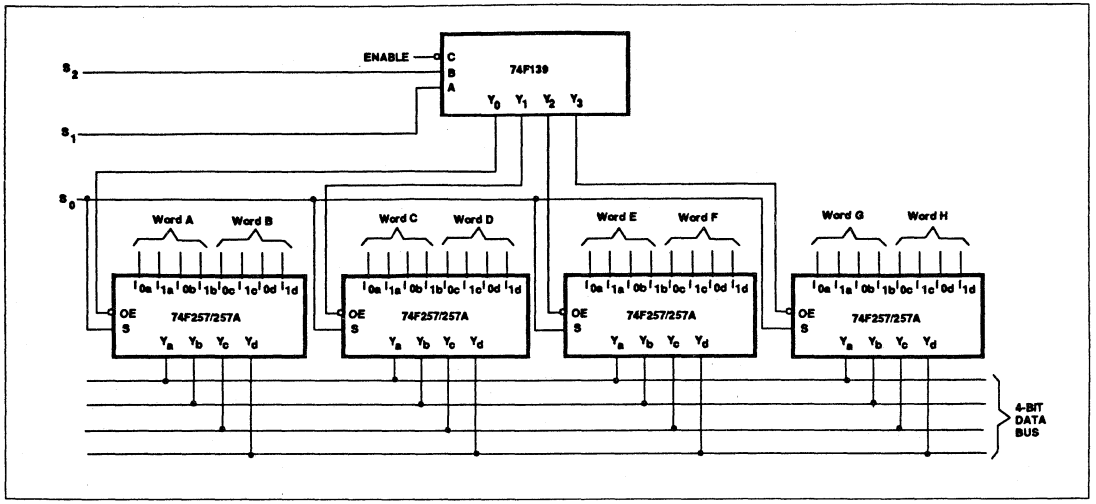
V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)	'F257	I_{CCH}	V_{CC} = MAX		9.0	16.0	mA
			I_{CCL}			14.5	22.0	mA
			I_{CCZ}			15.0	23.0	mA
		'F257A	I_{CCH}	V_{CC} = MAX		9.0	15.0	mA
			I_{CCL}			14.5	22.0	mA
			I_{CCZ}			15.0	23.0	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed lasty.
4. Measure I_{CC} with all outputs open and inputs grounded.

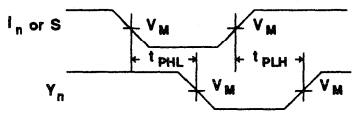
AC ELECTRICAL CHARACTERISTICS for 'F257

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 2.0	4.5 3.5	6.0 5.5	3.0 2.0	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay S to Y_n	Waveform 1	4.5 3.5	8.0 6.0	13.0 8.5	4.5 3.5	15.0 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	3.0 3.0	6.0 6.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	4.0 3.5	6.0 6.0	2.0 2.0	7.0 7.0	ns

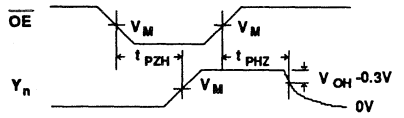
AC ELECTRICAL CHARACTERISTICS for 'F257A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 2.0	4.5 3.5	6.0 5.0	3.0 2.0	7.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Y_n	Waveform 1	5.5 4.0	7.5 5.5	9.5 7.0	5.0 4.0	10.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	4.5 4.5	6.5 6.0	7.5 7.5	4.5 4.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	4.0 3.5	5.5 5.5	2.0 2.0	6.0 6.0	ns

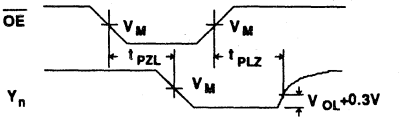
AC WAVEFORMS



Waveform 1. Propagation Delay, Data and Select to Output



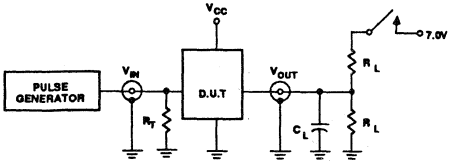
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

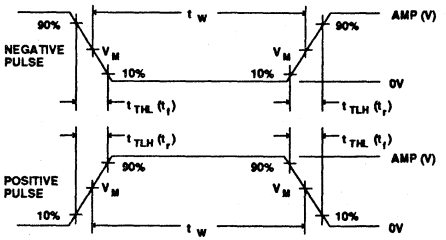
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0361
ECN No.	94759
Date of issue	October 7, 1988
Status	Product Specification
FAST Products	

FAST 74F258, 74F258A
Data Selectors/Multiplexers

74F258 Quad 2-Line To 1-Line Selector/Multiplexer, Inverting (3-State)
74F258A Quad 2-Line To 1-Line Selector/Multiplexer, Inverting (3-State)

FEATURES

- **Multifunction capability**
- **Inverting data path**
- **3-state outputs**
- **See 'F257A for non-inverting version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F258	3.8ns	10.7mA
74F258A	3.5ns	14mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F258N, N74F258AN
16-Pin Plastic SO	N74F258D, N74F258AD

DESCRIPTION

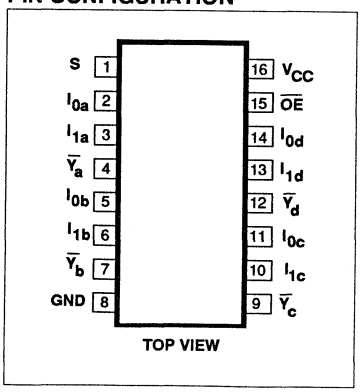
The 74F258/74F258A has four identical 2-input multiplexers with 3-state outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I_{0n} inputs are selected when the Select input is Low and the I_{1n} inputs are selected when the Select input is High. Data appears at the outputs in inverted form. The 'F258/'F258A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic level supplied to the Select input. Outputs are forced to a high impedance "off" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in high impedance state to avoid currents that would exceed the maximum ratings if the outputs are tied together. Design of the output signals must ensure that there is no overlap when outputs of 3-state devices are tied together. The 'F258A is the faster version of 'F258.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

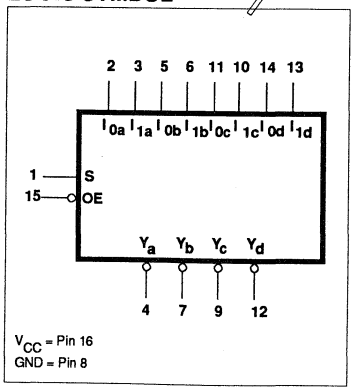
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20µA/0.6mA
S	Common Select input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

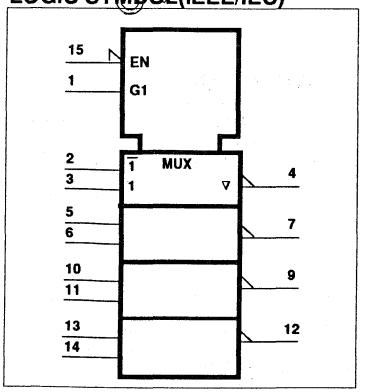
PIN CONFIGURATION



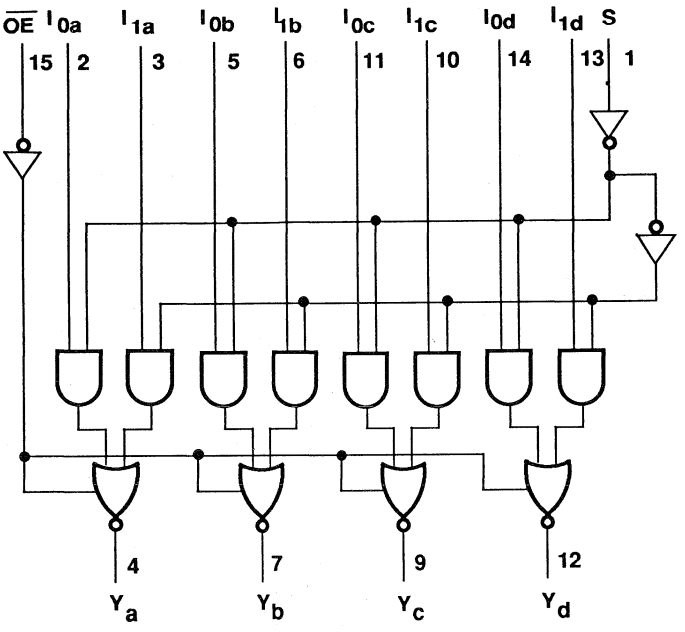
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	I_{1n} = 4.5V, $\overline{OE}$ = I_{0n} = S = GND		8.5	11.5	mA
		I_{CCL}		I_{1n} = S = 4.5V, $\overline{OE}$ = I_{0n} = GND		17	23	mA
		I_{CCZ}		I_{1n} = $\overline{OE}$ = 4.5V, I_{0n} = S = GND		16	22	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

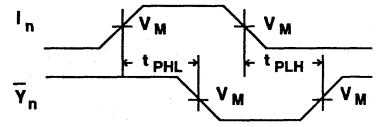
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F258					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	2.5 1.0	4.0 2.5	6.0 4.7	2.5 1.0	7.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$	Waveform 2	3.5 2.5	6.5 6.0	8.5 9.5	3.5 2.5	9.5 11.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 3 Waveform 4	3.0 3.0	5.9 5.5	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 3 Waveform 4	2.0 2.0	3.5 3.5	6.0 6.0	2.0 2.0	7.0 7.0	ns

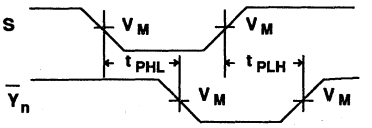
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F258A					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	3.0 1.0	4.5 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$	Waveform 2	3.5 2.5	6.5 6.0	8.0 8.0	3.5 2.5	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.0	6.0 5.5	7.5 7.5	3.5 3.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 3 Waveform 4	2.0 2.0	3.5 3.5	5.5 5.5	2.0 2.0	6.5 6.0	ns

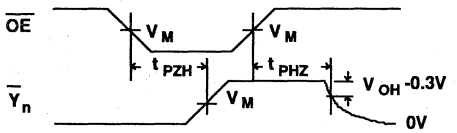
AC WAVEFORMS



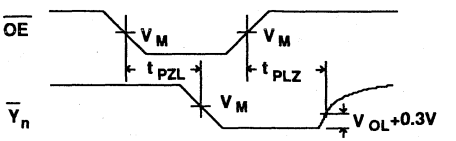
Waveform 1. Propagation Delay, Data to Output



Waveform 2. Propagation Delay, Select to Output



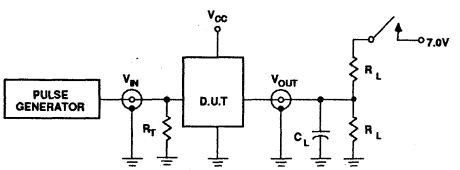
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

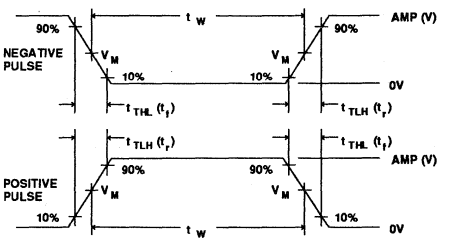
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0362
ECN No.	06316
Date of issue	April 11, 1989
Status	Product Specification
FAST Products	

FAST 74F259
Latch

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F259	7.5ns	31mA

FEATURES

- **Combines demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common reset input**
- **Useful as a 1-of-8 active-High decoder**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F259N
16-Pin Plastic SO	N74F259D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

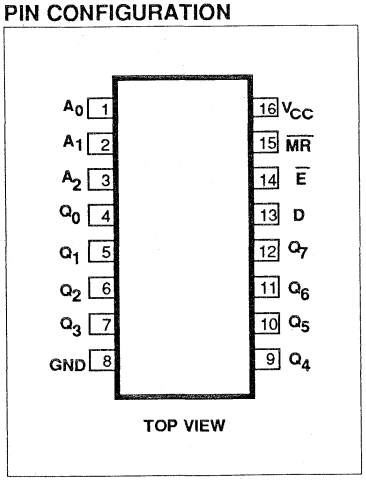
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D	Data input	1.0/1.0	20µA/0.6mA
A_0, A_1, A_2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset inputs (active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

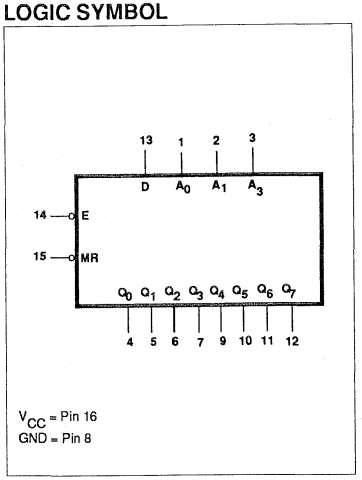
The 74F259 addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset ($\overline{MR}$) and Enable ($\overline{E}$) inputs (see Function Table). In the addressable latch mode, data at the Data inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the store mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the Enable should be held High (inactive) while the address lines are changing. In the 1-0f-8 decoding or demultiplexing mode ($\overline{MR}$=$\overline{E}$=Low), addressed outputs will follow the level of the Data input, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

PIN CONFIGURATION



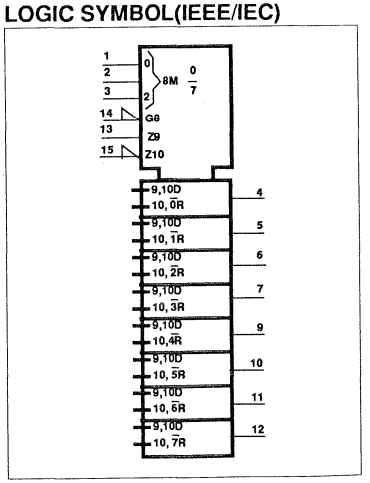
TOP VIEW

LOGIC SYMBOL

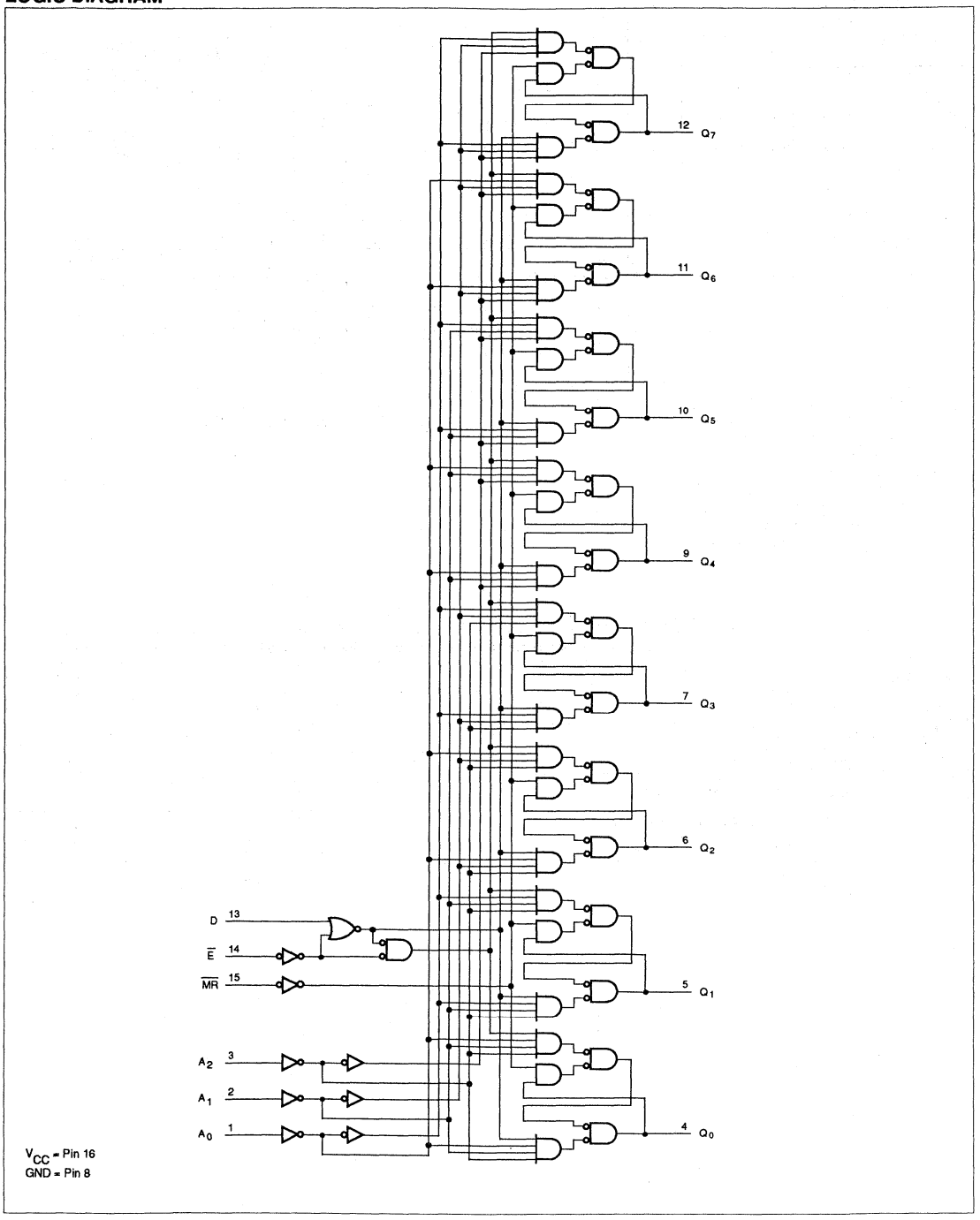


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS								OPERATING MODE
$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	L	L	L	L	L	L	L	L	L	Master Reset
L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L	Demultiplex (active-High decoder when D=H)
L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L	
L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L	
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L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d	
H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7	Store (do nothing)
H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7	Addressable Latch
H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7	
H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7	
.	.	.	.	.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	.	.	.	.	
H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d	

H = High voltage level
L = Low voltage level
X = Don't care
d = High or Low data one setup time prior to the Low-to-High Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			24	46	mA
		I_{CCL}				37	75	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

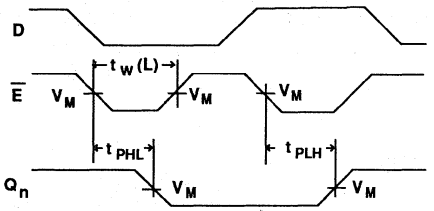
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D to Q_n	Waveform 1	4.0 3.0	7.0 5.0	9.0 7.0	4.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 2	5.0 4.0	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	5.0	7.0	9.0	4.5	10.0	ns

AC SETUP REQUIREMENTS

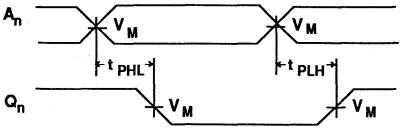
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D to $\overline{E}$	Waveform 4	3.0 6.5			3.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D to $\overline{E}$	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to $\overline{E}$[1]	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to $\overline{E}$[2]	Waveform 5	0 0			0 0		ns
$t_w(L)$	$\overline{E}$ Pulse width, Low	Waveform 1	7.5			8.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	3.0			3.0		ns

NOTES:
1. The Address to Enable setup time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time before the Low-to-High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

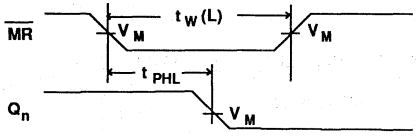
AC WAVEFORMS



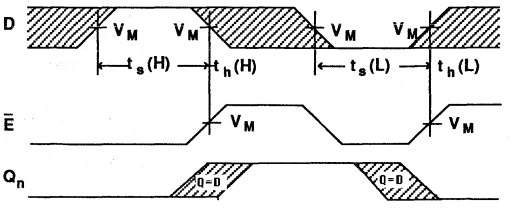
Waveform 1. Propagation Delay, Enable Input To Output, Enable Pulse Width



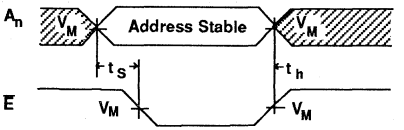
Waveform 2. Propagation Delay Address To Output



Waveform 3. Master Reset Pulse Width And Master Reset to Output Delay



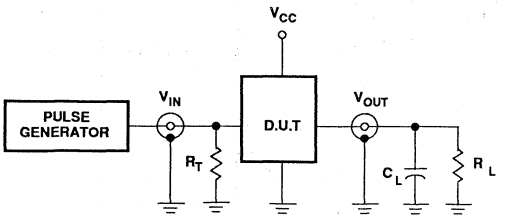
Waveform 4. Data Setup And Hold Times



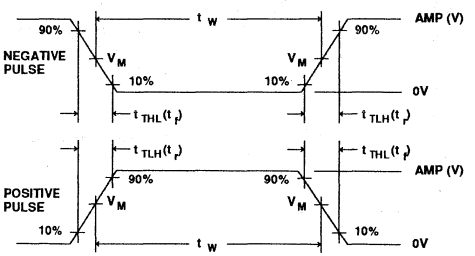
Waveform 5. Address Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

Document No.	853-0048
ECN No.	95209
Date of issue	November 29, 1988
Status	Product Specification
FAST Products	

FAST 74F260 Gate

Dual 5-Input NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F260	3.5 ns	6 mA

ORDERING INFORMATION

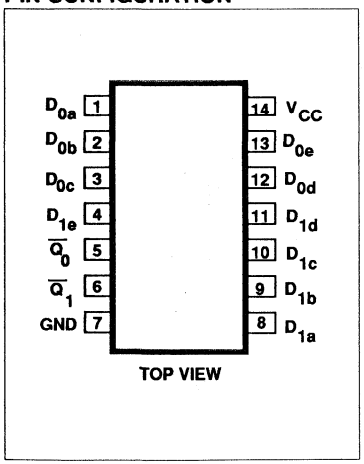
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F260N
14-Pin Plastic SO	N74F260D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

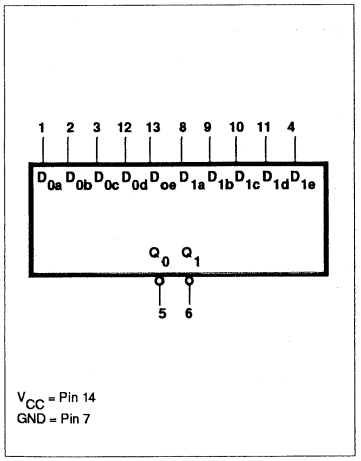
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}, D_{ne}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

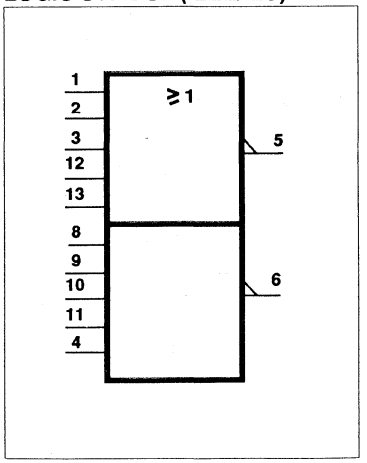
PIN CONFIGURATION



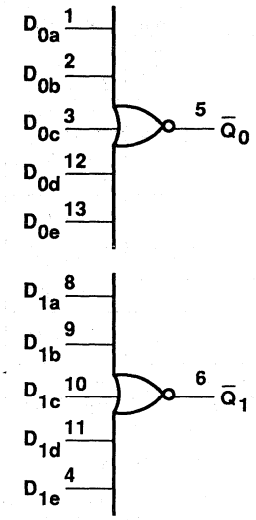
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS					OUTPUT
D_{na}	D_{nb}	D_{nc}	D_{nd}	D_{ne}	$\overline{Q}_n$
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

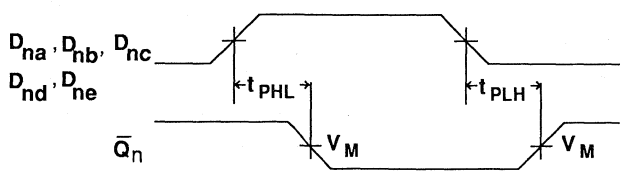
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		4.6	6.5	mA
		I_{CCL}		V_{IN}=4.5V		7.3	9.5	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd}, D_{ne} to $\overline{Q}_n$	Waveform 1	2.5 1.5	4.0 2.5	5.5 4.0	2.0 1.0	6.5 4.5	ns

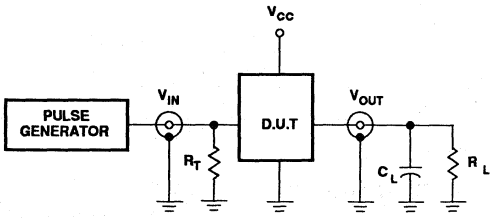
AC WAVEFORMS



Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



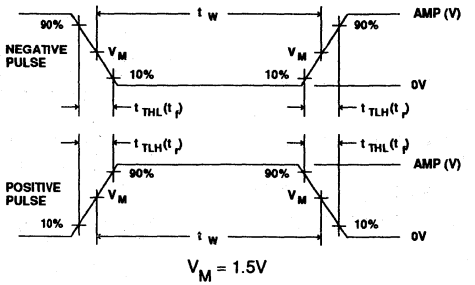
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0056
ECN No.	00287
Date of issue	August 31 1990
Status	Product Specification
FAST Products	

FAST 74F269 Counter

8-Bit Bidirectional Binary Counter

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

FEATURES

- **Synchronous counting and loading**
- **Built-in look-ahead carry capability**
- **Count frequency 115 MHz typ**
- **Supply current 95mA typ**

DESCRIPTION

The 74F269 is a fully synchronous 8-stage Up/Down Counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

ORDERING INFORMATION

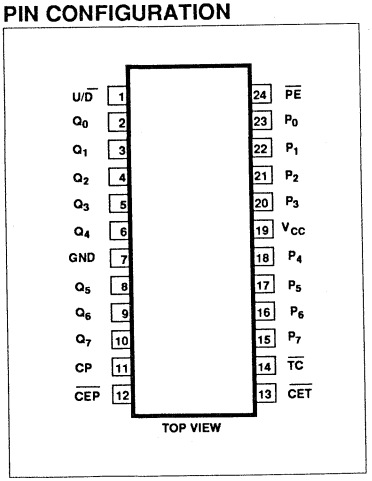
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim Dip (300 mil)	N74F269N
24-Pin Plastic SOL	N74F269D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

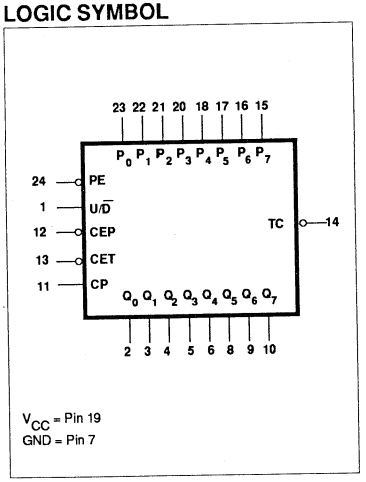
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
P_0 - P_7	Parallel Data inputs	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA
Q_0 - Q_7	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

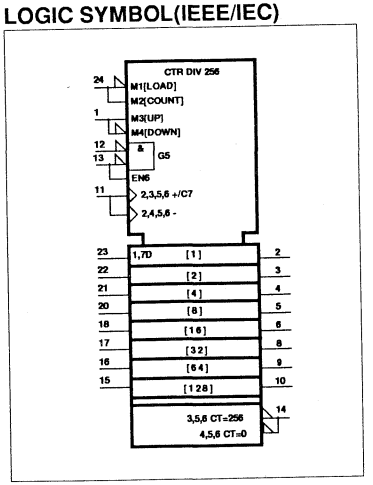
PIN CONFIGURATION



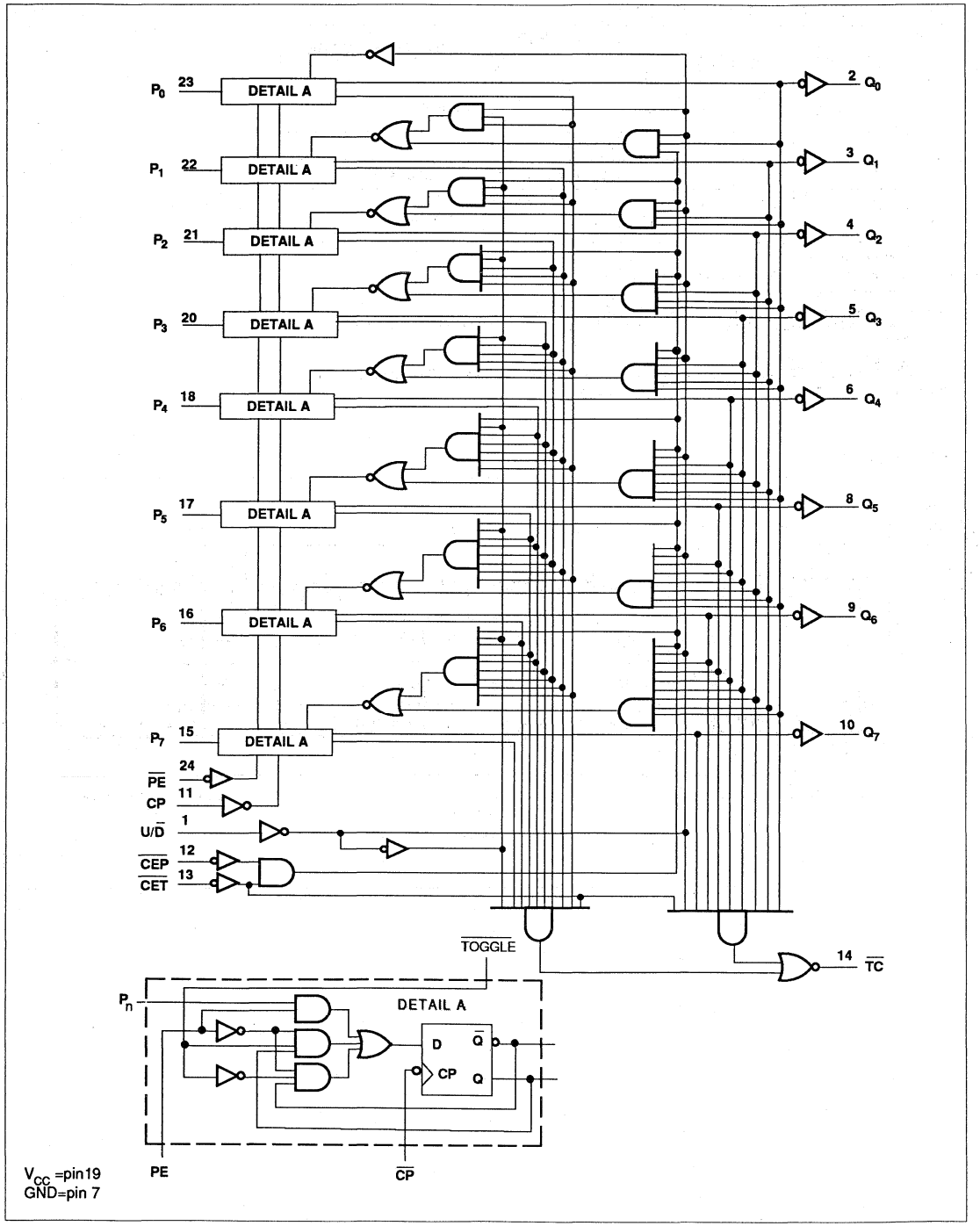
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT-FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	P_n	Q_n	$\overline{TC}$	
↑	X	X	X	l	l	L	(a)	Parallel load
↑	X	X	X	l	h	H	(a)	
↑	h	l	l	h	X	Count up	(a)	Count up
↑	l	l	l	h	X	Count down	(a)	Count down
↑	X	h	l	h	X	q_n	(a)	Hold (do nothing)
↑	X	X	h	h	X	q_n	H	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(a) = $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. The Terminal Count up is with all Q_n outputs High andTerminal Count Down is with all Q_n outputs Low.

APPLICATION

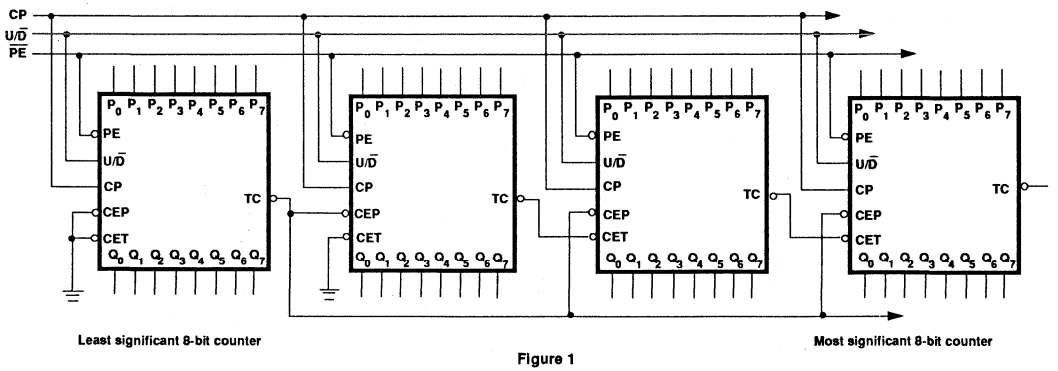


Figure 1
Synchronous multistage counting scheme

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuitoutput current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{PE}$=$\overline{CET}$=$\overline{CEP}$=U/$\overline{D}$=GND, P_n=4.5V, CP=↑		93	120	mA
		I_{CCL}		$\overline{PE}$=$\overline{CET}$=$\overline{CEP}$=U/$\overline{D}$=GND, P_n=GND, CP=↑		98	125	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable typ5
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

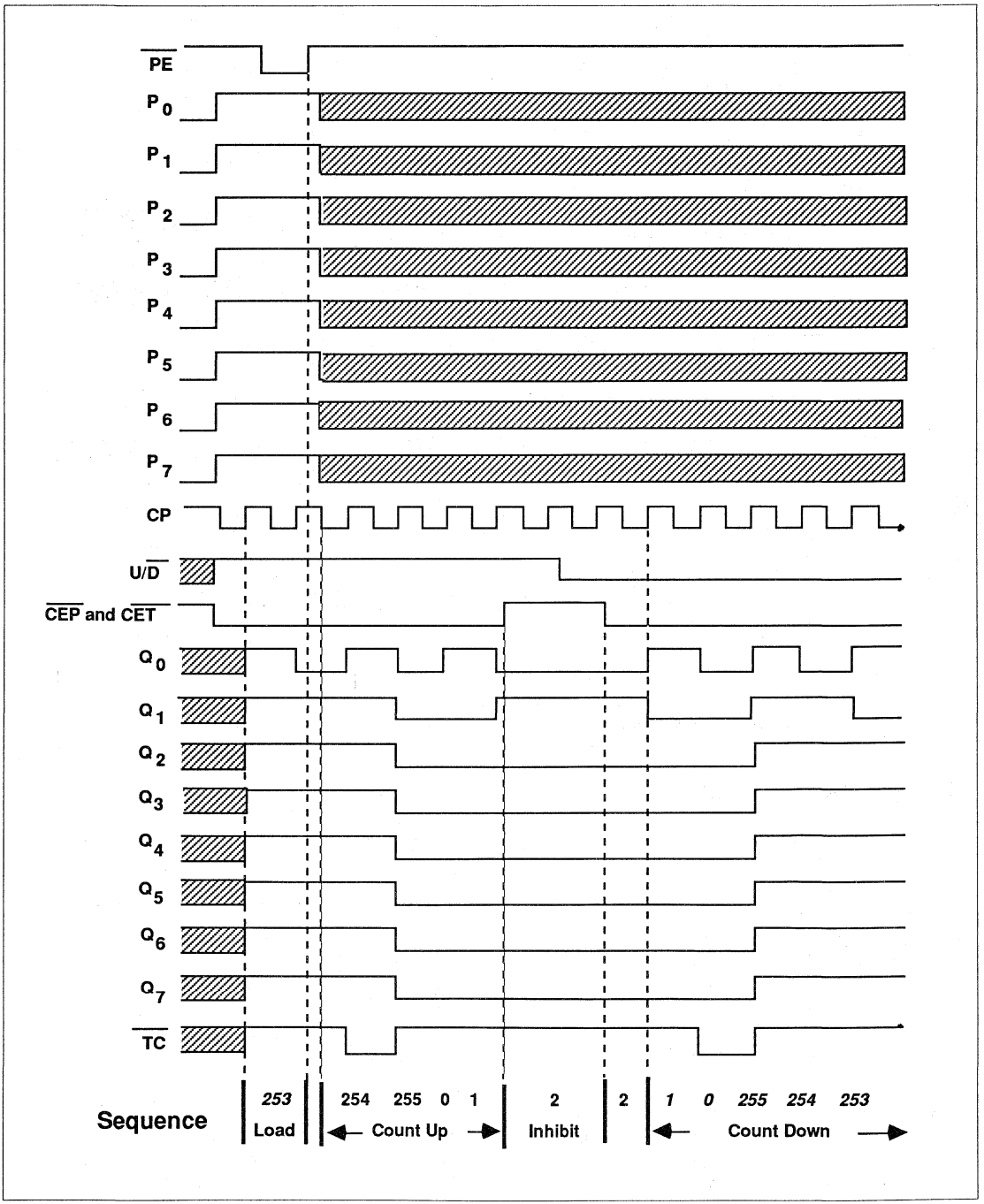
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Load, $\overline{PE}$ = Low)	Waveform 1	3.0 4.0	6.0 6.5	8.5 8.5	3.0 4.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Count, $\overline{PE}$ = High)	Waveform 1	3.0 4.5	6.0 7.0	9.0 10.0	3.0 4.0	10.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 5.0	6.5 6.5	9.5 9.5	4.0 5.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.5 3.5	6.0 6.5	9.0 9.0	3.0 3.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 3	4.5 4.5	7.0 7.0	9.0 9.5	4.0 4.0	10.0 10.0	ns

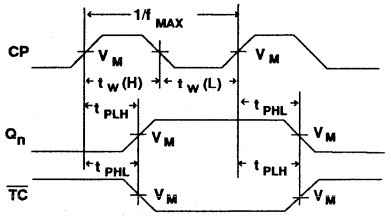
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low P_n to CP	Waveform 4	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low P_n to CP	Waveform 4	0 1.0			0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	5.0 6.0			5.5 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	4.5 6.0			5.0 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	Waveform 6	6.0 6.0			6.5 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width High or Low	Waveform 1	4.0 4.5			4.0 5.0		ns

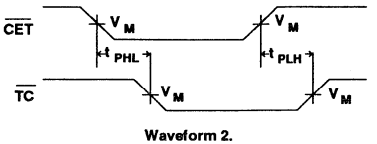
TIMING DIAGRAM (Typical Load, Count and Inhibit Sequence)



AC WAVEFORMS

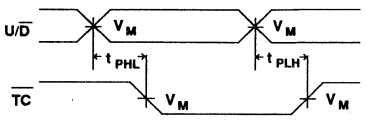


Waveform 1.
Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

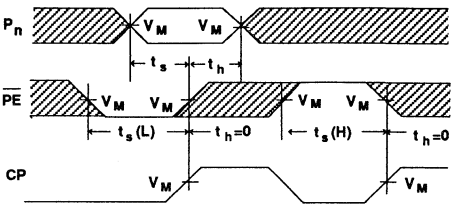


Waveform 2.

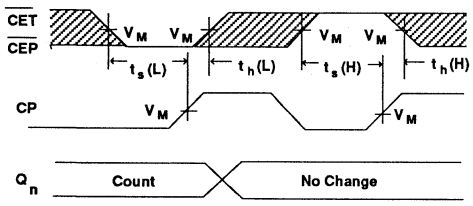
Propagation Delay, CET input to Terminal Count Output



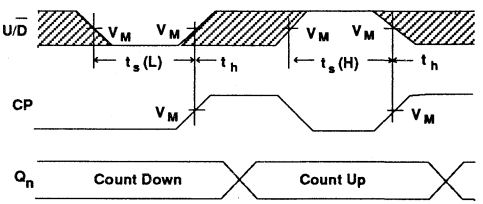
Waveform 3.
Propagation Delay, Up/Down Count Control Input to Terminal Count Output



Waveform 4.
Parallel Data and Parallel Enable Setup and Hold Times



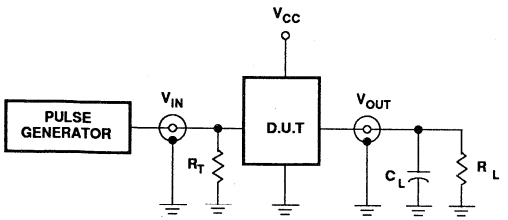
Waveform 5.
Count Enables Setup and Hold Times



Waveform 6.
Up/Down Count Control Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



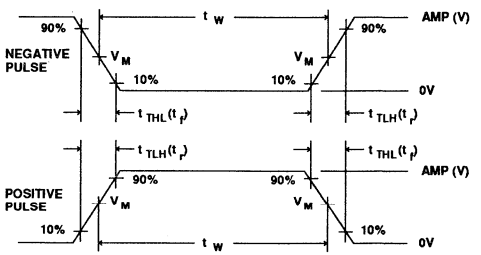
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal D flip–flop | 74F273/273A

FEATURES

- High impedance inputs for reduced loading (20μA in Low and High states)
- Ideal buffer for MOS microprocessor or memory
- Eight edge–triggered D–type flip–flops
- Buffered common clock
- Buffered asynchronous Master Reset
- 74F273A has improved DC, AC, and f_{MAX}
- 74F273A has improved noise margin
- See 74F377 for clock enable version
- See 74F373 for transparent latch version
- See 74F374 for 3–State version

DESCRIPTION

The 74F273 has eight edge–triggered D–type flip–flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip–flops simultaneously.

The register is fully edge–triggered. The state of each D input, one setup time before the Low–to–High clock transition, is transferred to the corresponding flip–flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common to all elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F273	125MHz	66mA
74F273A	170MHz	25mA

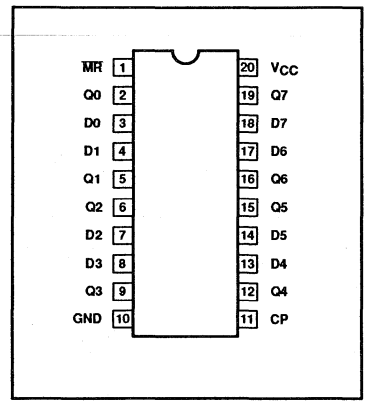
ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C
20–pin plastic DIP	74F273N, 74F273AN
20–pin plastic SOL	74F273D, 74F273AD

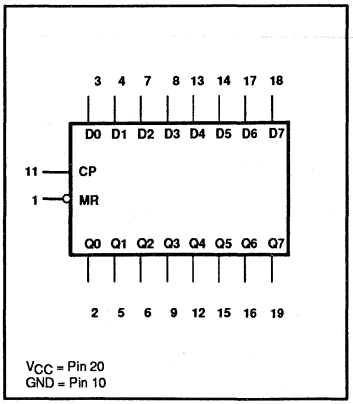
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active–Low)	1.0/0.033	20μA/20μA
CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

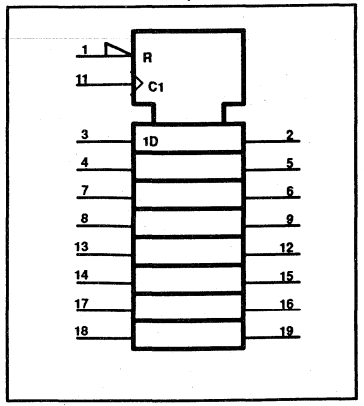
PIN CONFIGURATION



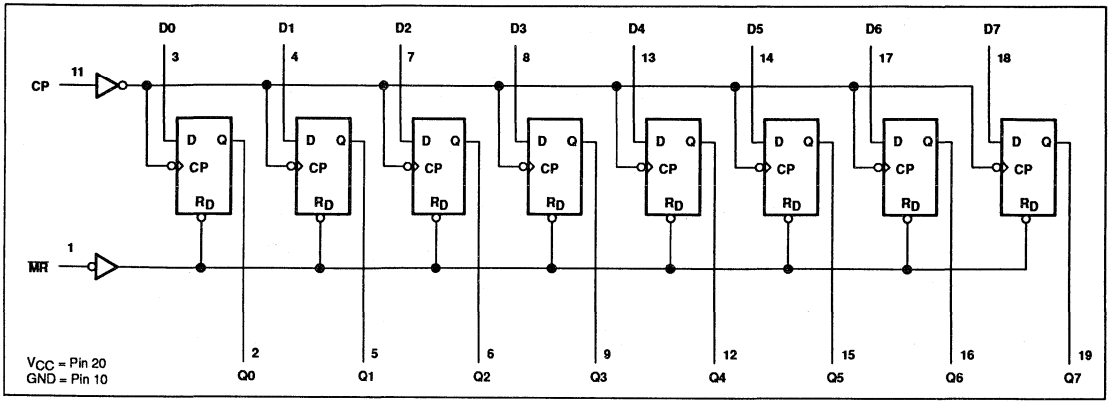
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	Dn	Q0 – Q7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
h = High voltage level one set–up time prior to the Low–to–High clock transition
L = Low voltage level
l = Low voltage level one set–up time prior to the Low–to–High clock transition
X = Don't care
↑ = Low–to–High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		MR & CP	V_{CC} = MIN, V_{IL} = 0.0V[3],	±10%V_{CC}	2.5			V
			inputs	V_{IH} = 4.5V[3], I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
			other	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
			inputs	V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.30	0.50	V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High–level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current			V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OS}	Short–circuit output current[4]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	74F273	I_{CCH}	V_{CC} = MAX			65	85	mA
			I_{CCL}				68	88	mA
		74F273A	I_{CCH}	V_{CC} = MAX			24	38	mA
			I_{CCL}				27	43	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS FOR 'F273

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	115	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	4.0 4.0	7.5 7.5	9.5 9.5	4.0 4.0	10.5 10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	2	4.0	5.5	8.5	3.5	9.0	ns

AC SETUP REQUIREMENTS FOR 'F273

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	3	3.0 3.0			3.0 3.0		
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	3	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	1	4.0 5.0			4.0 5.5		ns
$t_w(L)$	Master Reset pulse width, Low	2	3.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	8.5			9.0		ns

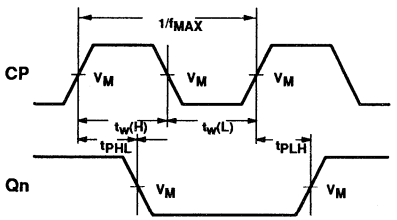
AC CHARACTERISTICS FOR 'F273A

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	150	170		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	3.5 5.0	5.0 7.0	8.0 9.5	3.0 4.5	9.0 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	2	5.0	7.0	9.0	5.0	9.5	ns

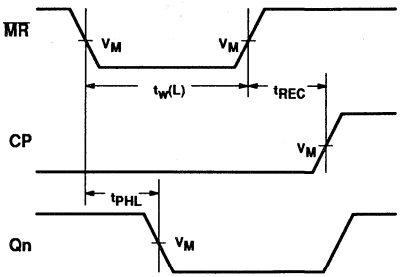
AC SETUP REQUIREMENTS FOR 'F273A

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	3	3.0 2.0			2.5 2.5		
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	3	0.5 0.0			2.5 1.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	1	4.5 3.5			5.0 4.0		ns
$t_w(L)$	Master Reset pulse width, Low	2	3.0			3.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	4.0			5.0		ns

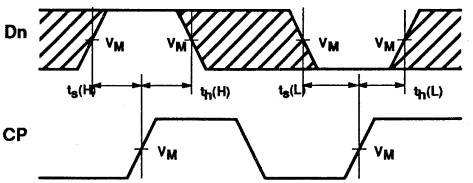
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



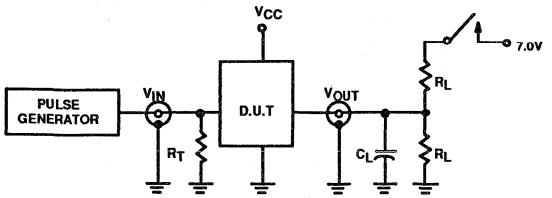
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



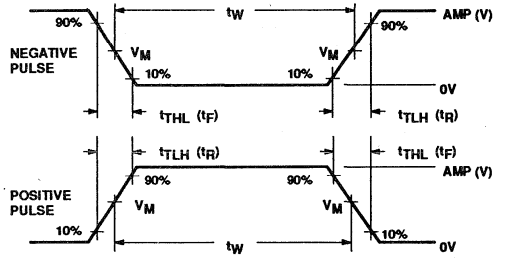
Waveform 3. Data Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0363
ECN No.	99142
Date of issue	March 19 1990
Status	Product Specification
FAST Products	

FAST 74F280A, 74F280B
Parity Checker Generator

9-Bit Odd/Even Parity Generator/Checker

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F280A	6.5ns	26mA
74F280B	5.5ns	26mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Buffered inputs--one normalized load**
- **Word length easily expanded by cascading**
- **Industrial temperature range available (-40°C to +85°C) for 74F280B**

DESCRIPTION

The 74F280A is a 9-bit Parity Generator or Checker commonly used to detect errors in high speed data transmission or data retreival systems. Both Even (Σ_E) and Odd (Σ_O) parity outputs are available for generating and checking even or odd parity on up to 9 bits.

The Even (Σ_E) parity output is High when an even number of data inputs (I_0-I_8) are HIgh. The Odd (Σ_O) parity output is High when an odd number of data inputs are High.

Expansion to larger word sizes is accomplished by tying the Even (Σ_E) outputs of up to nine parallel devices to the data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 20 ns.

The 74F280B is a faster version of 74F280A

ORDERING INFORMATION

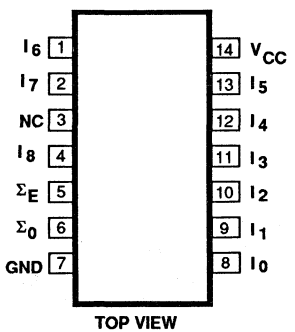
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
14-Pin Plastic DIP	N74F280AN, N74F280BN	I74F280BN
14-Pin Plastic SO	N74F280AD, N74F280BD	I74F280BD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0-I_8	Data inputs	1.0/0.033	20μA/20μA
Σ_E , Σ_O	Parity outputs	50/33	1.0mA/20mA

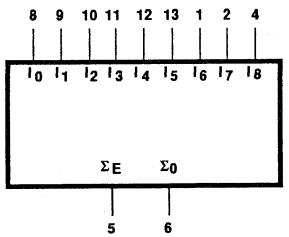
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



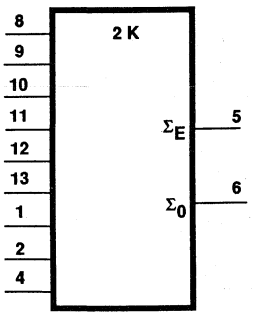
TOP VIEW

LOGIC SYMBOL

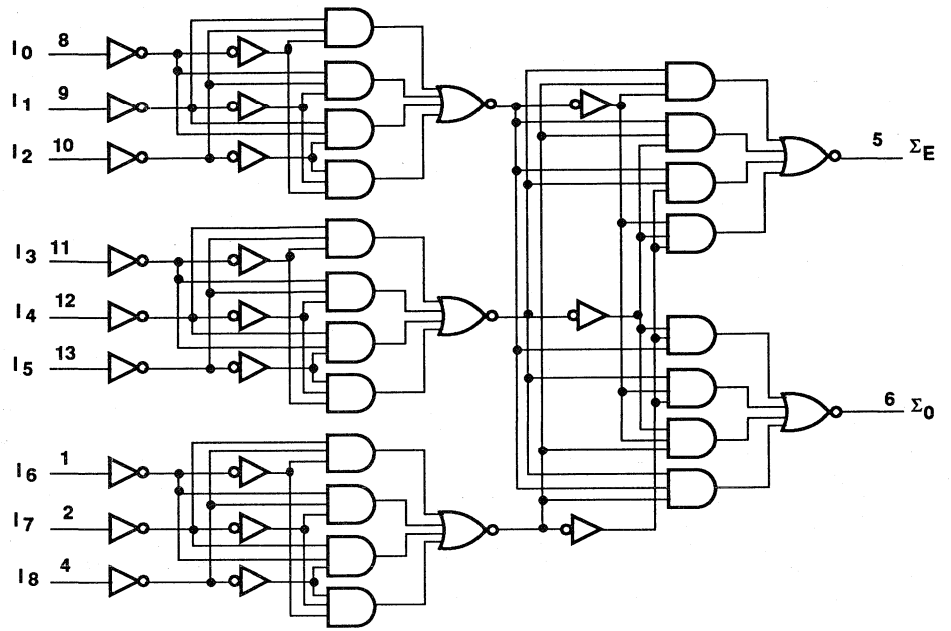


V_{CC} =Pin 14
GND=Pin 7

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS	OUTPUTS	
Number of High data inputs (I_0-I_8)	Σ_E	Σ_O
Even ------ 0, 2, 4, 6, 8	H	L
Odd ------1, 3, 5, 7, 9	L	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_A	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	-40		85	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
	Input clamp voltage		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input current at maximum input voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I			V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	Commercial range	V_{CC} = MAX, V_I = 2.7V				20	µA
	Low-level input current	Industrial range					40	µA
I_{IL}	Short-circuitoutput current[3]		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OS}	Supply current (total)		V_{CC} = MAX		-60		-150	mA
I_{CC}			V_{CC} = MAX			26	35	mA

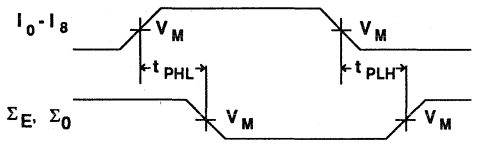
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

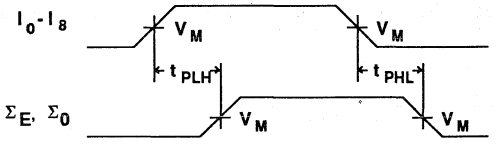
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS							UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	'F280A	Waveform 1,2	5.0 7.5	7.0 10.0	9.0 13.0	5.0 7.5	10.0 14.5			ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O	'F280A	Waveform 1,2	6.5 7.0	8.6 9.1	10.5 12.0	6.5 6.0	11.0 13.0			ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	'F280B	Waveform 1,2	4.0 4.0	6.5 7.0	9.0 10.0	3.5 3.5	10.0 11.1	3.0 3.5	11.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O	'F280B	Waveform 1,2	4.0 4.0	6.5 7.0	9.0 10.0	3.5 3.5	10.0 11.0	3.0 3.5	11.0 12.0	ns

AC WAVEFORMS



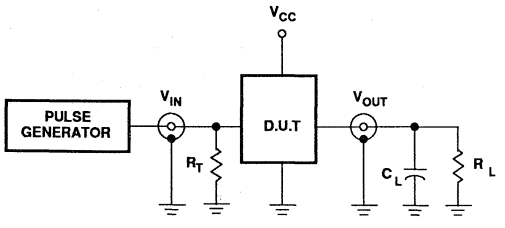
Waveform 1. Propagation Delay For Inverting Outputs



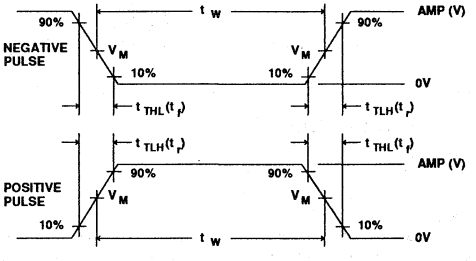
Waveform 2. Propagation Delay For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0364
ECN No.	95944
Date of issue	March 3, 1989
Status	Product Specification
FAST Products	

FAST 74F283

4-Bit Binary Full Adder With Fast Carry

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F283	6.5ns	40mA

FEATURES

- **High speed 4-bit binary addition**
- **Cascadable in 4-bit increments**
- **Fast internal carry look-ahead**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F283N
16-Pin Plastic SO	N74F283D

DESCRIPTION

The 74F283 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ_0-Σ_3) and the outgoing carry (C_{OUT}) according to the equation:

$C_{IN} + 2^0(A_0 + B_0) + 2^1(A_1 + B_1) + 2^2(A_2 + B_2) + 2^3(A_3 + B_3)$

$= \Sigma_0 + 2\Sigma_1 + 4\Sigma_2 + 8\Sigma_3 + 16C_{OUT}$

where (+) = plus

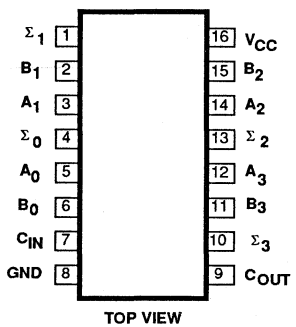
Due to the symmetry of the binary add function, the 'F283 can be used with either all active-High operands (positive logic) or with all active-Low operands (negative logic). See Function Table. In case of all active-Low operands (negative logic) the results Σ_1-Σ_4 and C_{OUT} should be interpreted also as active-Low. With active-High inputs, C_{IN} cannot be left open; it must be held Low when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus A_0, B_0, C_{IN} can arbitrarily be assigned to pins 5, 6, 7, etc.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	A operand inputs	1.0/2.0	20µA/1.2mA
B_0 - B_3	B operand inputs	1.0/2.0	20µA/1.2mA
C_{IN}	Carry input	1.0/1.0	20µA/0.6mA
C_{OUT}	Carry output	50/33	1.0mA/20mA
Σ_0 - Σ_3	Sum outputs	50/33	1.0mA/20mA

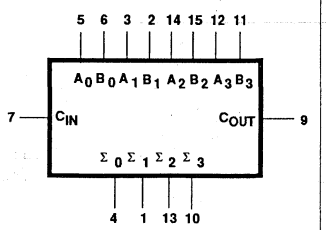
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



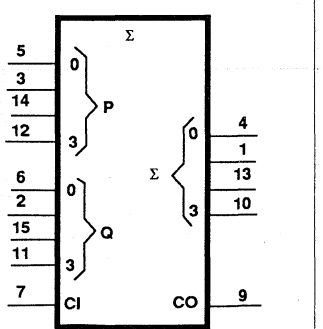
TOP VIEW

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



4-Bit Adder

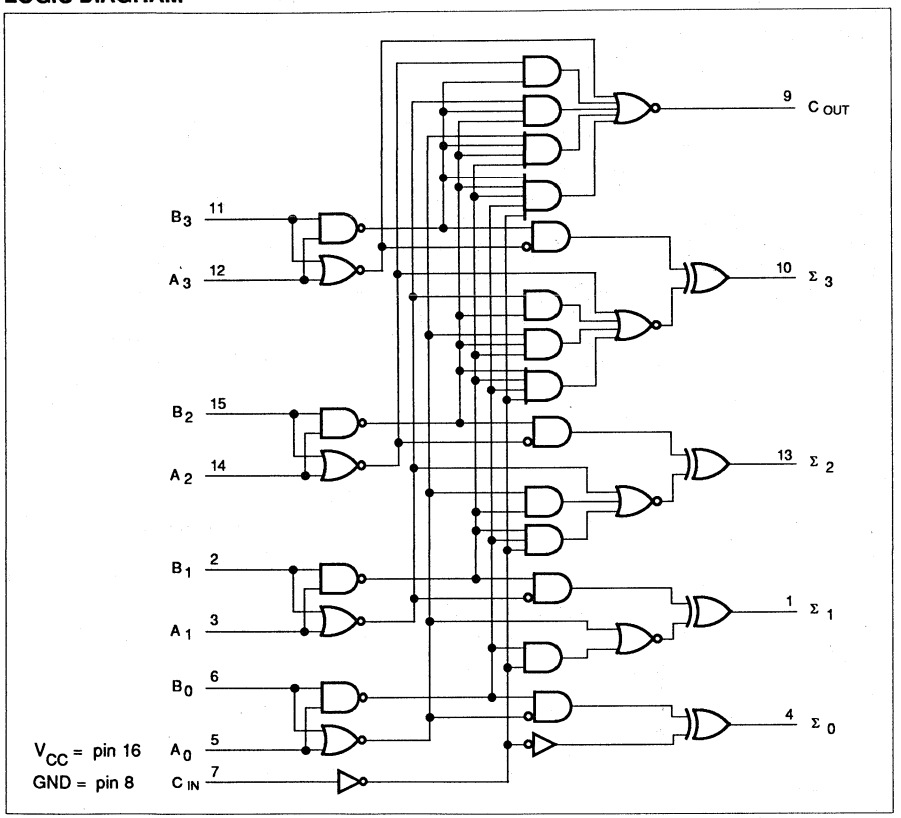
FAST 74F283

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage.

Figure a shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) Low makes Σ_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure b shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, Σ_2) is used as means of getting a carry (C_{10}) signal into the fourth stage adder (via A_2 and B_2) and bringing out the carry from the second stage on Σ_2. Note that as long as A_2 and B_2 are the same, whether High or Low, they do not influence Σ_2. Similarly, when A_2 and B_2 are the same, the carry into the third stage does not influence the carry out of the third stage.

Figure c shows a method of implementing a 5-input encoder where the inputs are equally weighted. The outputs Σ_0, Σ_1 and Σ_2 present a binary number equal to the number of inputs I_0 - I_4 that are true. Figure d shows one method of implementing a 5-input majority gate. When three or more of the inputs I_0 - I_4 are true, the output M_4 is true.

LOGIC DIAGRAM



FUNCTION TABLE

PINS	C_{IN}	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	Σ_0	Σ_1	Σ_2	Σ_3	C_{OUT}
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active High	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Example:
1001
1010
10011
(10+9=19)
(carry+5+6=12)

H = High voltage level
L = Low voltage level

APPLICATIONS

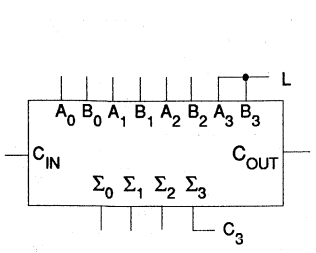


Figure a 3-bit adder

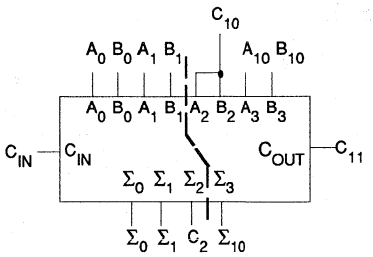


Figure b 2-bit and 1-bit adder

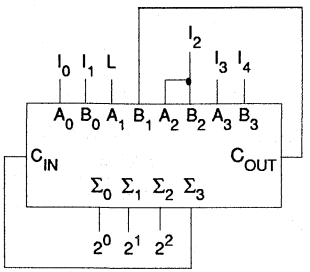


Figure c 5-input Encoder

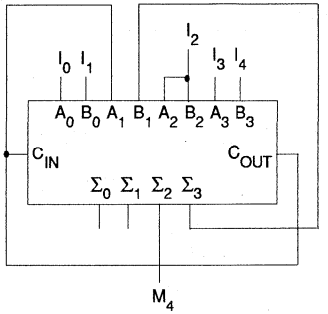


Figure d 5-input majority Gate

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_{IN} only	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		A_n, B_n					-1.2	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			40	55	mA

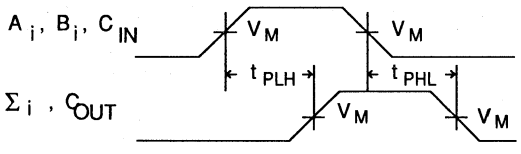
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} should be measured with all outputs open and the following conditions:
   Condition 1: all inputs grounded
   Condition 2: all B intputs Low, other inputs at 4.5V
   Condition 3: all inputs at 4.5V

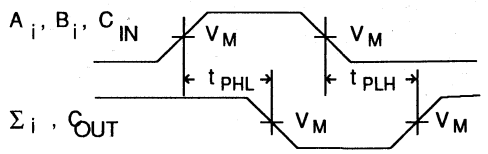
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_i	Waveform 1, 2	3.5 4.0	7.0 7.0	9.5 9.5	3.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to Σ_i	Waveform 1, 2	3.5 3.5	7.0 7.0	9.5 9.5	2.5 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2	3.5 3.0	5.7 5.4	7.5 7.0	3.5 2.5	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{OUT}	Waveform 1, 2	3.5 2.5	5.7 5.3	7.5 7.0	3.0 2.5	8.5 8.0	ns

AC WAVEFORMS



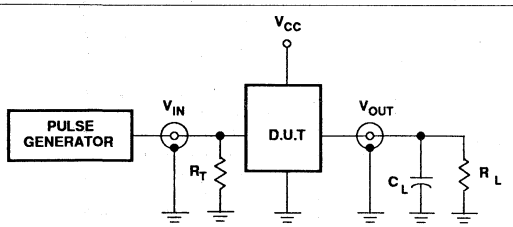
Waveform 1. Propagation Delay
Operands and Carry inputs to Outputs



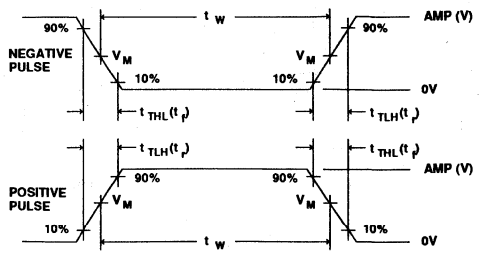
Waveform 2. Propagation Delay
Operands and Carry inputs to Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0061
ECN No.	97377
Date of issue	August 14, 1989
Status	Product Specification
FAST Products	

FAST 74F298
Multiplexer

Quad 2-Input Multiplexer With Storage

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F298	115MHz	30mA

FEATURES

- **Fully synchronous operation**
- **Select from two data sources**
- **Buffered, negative edge triggered clock**
- **Provides the equivalent of function capabilities of two separate MSI functions (74F157 and 74F175)**

DESCRIPTION

The 74F298 is a high speed Quad 2-Input Multiplexer with storage. It selects 4 bits of data from two sources (ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the High-to-Low transition of the clock ($\overline{CP}$). The 4-bit register is fully edge triggered. The data inputs (I_0 and I_1) and Select input (S) must be stable only one setup time prior to the High-to-Low transition of the clock for predictable operation.

ORDERING INFORMATION

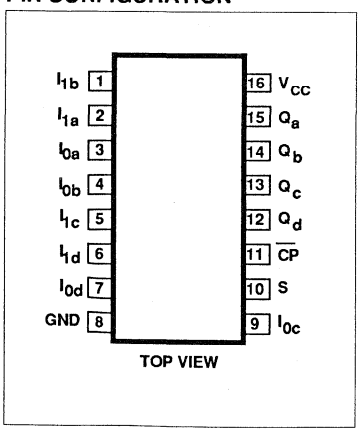
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-pin Plastic DIP	N74F298N
16-pin Plastic SO	N74F298D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}, I_{0b}, I_{0c}, I_{0d}	Data inputs	1.0/1.0	20µA/0.6mA
I_{1a}, I_{1b}, I_{1c}, I_{1d}	Data inputs	1.0/1.0	20µA/0.6mA
S	Select input	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock input (active falling edge)	1.0/1.0	20µA/0.6mA
Q_a, Q_b, Q_c, Q_d	Data outputs	50/33	1.0mA/20mA

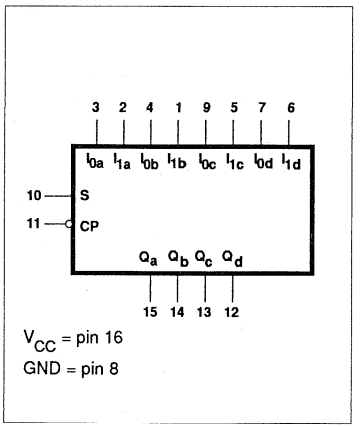
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



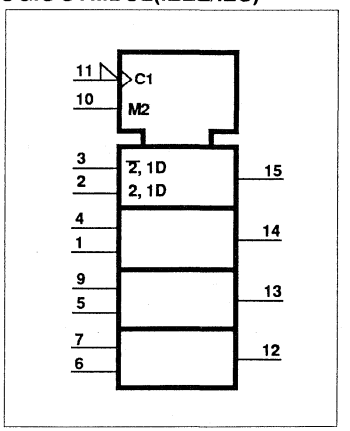
TOP VIEW

LOGIC SYMBOL

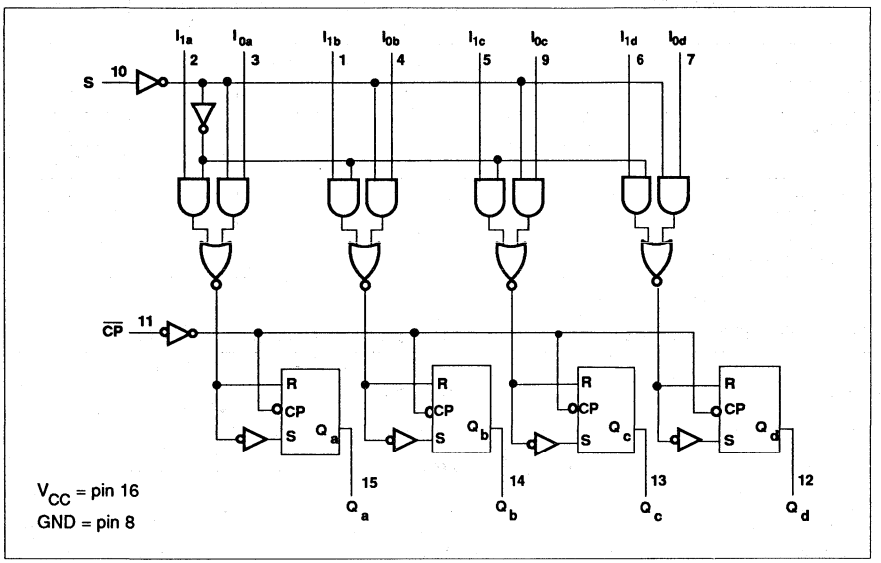


V_{CC} = pin 16
GND = pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT	OPERATING MODE
$\overline{CP}$	S	I_{0n}	I_{1n}	Q_n	
↓	l	l	X	L	Load source "0"
↓	l	h	X	H	
↓	h	X	l	L	Load source "1"
↓	h	X	h	H	

H = High voltage level
h = High voltage level one set-up time prior to the High-to Low clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low clock transition
X = Don't care
↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=-MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuitoutput current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				32	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

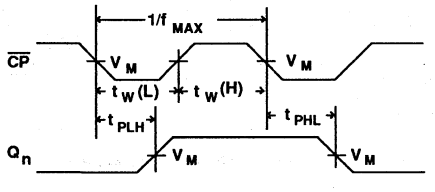
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	115		105		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n	Waveform 1	4.0 4.5	5.5 6.5	7.5 8.5	4.0 4.5	9.0 9.5	ns

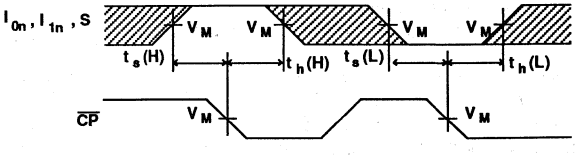
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I_{0n}, I_{1n} to $\overline{CP}$	Waveform 2	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I_{0n}, I_{1n} to $\overline{CP}$	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to $\overline{CP}$	Waveform 2	6.0 5.0			7.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S to $\overline{CP}$	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width, High or Low	Waveform 1	5.0 5.0			5.0 7.0		ns

AC WAVEFORMS



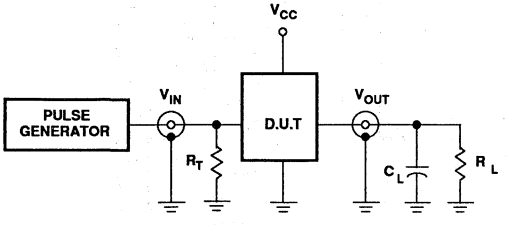
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



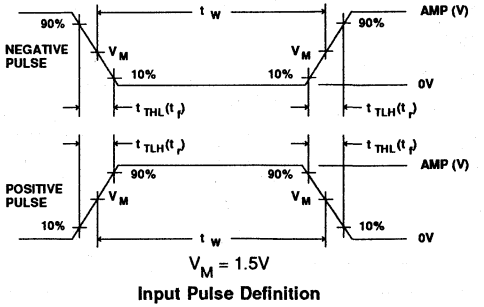
Waveform 2. Data Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0365
ECN No.	98989
Date of issue	March 1, 1990
Status	Product Specification
FAST Products	

FAST 74F299 Register

8-Bit Universal Shift/Storage Register(3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F299	115 MHz	58mA

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional serial inputs and outputs for expansion**
- **Four operating modes: Shift left, shift right, load and store**
- **3-state outputs for bus oriented applications**

DESCRIPTION

The 74F299 is an 8-bit universal shift / storage register with 3-state outputs. Four modes of operation are possible: Hold (store), shift left, shift right and parallel load. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active-Low Master Reset is used to reset the register.

The 74F299 contains eight edge-triggered D-type flip-flops and the inter-stage logic necessary to perform synchronous, shift left, shift right, parallel

ORDERING INFORMATION

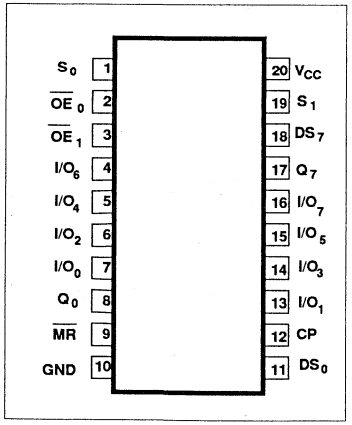
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F299N
20-Pin Plastic SOL	N74F299D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

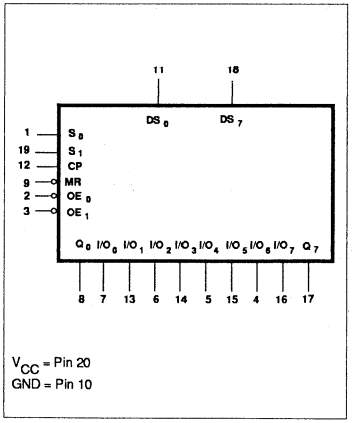
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS_0	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS_7	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S_0, S_1	Mode Select inputs	1.0/2.0	20µA/1.2mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_0, Q_7	Serial outputs	50/33	1.0mA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

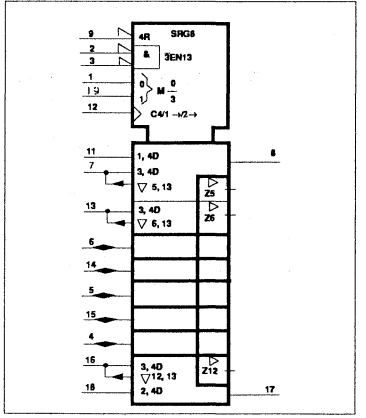
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

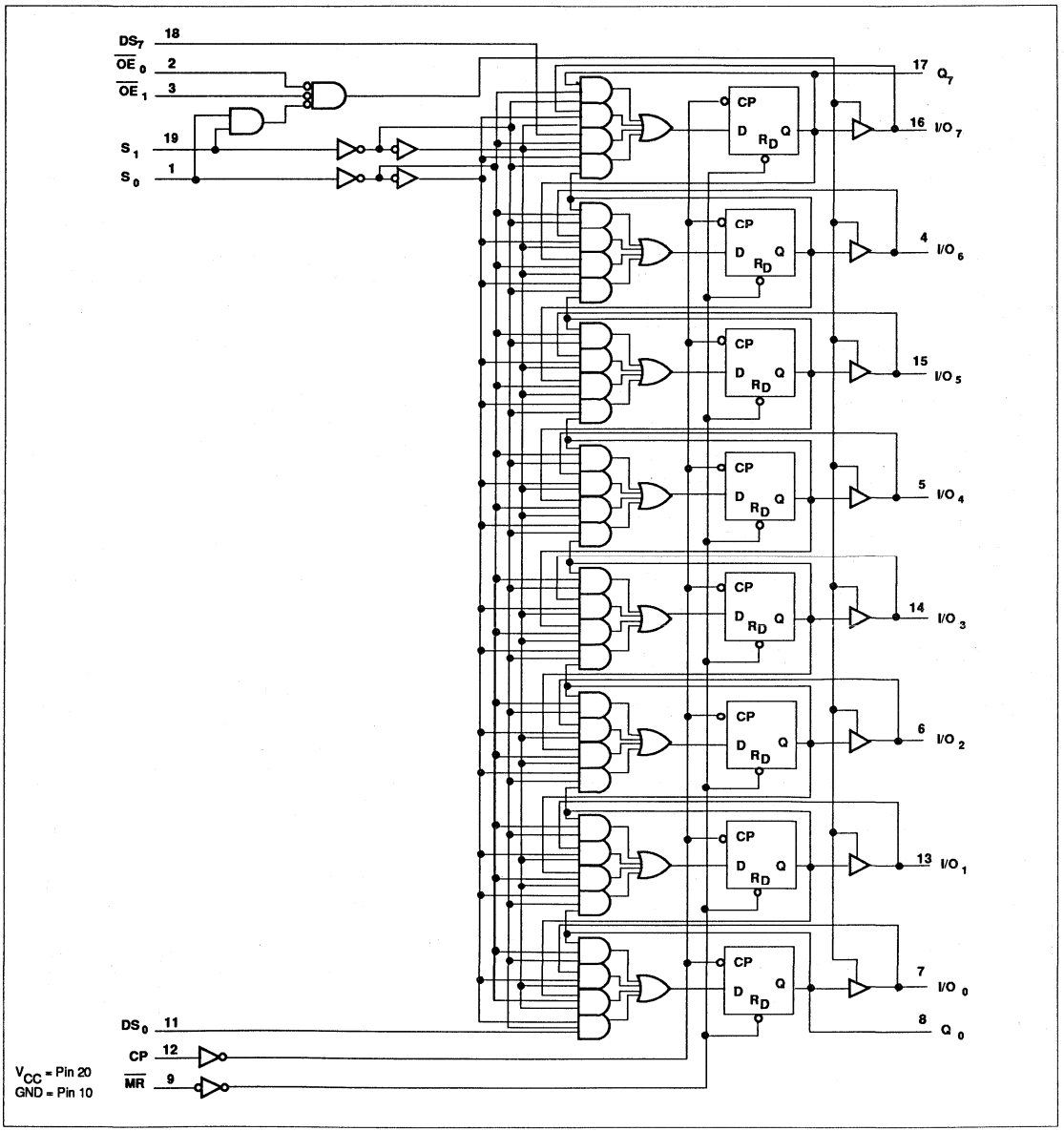


DESCRIPTION (Continued)

load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting on longer words. A Low signal on $\overline{MR}$ overrides the Select and and CP input and resets the flip-flops.

All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set up and hold times, relative to the rising edge of clock are observed. A High signal on either $\overline{OE}_0$ or $\overline{OE}_1$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OE}_n$	$\overline{MR}$	S_1	S_0	CP	
L	L	X	X	X	Asynchronous Reset; Q_0-Q_7=Low
L	H	H	H	↑	Parallel load ; $I/O_n \rightarrow Q_n$ (I/O_n outputs disabled)
L	H	L	H	↑	Shift right ; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
L	H	H	L	↑	Shift left ; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs in High Z

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Q_0, Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_0, Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_0, Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_0, Q_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} =MAX, V_I = 7.0V					100	µA
		I/O_n	V_{CC} =5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	S_0, S_1	V_{CC} = MAX, V_I = 0.5V					-1.2	mA
		others						-0.6	mA
I_{IH}+I_{OZH}	Off state output current, High-level voltage applied	I/O_n only	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC}= MAX				55	60	mA
		I_{CCL}					70	90	mA
		I_{CCZ}					65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	I/O	Waveform 1	70	100		70		MHz
		Q_n		85	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0 or Q_7		Waveform 1	4.0 4.5	5.0 6.0	7.5 8.0	3.5 4.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n		Waveform 1	4.0 4.0	6.0 6.5	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_0 or Q_7		Waveform 2	5.5	7.5	9.5	5.5	10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n		Waveform 2	5.5	7.5	10.0	5.5	10.5	ns
t_{PZH} t_{PZL}	Output Enable time Sn, $\overline{OE}$ to I/O_n		Waveform 4 Waveform 5	3.5 4.0	6.0 7.5	8.0 10.0	3.5 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time Sn, $\overline{OE}$ to I/O_n		Waveform 4 Waveform 5	2.5 1.5	4.5 2.5	7.0 5.5	2.5 1.5	8.0 6.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0 or S_1 to CP	Waveform 3	6.5 6.5			7.5 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0 or S_1 to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n, DS_L or DS_R to CP	Waveform 3	3.5 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n, DS_L or DS_R to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	5.0 4.5			5.0 4.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.0		ns

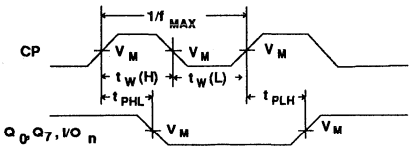
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	I/O	Waveform 1	70	100		70		MHz
		Q_n		85	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_o or Q_7		Waveform 1	4.0 4.5	5.0 6.0	7.5 8.0	3.5 4.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n		Waveform 1	4.0 4.0	6.0 6.5	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_o or Q_7		Waveform 2	5.5	7.5	9.5	5.5	10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n		Waveform 2	5.5	7.5	10.0	5.5	10.5	ns
t_{PZH} t_{PZL}	Output Enable time S_n, $\overline{OE}$ to I/O_n		Waveform 4 Waveform 5	3.5 4.0	6.0 7.5	8.0 10.0	3.5 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time S_n, $\overline{OE}$ to I/O_n		Waveform 4 Waveform 5	2.5 1.5	4.5 2.5	7.0 6.5	2.5 1.5	8.0 6.5	ns

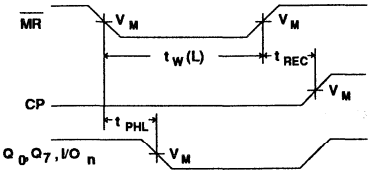
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0 or S_1 to CP	Waveform 3	6.5 6.5			7.5 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0 or S_1 to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_0, DS_0 or DS_7 to CP	Waveform 3	3.5 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_0, DS_0 or DS_7 to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	5.0 4.5			5.0 4.5		ns
$t_w(H)$ $t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.0		ns

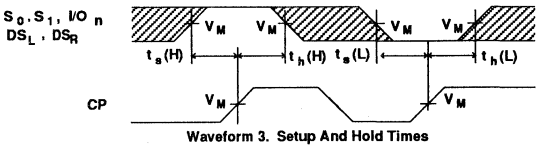
AC WAVEFORMS



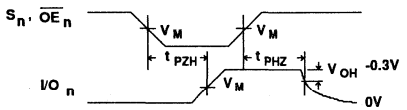
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



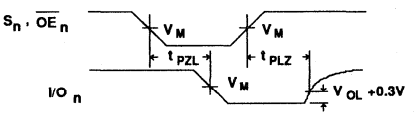
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Setup And Hold Times



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

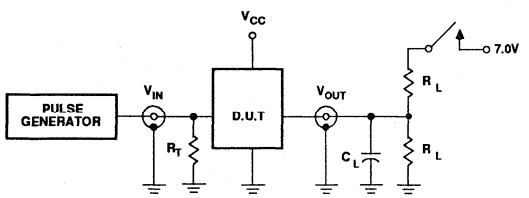


Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

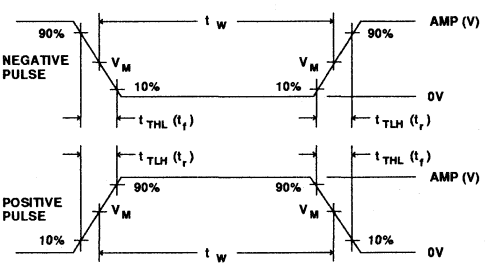
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0366
ECN No.	93020
Date of issue	April 22, 1988
Status	Product Specification
FAST Products	

FAST 74F322 Register

8-Bit Serial/Parallel Register With Sign Extend (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F322	125 MHz	60mA

FEATURES

- **Multiplexed parallel I/O ports**
- **Separate serial input and output**
- **Sign extend function**
- **3-state outputs for bus applications**
- **Direct Overriding Clear**

DESCRIPTION

The 74F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend, and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the registers.

The 'F322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A Low signal on $\overline{RE}$ enables shifting or parallel loading, while a High signal enables the hold mode. A High signal on S/$\overline{P}$ enables shift right, while a Low signal disables the 3-state output buffers and enables parallel loading. In the shift right mode a High signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A Low signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents thus performing the sign extend function. A High signal on $\overline{OE}$ disables the 3-state output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

ORDERING INFORMATION

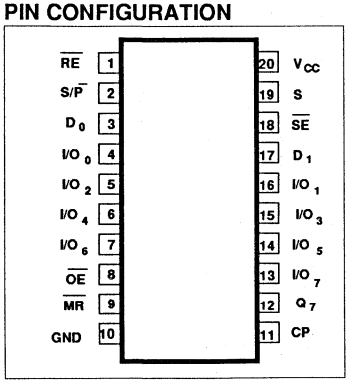
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F322N
20-Pin Plastic SOL	N74F322D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

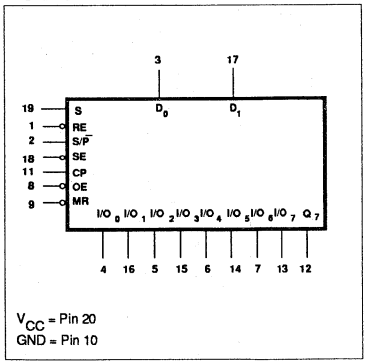
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Serial data inputs	1.0/1.0	20µA/0.6mA
S	Serial data select input	1.0/2.0	20µA/1.2mA
$\overline{SE}$	Sign Extend input	1.0/3.0	20µA/1.8mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
S/$\overline{P}$	Serial (High) or Parallel (Low) mode control input	1.0/1.0	20µA/0.6mA
$\overline{RE}$	Register Enable input (active-Low)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_7	Bi-state serial output	50/33	1.0mA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

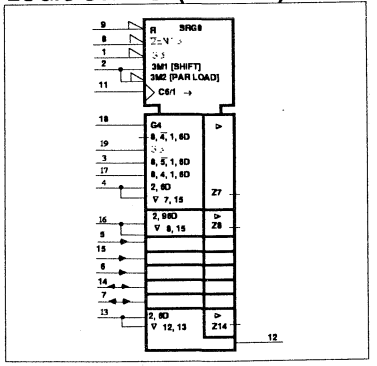
PIN CONFIGURATION



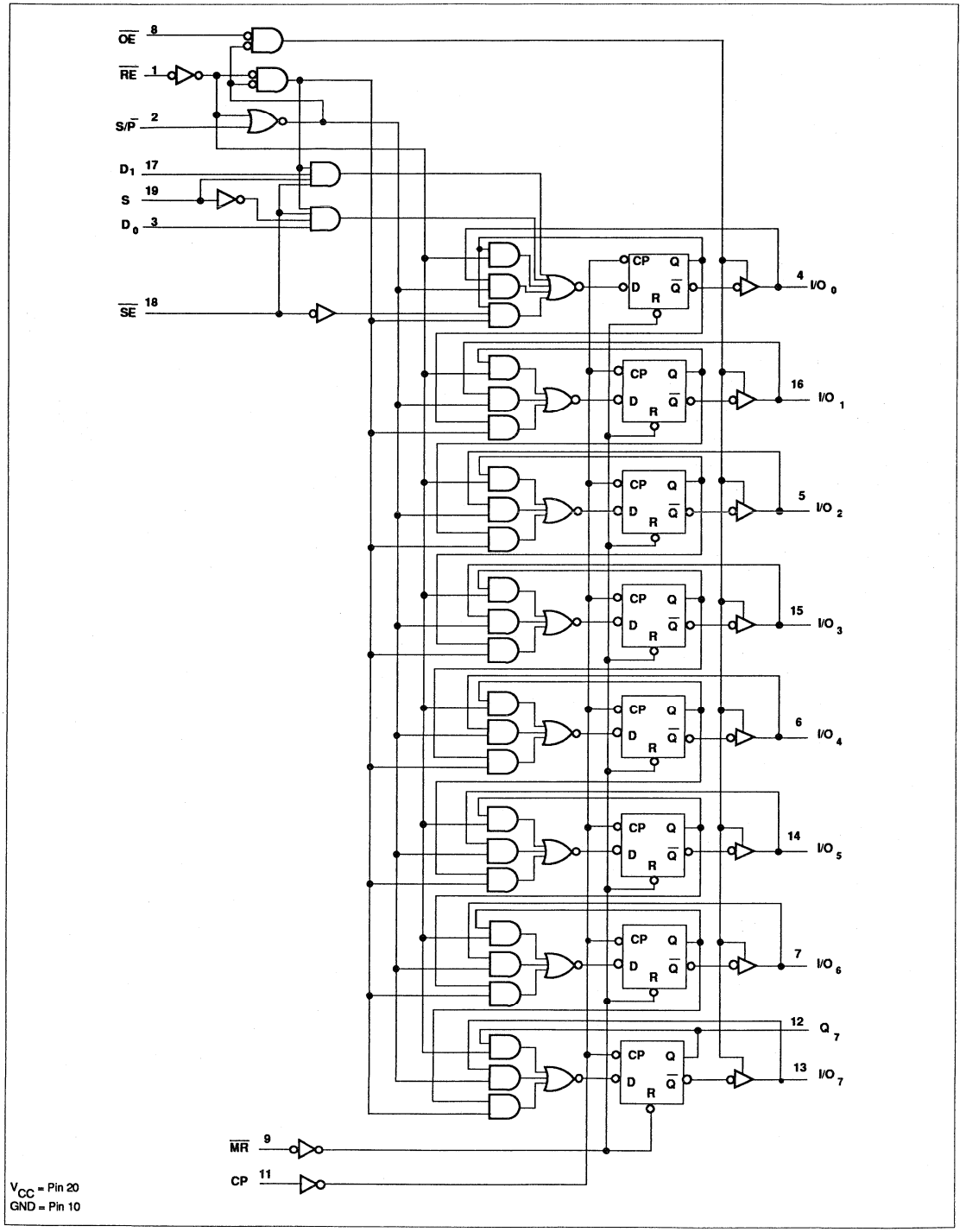
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS									OPERATING MODE
$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O_0	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7	Q_7	
L	H	X	X	X	L	X	L	L	L	L	L	L	L	L	L	Clear
L	X	H	X	X	L	X	L	L	L	L	L	L	L	L	L	
H	L	L	X	X	X	↑	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_7	Parallel load
H	L	H	H	L	L	↑	D_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_6	Shift right
H	L	H	H	H	L	↑	D_1	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_6	
H	L	H	L	X	L	↑	O_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_6	Sign extend
H	H	X	X	X	L	X	NC	NC	NC	NC	NC	NC	NC	NC	NC	Hold
X	L	L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	NC	3-State
X	X	X	X	X	H	↕	Z	Z	Z	Z	Z	Z	Z	Z	NC	

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
I_0-I_7 = The level of the steady state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_7) are isolated from the I/O terminal.
D_0-D_7 = The level of the steady state inputs to the serial multiplexer input.
O_0-O_7 = The level of the respective Q_n flip-flop prior to the last clock Low-to-High transition.
* = When the input is High, all I/O terminals are at the high impedance state, sequential operation or clearing of the register is not affected.
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_7	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		I/O_n	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	$\overline{SE}$	V_{CC} = MAX, V_I = 0.5V					-1.8	mA
		S						-1.2	mA
		others						-0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied		V_{CC} = MAX, V_I = 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	75	mA
		I_{CCL}					60	90	mA
		I_{CCZ}					65	95	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

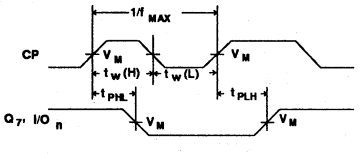
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 4.5	6.0 7.0	9.0 9.5	4.0 4.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_7	Waveform 1	4.5 5.0	6.5 6.5	9.0 9.0	4.5 5.0	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	6.5	9.5	4.5	10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_7	Waveform 2	5.0	6.5	9.5	4.5	10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	3.0 5.5	5.0 7.5	8.0 10.5	3.0 5.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	2.0 1.0	4.0 2.5	6.5 5.5	2.0 1.0	7.5 6.0	ns
t_{PZH} t_{PZL}	Output Enable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.0 6.0	6.0 8.0	9.0 11.0	3.5 5.5	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.0 2.0	6.0 4.0	9.0 7.0	3.5 2.0	10.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{RE}$ to I/O_n	Waveform 4 Waveform 5	8.0 9.0	9.5 11.0	12.5 14.0	7.0 8.0	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{RE}$ to I/O_n	Waveform 4 Waveform 5	6.5 4.5	8.5 6.5	11.5 9.5	5.5 4.0	13.0 10.5	ns

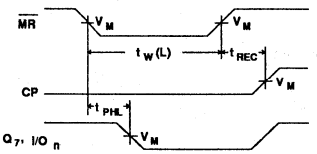
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{RE}$ to CP	Waveform 3	8.0 12.5			9.5 14.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{RE}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_0, D_1 or I/O_n to CP	Waveform 3	4.0 4.5			6.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_0, D_1 or I/O_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SE}$ to CP	Waveform 3	5.5 5.0			7.0 5.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SE}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S/$\overline{P}$ to CP	Waveform 3	10.5 9.5			11.0 10.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to CP	Waveform 3	4.0 8.5			4.5 9.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S or S/$\overline{P}$ to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

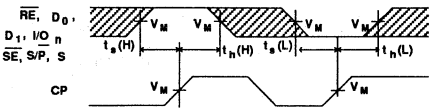
AC WAVEFORMS



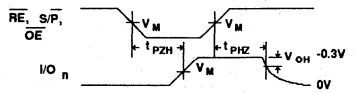
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



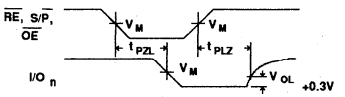
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data Setup And Hold Times



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

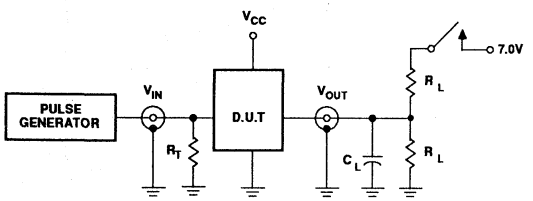


Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

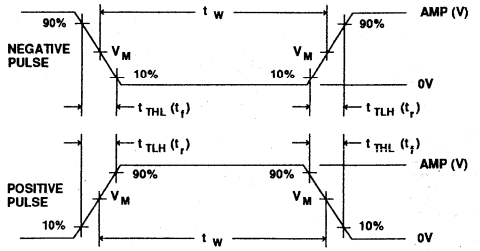
NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0367
ECN No.	98987
Date of issue	March 1, 1990
Status	Product Specification
FAST Products	

FAST 74F323 Register

8-Bit Universal Shift/Storage Register With Synchronous Reset and Common I/O pins (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F323	115 MHz	55mA

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional serial inputs and outputs for expansion**
- **Four operating modes: Shift left, shift right, load and store**
- **3-state outputs for bus oriented applications**

DESCRIPTION

The 74F323 is an 8-bit universal shift /storage register with 3-state outputs.Its function is similar to the 74F299 with the exception of synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin counts. Separate serial inputs and outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. Four modes of operation are possible: Hold (store), shift left, shift right and parallel load.

The 74F323 contains eight edge-triggered D-type flip-flops and the interstage logic

ORDERING INFORMATION

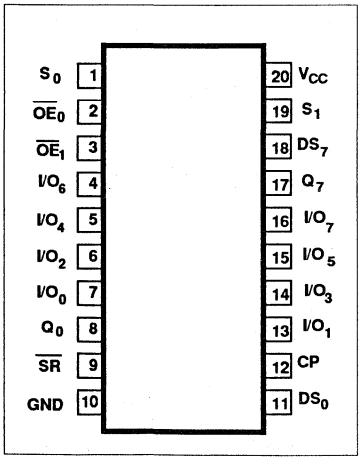
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F323N
20-Pin Plastic SOL	N74F323D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

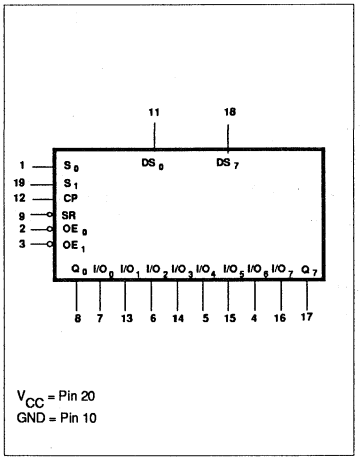
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS_0	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS_7	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S_0 ,S_1	Mode select inputs	1.0/2.0	20µA/1.2m
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$,$\overline{OE}_1$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_0 ,Q_7	Serial outputs	50/33	20µA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

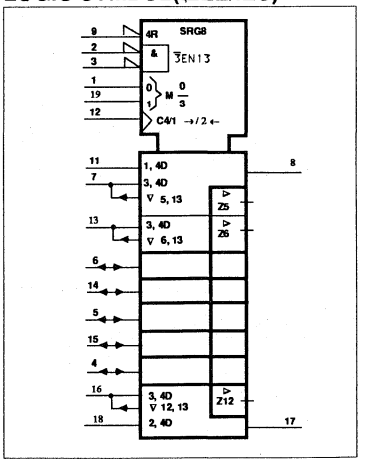
PIN CONFIGURATION



LOGIC SYMBOL

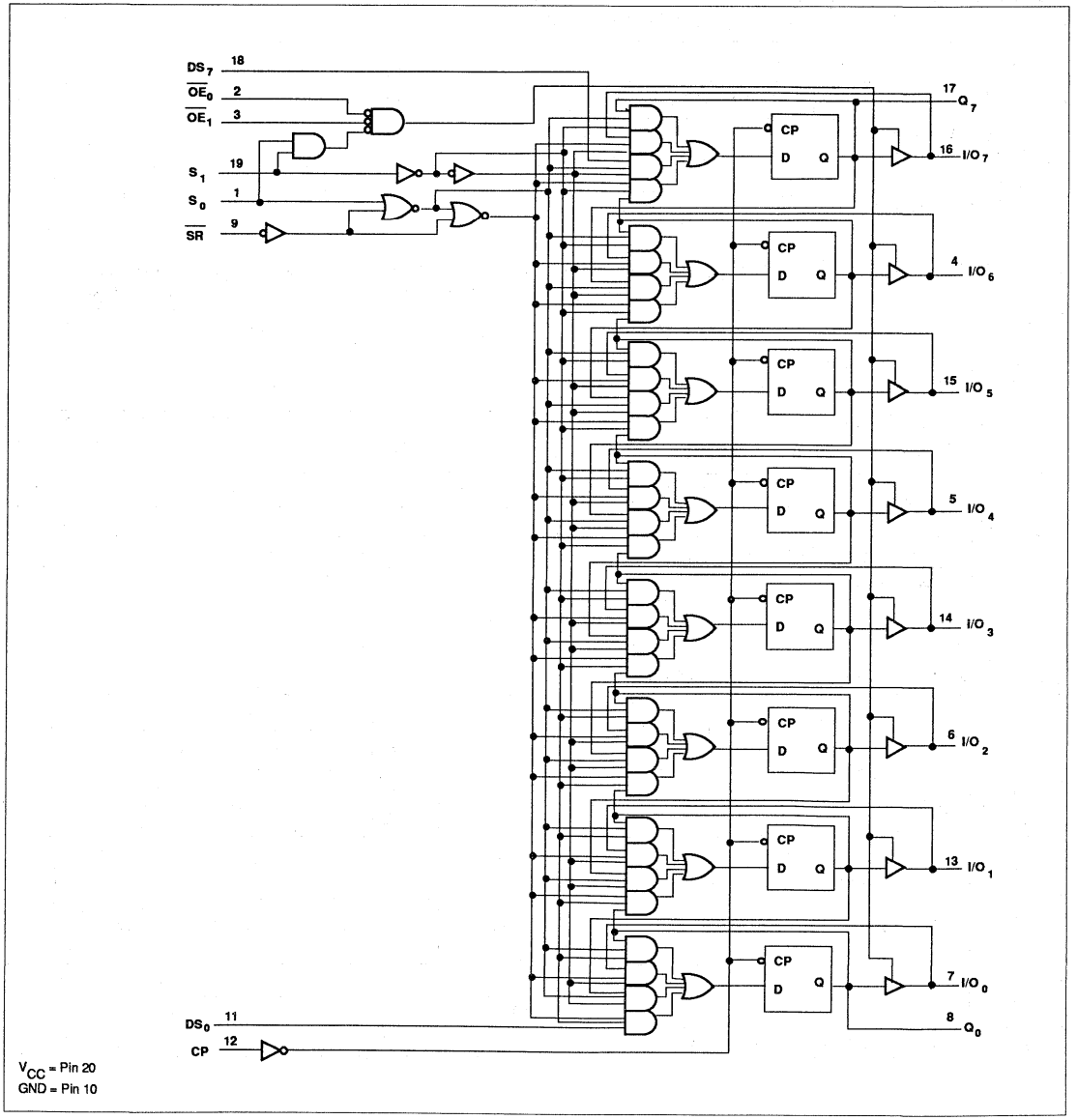


LOGIC SYMBOL(IEEE/IEC)



necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operations is determined by S_0 and S_1, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words. A Low signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of clock. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set up and hold times, relative to the rising edge of clock are observed. A high signal on either $\overline{OE}_0$ or $\overline{OE}_1$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OE}_n$	$\overline{SR}$	S_1	S_0	CP	
L	L	X	X	↑	Synchronous Reset; Q_0-Q_7=Low
L	H	H	H	↑	Parallel load ; $I/O_n \rightarrow Q_n$
L	H	L	H	↑	Shift right ; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc
L	H	H	L	↑	Shift left ; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs disabled (3-state)

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_0, Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_0, Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_0, Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_0, Q_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} =MAX, V_I = 7.0V					100	µA
		I/O_n	V_{CC} =5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	S_0, S_1	V_{CC} = MAX, V_I = 0.5V					-1.2	mA
		others						-0.6	mA
I_{IH}+I_{OZH}	Off state output current, High-level voltage applied	I/O_n only	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC}= MAX				55	75	mA
		I_{CCL}					65	90	mA
		I_{CCZ}					55	85	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

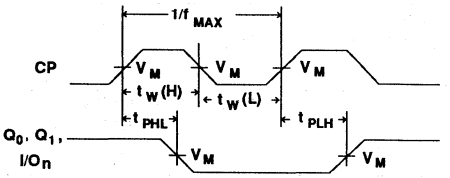
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	I/O	Waveform 1	70	100		70		MHz
		Q_n		85	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_o or Q_7		Waveform 1	4.0 3.5	6.0 6.0	8.5 8.5	3.5 4.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n		Waveform 1	4.0 5.0	6.0 6.5	9.0 9.5	4.0 4.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time S_n, $\overline{OE}$ to I/O_n		Waveform 4 Waveform 5	3.5 4.0	6.0 8.0	9.0 11.0	3.5 4.0	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time S_n, $\overline{OE}$ to I/O_n		Waveform 4 Waveform 5	2.5 1.5	5.0 3.0	7.5 5.5	2.5 1.5	8.0 6.5	ns

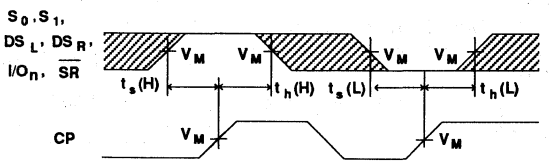
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0 or S_1 to CP	Waveform 2	6.5 6.5			7.5 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0 or S_1 to CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_0, DS_0 or DS_7 to CP	Waveform 2	3.5 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_0, DS_0 or DS_7 to CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SR}$ to CP	Waveform 2	7.0 7.0			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SR}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.5 3.5			4.0 4.0		ns

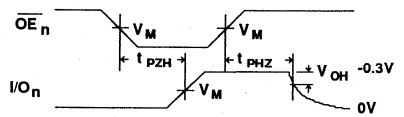
AC WAVEFORMS



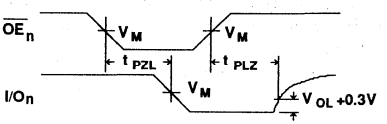
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data, Select and Reset Setup And Hold Times



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

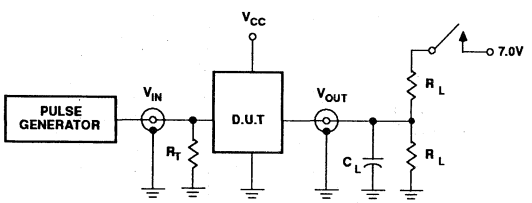


Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

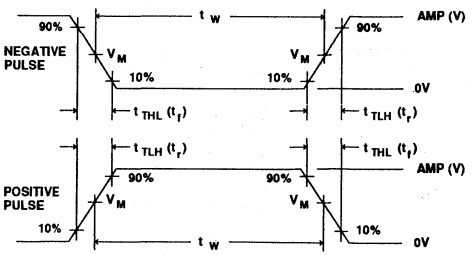
NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0368
ECN No.	96093
Date of issue	March 20, 1989
Status	Product Specification
FAST Products	

FAST 74F350
Shifter

4-Bit Shifter

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F350	5.2ns	24mA

FEATURES

- **Shifts 4 bits of data to 0,1,2,3 places under control of two select lines**
- **3-state outputs for bus organized systems**

DESCRIPTION

The 74F350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers.The 'F350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical-- with logic zeros filled in at either end of the shifting field.

2.Arithmetic-- where the sign bit is extended during a shift down.

3. End around-- where the data word forms a continuous loop.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F350N
16-Pin Plastic SO	N74F350D

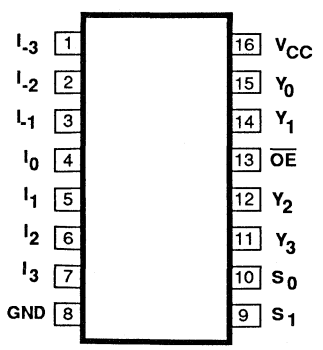
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{-n}, I_n	Data inputs	1.0/2.0	20µA/1.2mA
S_0, S_1	Select inputs (active Low)	1.0/2.0	20µA/1.2mA
$\overline{OE}$	Output Enable input (active Low)	1.0/2.0	20µA/1.2mA
Y_0 - Y_3	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

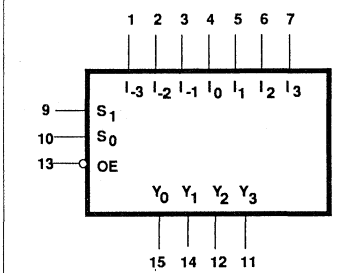
The 3-state outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active Low Output Enable ($\overline{OE}$) controls the state of the outputs. The outputs are in the high impedance "off " state when $\overline{OE}$ is High, and they are active when $\overline{OE}$ is Low.

PIN CONFIGURATION



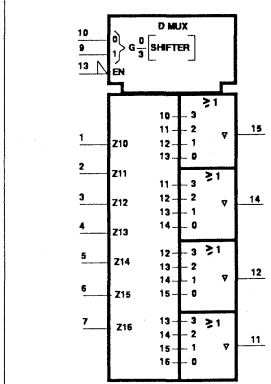
TOP VIEW

LOGIC SYMBOL

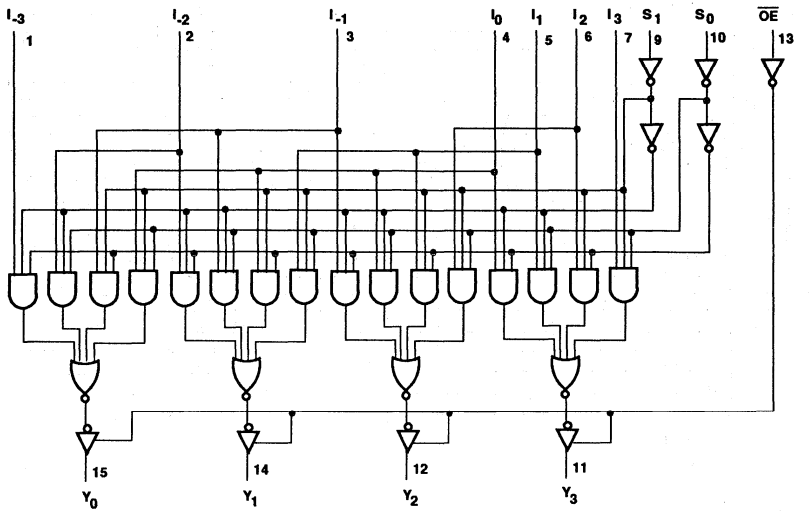


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



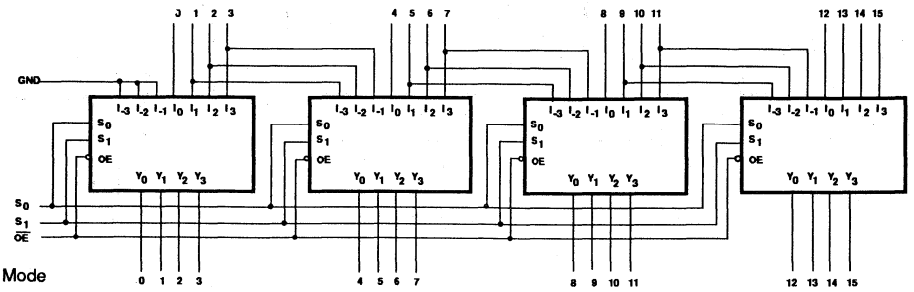
V_{CC}= pin 16
GND= Pin 8

FUNCTION TABLE

INPUTS										OUTPUTS			
$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

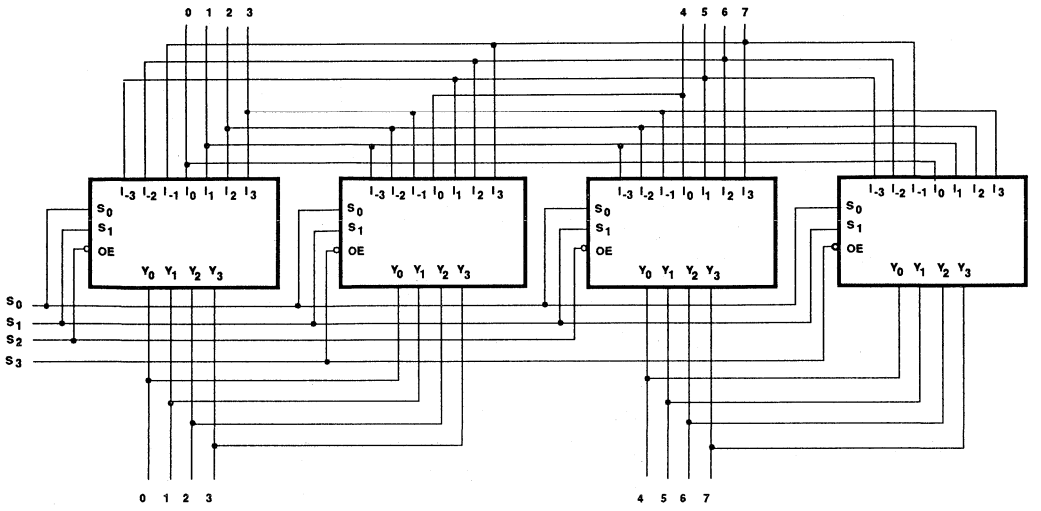
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
D_n = High or Low state of referenced I_n input

APPLICATION for 16-bit shift up 0,1,2, or 3 places



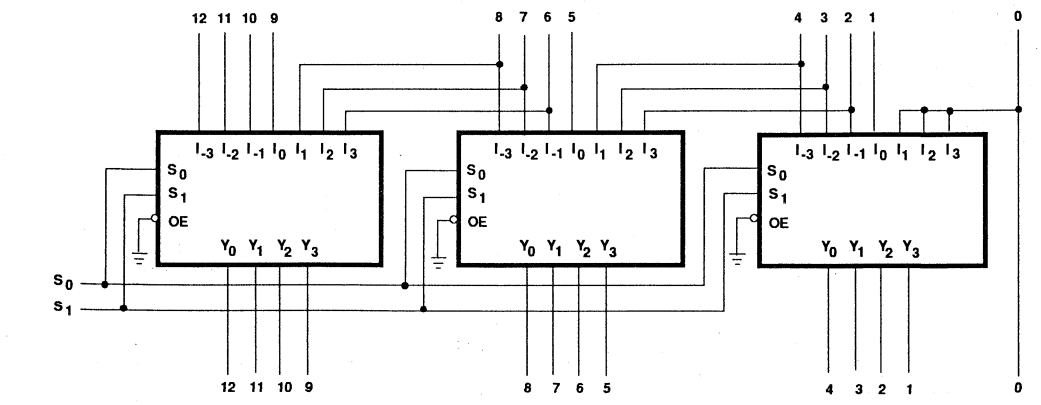
S_0	S_1	Mode
L	L	No shift
H	L	Shift 1 place
L	H	Shift 2 places
H	H	Shift 3 places

APPLICATION for 8-bit end around shift 0,1,2,3,4,5,6,7 places



S_2	S_1	S_0	Mode
L	L	L	No shift
L	L	H	Shift end around 1
L	H	L	Shift end around 2
L	H	H	Shift end around 3
H	L	L	Shift end around 4
H	L	H	Shift end around 5
H	H	L	Shift end around 6
H	H	H	Shift end around 7

APPLICATION for 13-bit two's complement scaler



S_1	S_0		Scale
L	L	÷8	1/8
L	H	÷4	1/4
H	L	÷2	1/2
H	H	No change	1

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			22	35	mA
		I_{CCL}				26	41	mA
		I_{CCZ}				26	42	mA

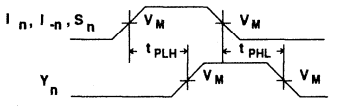
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

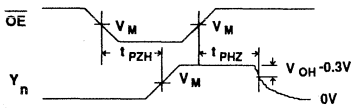
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 2.5	4.5 4.0	6.0 5.5	3.0 2.5	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 1	4.0 3.0	7.8 6.5	10.0 8.5	4.0 3.0	11.0 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.5 4.0	5.0 7.0	7.0 9.0	2.5 4.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	2.0 2.0	3.9 4.0	5.5 5.5	2.0 2.0	6.5 6.5	ns

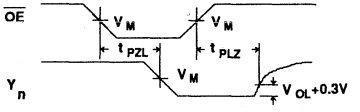
AC WAVEFORMS



Waveform 1. Propagation delay Data and Select to Output



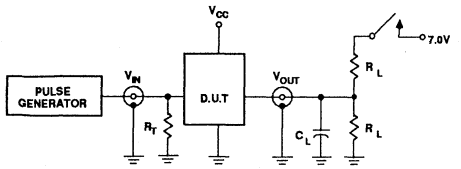
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

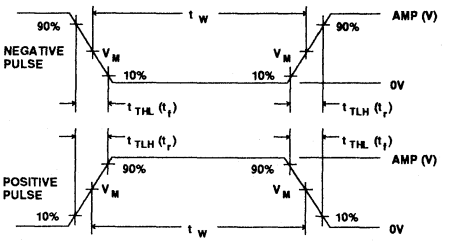
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0103
ECN No.	95946
Date of issue	March 3, 1989
Status	Product Specification
FAST Products	

FAST 74F353
Multiplexer

Dual 4-Input Multiplexer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F353	6.0ns	11mA

FEATURES

- **Inverting version of 'F253**
- **3-state outputs for bus interface and multiplex expansion**
- **Common select inputs**
- **Separate Output Enable inputs**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F353N
16-Pin Plastic SO	N74F353D

DESCRIPTION

The 74F353 has two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common Select inputs (S_0,S_1). When the individual Output Enable ($\overline{OE}_a$,$\overline{OE}_b$) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance (Hi-Z) state.

The 'F353 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two common Select inputs.

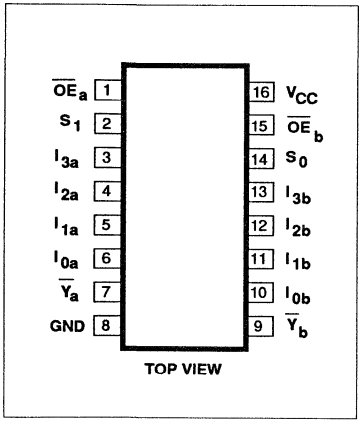
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}- I_{3a}	Port A data inputs	1.0/1.0	20µA/0.6mA
I_{0b}- I_{3b}	Port B data inputs	1.0/1.0	20µA/0.6mA
S_0, S_1	Common Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}_a$	Port A Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_b$	Port B Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$, $\overline{Y}_b$	3-state outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

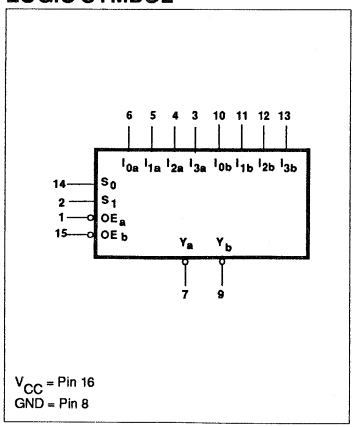
To avoid exceeding the maximum current ratings when the outputs of the 3-state devices are tied together, all but one device must be in the high-impedance state. Therefore, only one Output Enable must be active at a time.

PIN CONFIGURATION



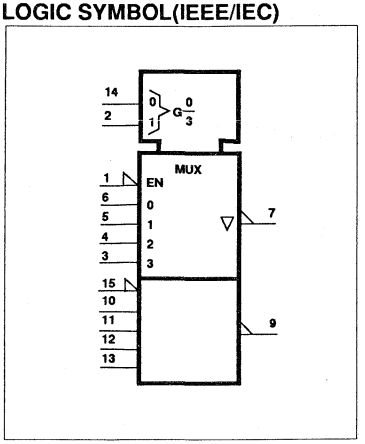
TOP VIEW

LOGIC SYMBOL

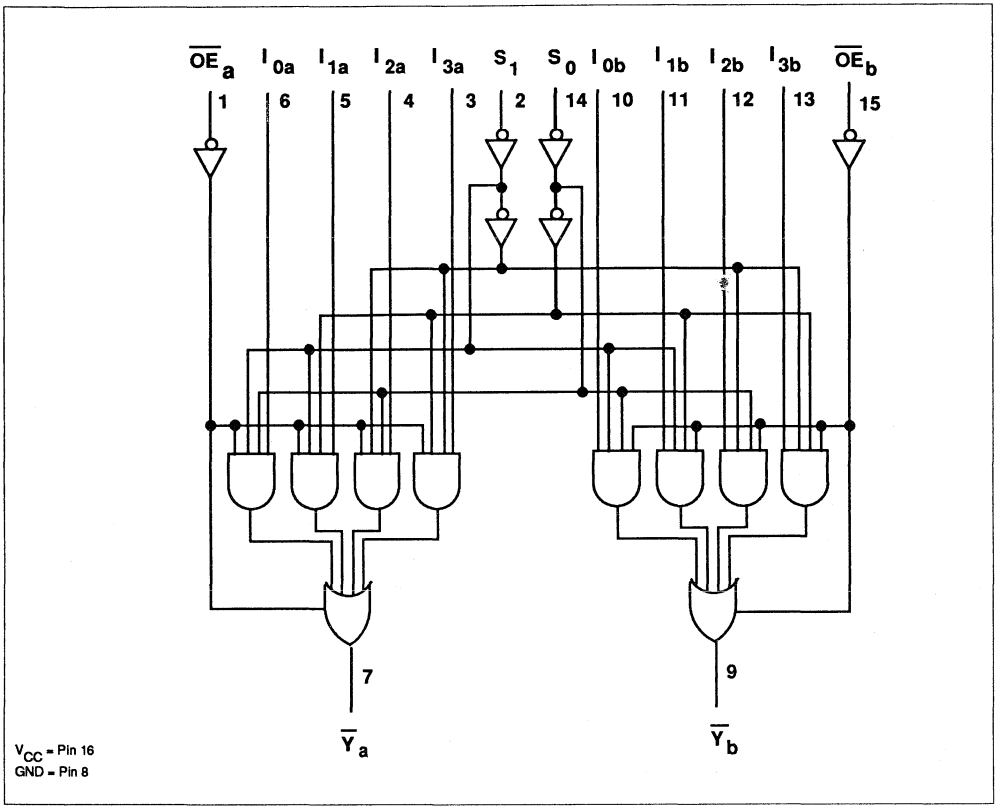


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Y}$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{OE}_n$=S_n=I_n=GND		9	14	mA
		I_{CCL}		$\overline{OE}_n$=S_n=GND, I_n=4.5V		11	20	mA
		I_{CCZ}		$\overline{OE}_n$=4.5V, S_n=I_n=GND		13	23	mA

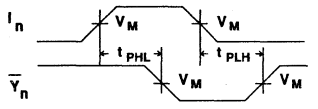
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

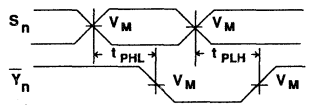
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	3.0 1.5	5.0 3.0	7.0 5.0	3.0 1.0	8.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}_n$	Waveform 2	5.0 3.0	9.0 6.0	12.0 8.5	4.5 3.0	12.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.0	6.0 6.5	8.0 8.0	3.5 3.5	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.5 1.5	4.0 2.5	5.5 6.0	2.0 1.5	6.0 7.0	ns

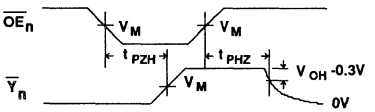
AC WAVEFORMS



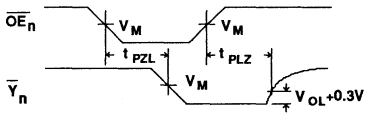
Waveform 1. Propagation Delay, Data to Output



Waveform 2. Propagation Delay, Select to Output



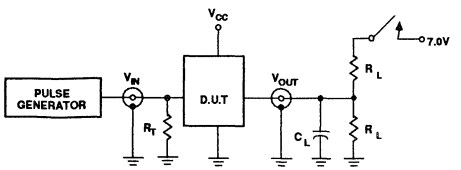
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outposts

SWITCH POSITION

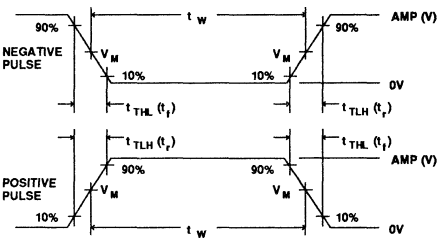
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0042
ECN No.	98496
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F365, 74F366 74F367, 74F368 Buffers/Drivers

'F365, 'F367 Hex Buffer/Driver (3-State)
'F366, 'F368 Hex Inverter Buffer/Driver (3-State)

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **High speed**
- **Bus oriented**
- **3-state buffer outputs sink 64mA**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F365, 74F367	5.0ns	36mA
74F366, 74F368	5.0ns	33mA

ORDERING INFORMATION

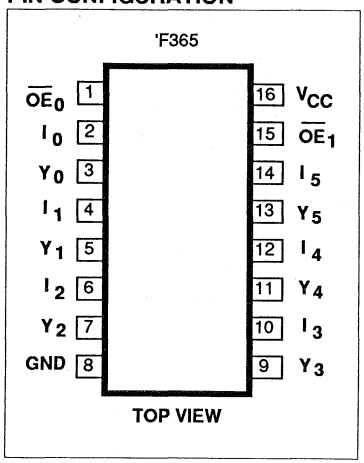
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F365N, N74F366N, N74F367N, N74F368N
16-Pin Plastic SO	N74F365D, N74F366D, N74F367D, N74F368D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

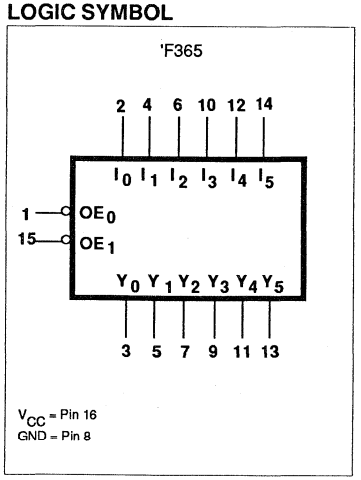
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0-I_5	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$,$\overline{OE}_1$	Output enable inputs (active Low)	1.0/0.033	20μA/20μA
Y_0- Y_5, $\overline{Y}_0$- $\overline{Y}_5$	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

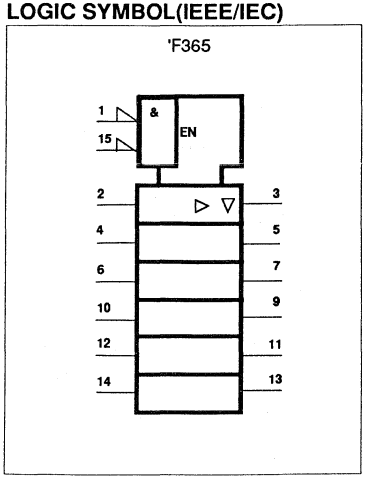
PIN CONFIGURATION



LOGIC SYMBOL

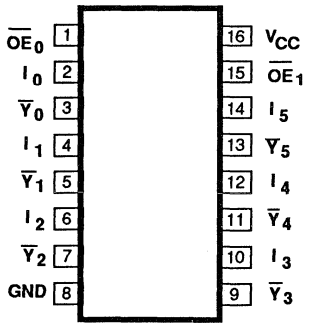


LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION

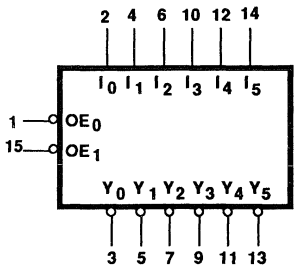
'F366



TOP VIEW

LOGIC SYMBOL

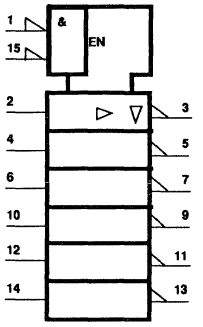
'F366



V_{CC} = Pin 16
GND = Pin 8

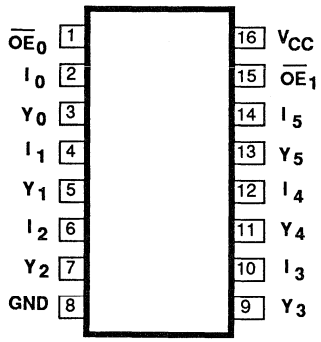
LOGIC SYMBOL(IEEE/IEC)

'F366



PIN CONFIGURATION

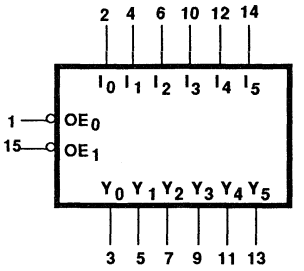
'F367



TOP VIEW

LOGIC SYMBOL

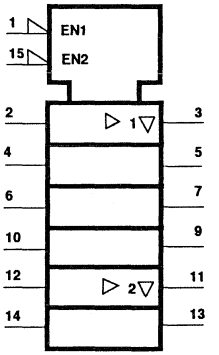
'F367



V_{CC} = Pin 16
GND = Pin 8

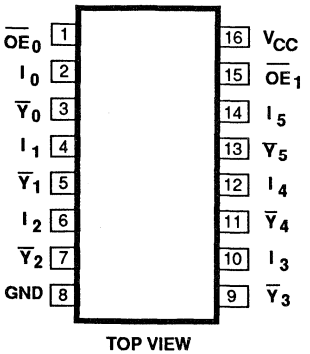
LOGIC SYMBOL(IEEE/IEC)

'F367



PIN CONFIGURATION

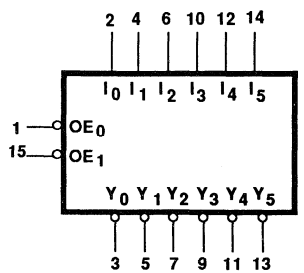
'F368



TOP VIEW

LOGIC SYMBOL

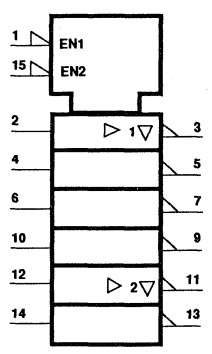
'F368



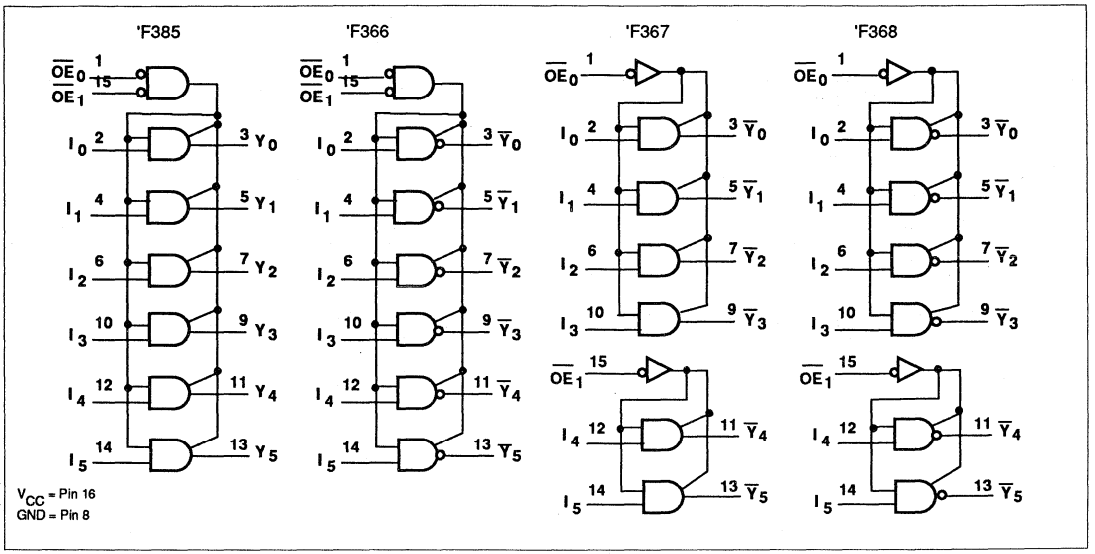
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)

'F368



LOGIC DIAGRAM



FUNCTION TABLE for 'F365 and 'F366

INPUTS			OUTPUTS	
$\overline{OE}_0$	$\overline{OE}_1$	I_n	Y_n	$\overline{Y}_n$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

FUNCTION TABLE for 'F367 and 'F368

INPUTS		OUTPUTS	
$\overline{OE}_n$	I_n	Y_n	$\overline{Y}_n$
L	L	L	H
L	H	H	L
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

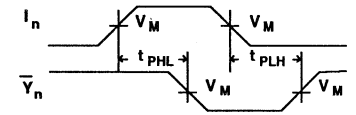
SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F365 'F367	I_{CCH}	V_{CC} = MAX				25	35	mA
			I_{CCL}					47	62	mA
			I_{CCZ}					35	48	mA
		'F366 'F368	I_{CCH}	V_{CC} = MAX				18	25	mA
			I_{CCL}					47	62	mA
			I_{CCZ}					35	48	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

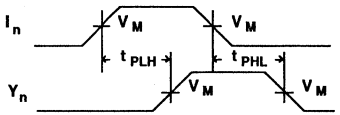
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	'F366, 'F368	Waveform 1	3.0 2.0	5.0 3.0	6.5 5.0	3.0 1.5	7.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	'F365, 'F367	Waveform 2	2.5 2.5	4.5 5.5	6.5 7.0	2.0 2.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F365, 'F366	Waveform 3 Waveform 4	2.5 2.5	4.0 5.0	6.5 8.0	2.5 2.5	7.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F367, 'F368	Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	6.5 6.5	2.0 2.0	7.0 7.0	ns

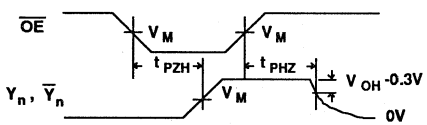
AC WAVEFORMS



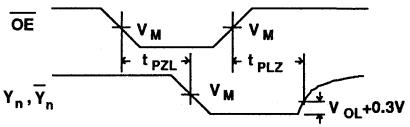
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



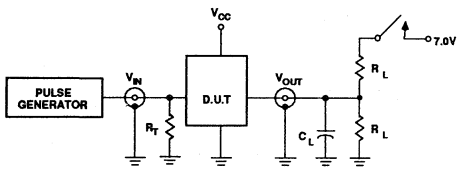
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M =1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

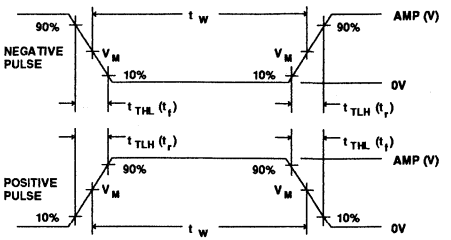
TEST	SWITCH
t_{PLZ},t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Latch/flip-flop — 74F373/74F374

74F373 Octal transparent latch (3-State)
74F374 Octal D flip-flop (3-State)

FEATURES

- 8–bit transparent latch–74F373
- 8–bit positive edge triggered register–74F374
- 3–state outputs glitch free during power–up and power–down
- Common 3–state output register
- Independent register and 3–state buffer operation

DESCRIPTION

The 74F373 is an octal transparent latch coupled to eight 3–state output devices. The two sections of the device are controlled independently by enable (E) and output enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is high. The latch remains transparent to the data input while E is high, and stores the data that is present one setup time before the high–to–low enable transition.

The 3–state output buffers are designed to drive heavily loaded 3–state busses, MOS memories, or MOS micrprocessors.

The active low output enable ($\overline{OE}$) controls all eight 3–state buffers independent of the latch operation. When $\overline{OE}$ is low, latched or transparent data appears at the output.

When $\overline{OE}$ is high, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F374 is an 8–bit edge triggered register coupled to eight 3–state output buffers. The two sections of the device are controlled independently by clock (CP) and output enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of the D input, one setup time before the low–to–high clock transition is transferred to the corresponding flip–flop's Q output.

The 3–state output buffers are designed to drive heavily loaded 3–state busses, MOS memories, or MOS microprocessors.

The active low output enable ($\overline{OE}$) controls all eight 3–state buffers independent of the register operation. When $\overline{OE}$ is low, the data in the register appears at the outputs. When $\overline{OE}$ is high, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F373	4.5ns	35mA

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F374	165MHz	55mA

ORDERING INFORMATION

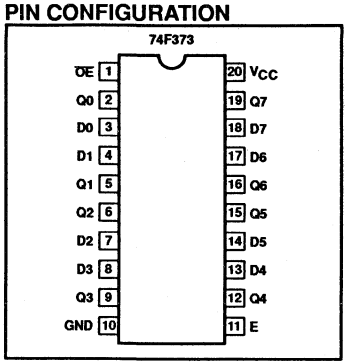
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20–pin plastic DIP	N74F373N, N74F374N
20–pin plastic SOL	N74F373D, N74F374D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

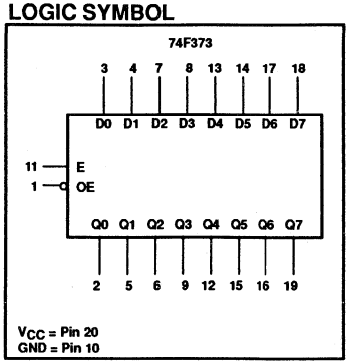
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/1.0	20μA/0.6mA
E (74F373)	Enable input (active high)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable inputs (active low)	1.0/1.0	20μA/0.6mA
CP (74F374)	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
Q0 – Q7	3–state outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

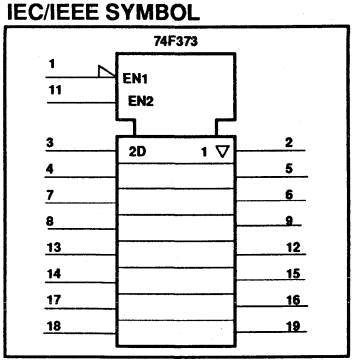
PIN CONFIGURATION



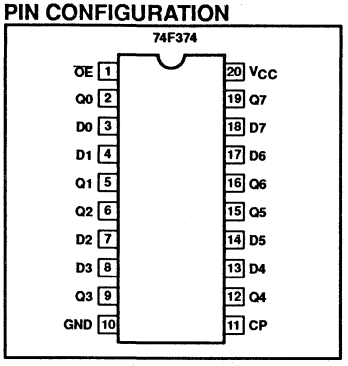
LOGIC SYMBOL



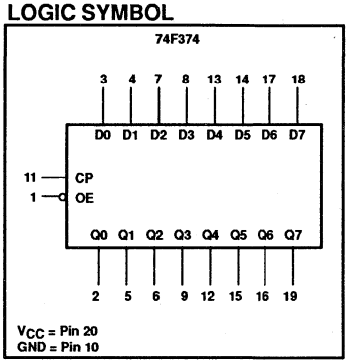
IEC/IEEE SYMBOL



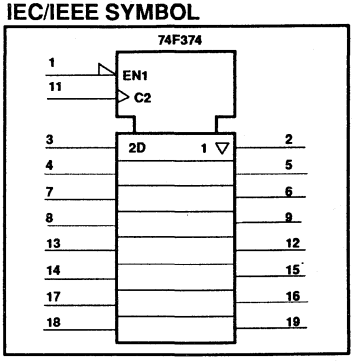
PIN CONFIGURATION



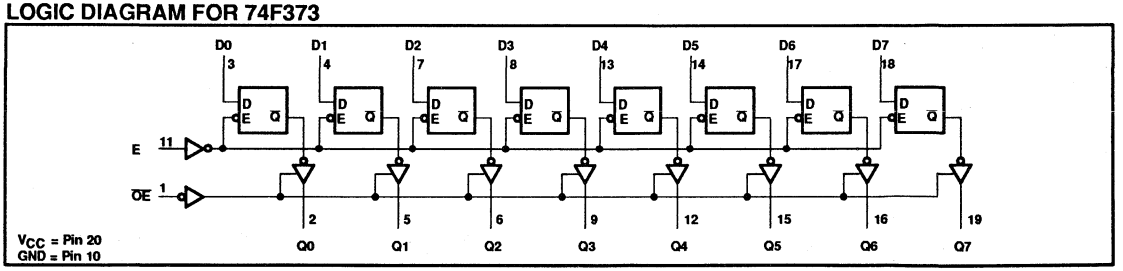
LOGIC SYMBOL



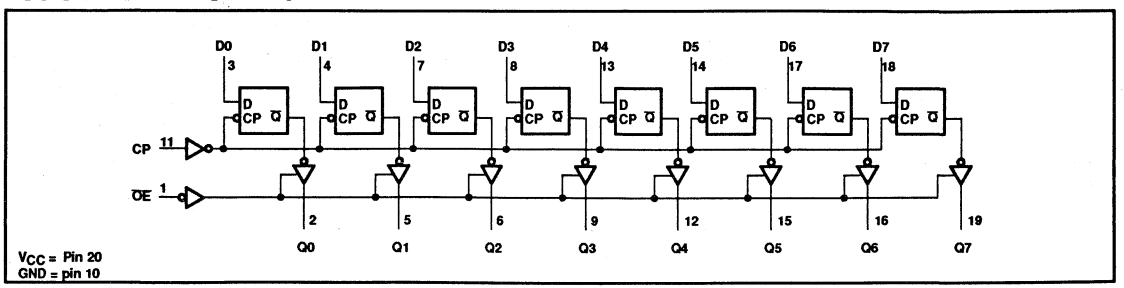
IEC/IEEE SYMBOL



LOGIC DIAGRAM FOR 74F373



LOGIC DIAGRAM FOR 74F374



FUNCTION TABLE FOR 74F373

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn	REGISTER	Q0 – Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

NOTES:
3. H = High–voltage level
4. h = High state must be present one setup time before the high–to–low enable transition
5. L = Low–voltage level
6. l = Low state must be present one setup time before the high–to–low enable transition
7. NC = No change
8. X = Don't care
9. Z = High impedance "off" state
10. ↓ = High–to–low enable transition

FUNCTION TABLE FOR 74F374

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	Q0 – Q7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↥	X	NC	NC	Hold
H	↥	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

NOTES:
1. H = High–voltage level
2. h = High state must be present one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low state must be present one setup time before the low–to–high clock transition
5. NC = No change
6. X = Don't care
7. Z = High impedance "off" state
8. ↑ = Low–to–high clock transition
9. ↥ = Not low–to–high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	48	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–3	mA
I_{OL}	Low–level output current			24	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off–state output current, high–level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short–circuit output current3		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	74F373	V_{CC} = MAX			35	60	mA
		74F374				57	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

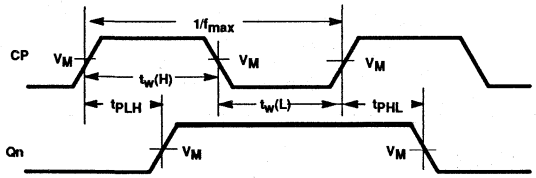
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	74F373	Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	12.0 8.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	74F373	Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	11.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	74F373	Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.0 6.0	ns
f_{max}	Maximum clock frequency	74F374	Waveform 1	150	165		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	74F374	Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	74F374	Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	74F374	Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	6.0 5.5	2.0 2.0	7.0 6.5	ns

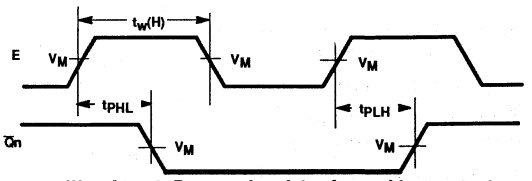
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to E	74F373	Waveform 4	0 1.0			0 1.0		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to E	74F373	Waveform 4	3.0 3.0			3.0 3.0		ns
t_w (H)	E Pulse width, high	74F373	Waveform 1	3.5			4.0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to CP	74F374	Waveform 5	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	74F374	Waveform 5	3.5 4.0			3.5 4.0		ns

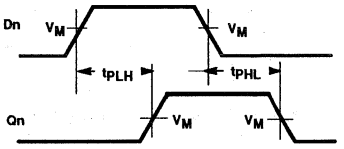
AC WAVEFORMS



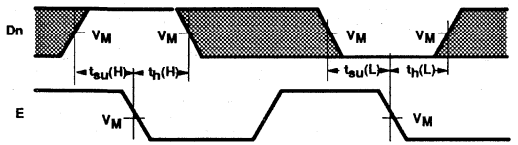
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



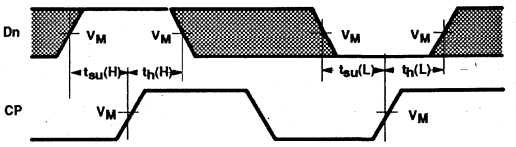
Waveform 2. Propagation delay for enable to output and enable pulse width



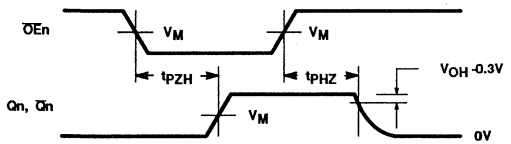
Waveform 3. Propagation delay for data to output



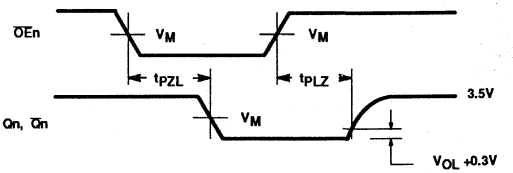
Waveform 4. Data setup time and hold times



Waveform 5. Data setup time and hold times



Waveform 6. 3-state output enable time to high level and output disable time from high level



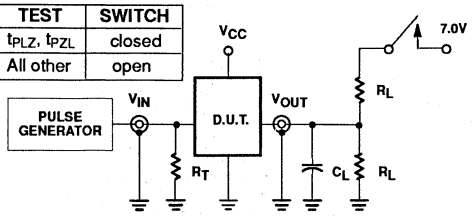
Waveform 7. 3-state output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



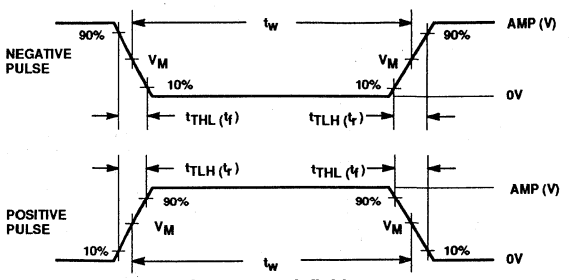
Test circuit for 3–state outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Octal D-type flip-flop with enable — 74F377/377A

FEATURES

- High impedance inputs for reduced loading (20μA in Low and High states)
- Ideal for addressable register applications
- Enable for address and data synchronization applications
- Eight edge–triggered D–type flip–flops
- Buffered common clock
- See 'F273 for Master Reset version
- See 'F373 for transparent latch version
- See 'F374 for 3–State version
- 'F377A improved AC, DC, f_{MAX} and functionality

DESCRIPTION

The 74F377 has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F377	120MHz	65mA
74F377A	165MHz	29mA

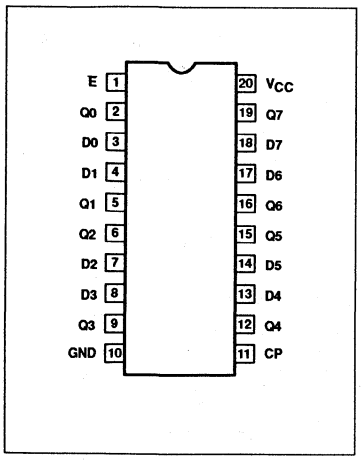
ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C
20–pin plastic DIP	N74F377N/N74F377AN
20–pin plastic SOL	N74F377D/N74F377AD

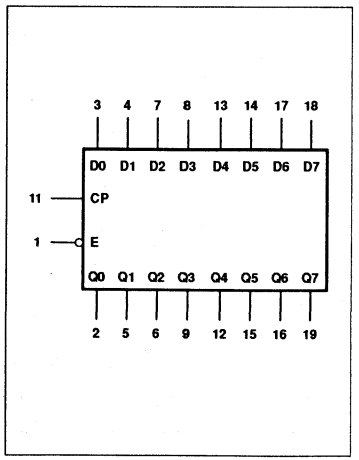
INPUT AND OUTPUT LOADING AND FAN–OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/0.033	20μA/20μA
CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
$\overline{E}$	Enable input (active–Low)	1.0/0.033	20μA/20μA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

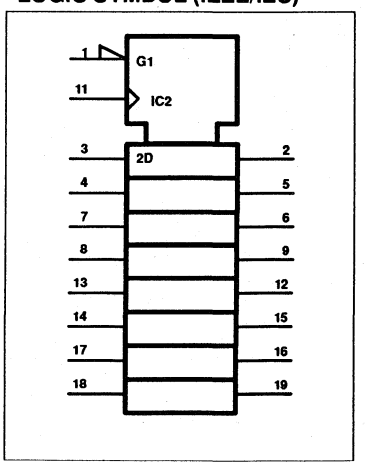
PIN CONFIGURATION



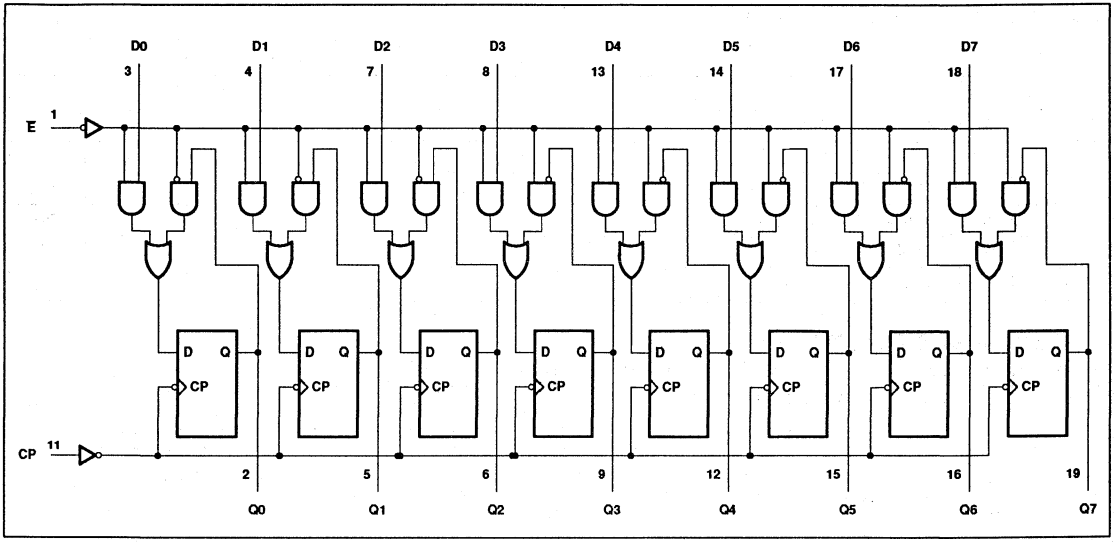
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	Dn	Qn	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage	E & CP inputs		V_{CC} = MIN, V_{IL} = 0.0V[3],	±10%V_{CC}	2.5			V
				V_{IH} = 4.5V[3], I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
		Other inputs		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High–level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current			V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OS}	Short circuit output current[4]			V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	'F377	I_{CCH}	V_{CC} = MAX			55	72	mA
			I_{CCL}	V_{CC} = MAX			70	90	mA
		'F377A	I_{CCH}	V_{CC} = MAX			27	40	mA
			I_{CCL}	V_{CC} = MAX			29	43	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. To reduce the effect of external noise during test. Special test conditions are not necessary for the '377A.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS FOR 'F377

SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			LIMITS T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	110	120		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	4.0 4.0	7.0 7.0	9.0 9.0	4.0 4.0	10.0 10.5	ns

AC CHARACTERISTICS FOR 'F377A

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	150	165		120		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	3.0 4.5	5.0 6.5	8.0 9.0	2.5 4.0	9.0 10.5	ns

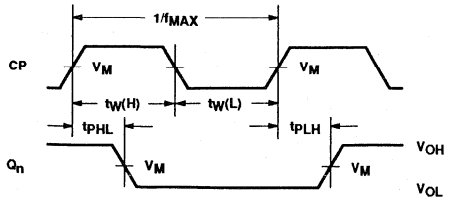
AC SETUP REQUIREMENTS FOR 'F377

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to CP	2	2.0 2.0			2.5 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CP	2	0.0 1.0			1.0 1.0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{E}$ to CP	2	3.0 4.0			3.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{E}$ to CP	2	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	Clock Pulse width High or Low	1	4.0 4.5			5.0 5.0		ns

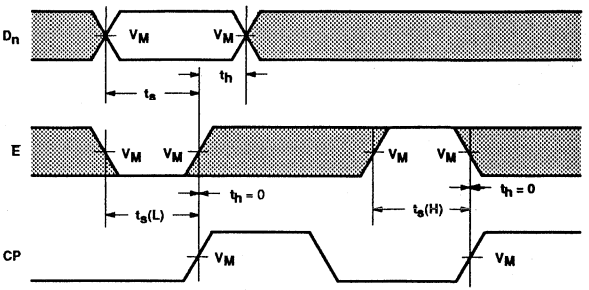
AC SETUP REQUIREMENTS FOR 'F377A

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to CP	2	2.5 2.5			2.5 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CP	2	1.0 0.0			1.0 0.0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{E}$ to CP	2	3.0 4.0			3.0 4.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{E}$ to CP	2	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	Clock Pulse width High or Low	1	4.0 4.0			5.0 4.0		ns

AC WAVEFORMS



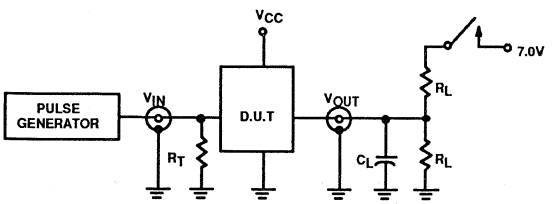
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



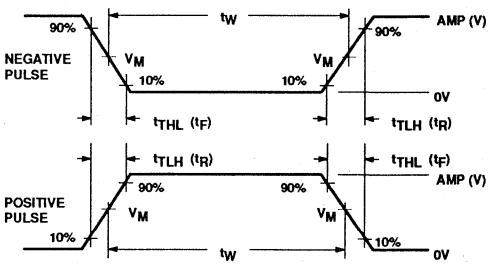
Waveform 2. Data and Enable Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3–State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0067
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Date of issue	October 5, 1989
Status	Product Specification
FAST Products	

FAST 74F378
Flip-Flop

Hex D Flip-Flop With Enable

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F378	100MHz	35mA

FEATURES

- **6-bit high-speed parallel register**
- **Positive edge-triggered D-type inputs**
- **Fully buffered common Clock and Enable inputs**
- **Input clamp diodes limit high speed termination effects**
- **Fully TTL and CMOS compatible**

DESCRIPTION

The 74F378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output. The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

ORDERING INFORMATION

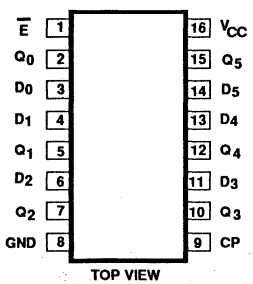
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F378N
16-Pin Plastic SO	N74F378D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_5	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_5	Data outputs	50/33	1.0mA/20mA

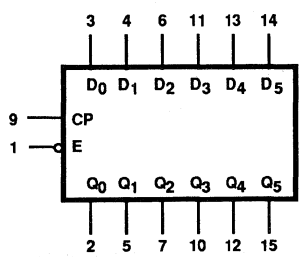
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



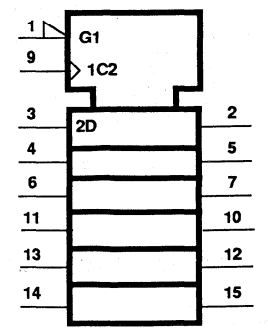
TOP VIEW

LOGIC SYMBOL

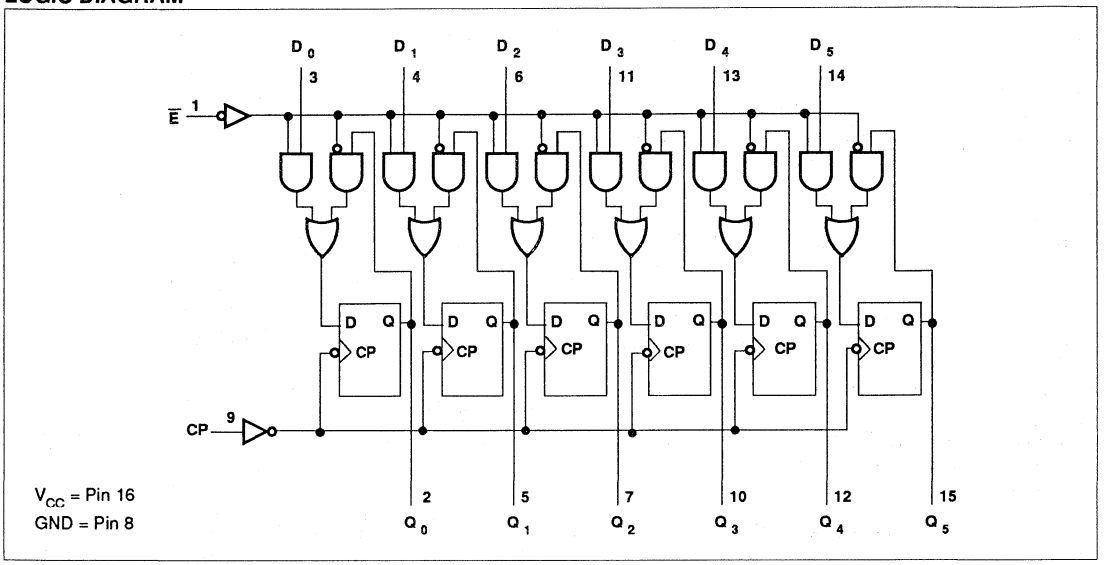


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	D_n	Q_n	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h	↑	X	no change	Hold (do nothing)
H	X	X	no change	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuitoutput current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			32	45	mA
		I_{CCL}				35	45	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable typ5
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

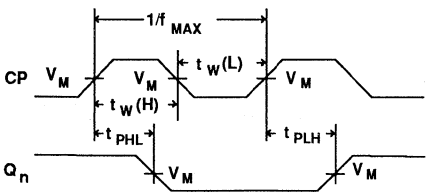
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 3.5	5.5 6.0	7.5 8.5	3.0 3.5	8.5 9.5	ns

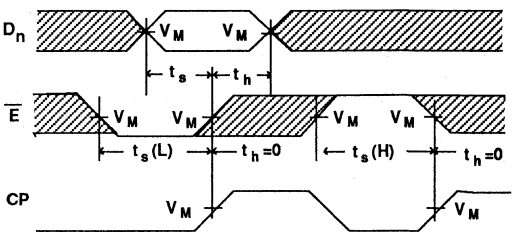
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 2	4.0 4.0			4.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 2	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	4.0 10.0			4.0 10.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
t_w(H) t_w(L)	CP Pulse width High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS



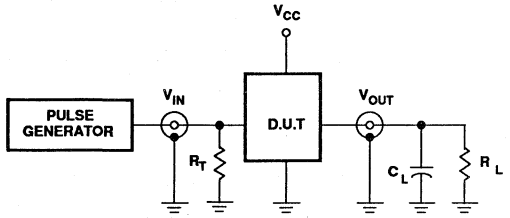
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2.
Data And Enable Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



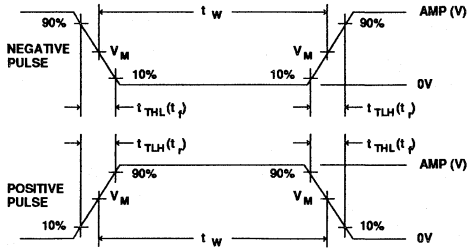
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Quad registers — 74F379/74F379A

74F379 — Quad parallel register with enable
74F379A — Quad parallel register with enable (light loading 74F379)

FEATURES

- Edge–triggered D–type inputs
- Buffered positive edge–triggered clock
- Buffered common enable input
- True and complementary outputs
- 74F379A offers light loading PNP inputs (I_{IL} = –20μA)

DESCRIPTION

The 74F379/379A are 4–bit registers with buffered common enable ($\overline{E}$). These devices are similar to the 74F175 but feature the common enable rather than common master reset.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F379	120MHz	28mA
74F379A	200MHz	29mA

ORDERING INFORMATION

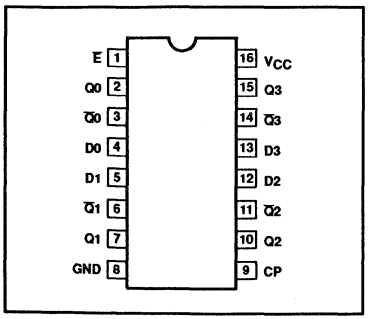
DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16–pin plastic DIP	N74F379N, N74F379AN
16–pin plastic SO	N74F379D, N74F379AD

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

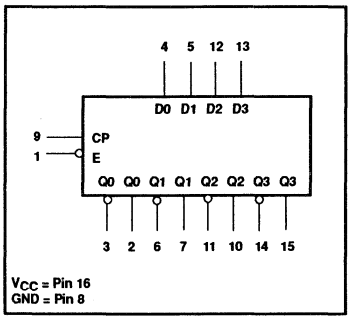
TYPE	PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F379	D0 – D3	Data inputs	1.0/1.0	20μA/0.6mA
	CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
	$\overline{E}$	Enable input (active low)	1.0/1.0	20μA/0.6mA
74F379A	D0 – D3	Data inputs	1.0/0.033	20μA/20μA
	CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
	$\overline{E}$	Enable input (active low)	1.0/0.033	20μA/20μA
	Q0 – Q3	True outputs	50/33	1.0mA/20mA
	$\overline{Q}$0 – $\overline{Q}$3	Complementary outputs	50/33	15mA/20mA

Note to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

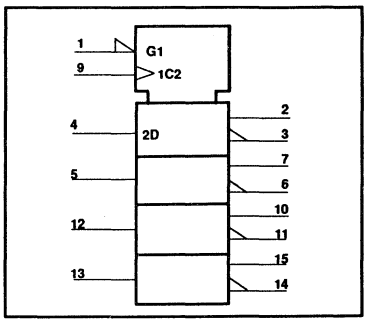
PIN CONFIGURATION



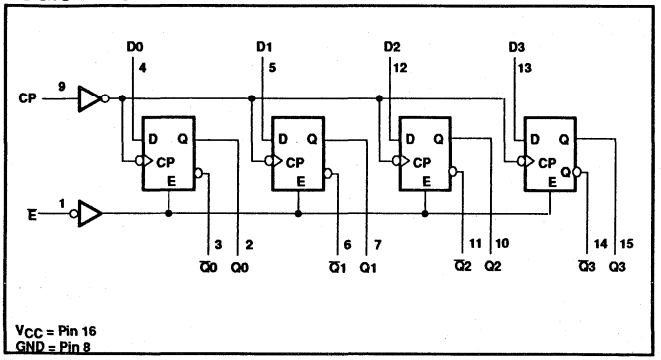
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	
$\overline{E}$	CP	Dn	Qn	$\overline{Q}$n
H	↑	X	NC	NC
L	↑	h	H	L
L	↑	l	L	H

Notes to function table

1. H = High–voltage level
2. h = High state must be present one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low state must be present one setup time before the low–to–high clock transition
5. NC= No change
6. X = Don't care
7. ↑ = Low–to–high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current	74F379	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
		74F379A					–20	µA
I_{OS}	Short–circuit output current3		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	74F379	V_{CC} = MAX			28	40	mA
		74F379A				29	42	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F379

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
f_{max}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Qn}$	Waveform 1	3.5 4.5	5.0 6.5	7.0 8.5	3.5 4.5	8.0 9.5	ns

AC SETUP REQUIREMENTS FOR 74F379

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low level $\overline{E}$ to CP	Waveform 2	6.0 6.0			6.0 6.0		ns
t_h (H) t_h (L)	Hold time, high or low level $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	Waveform 1	4.0 5.0			4.0 5.0		ns

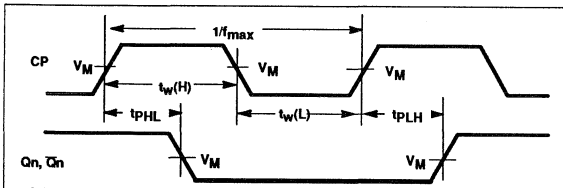
AC ELECTRICAL CHARACTERISTICS FOR 74F379A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	175	200		155		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Q}$n	Waveform 1	2.0 4.0	3.5 5.5	6.5 8.0	2.0 3.5	7.0 8.5	ns

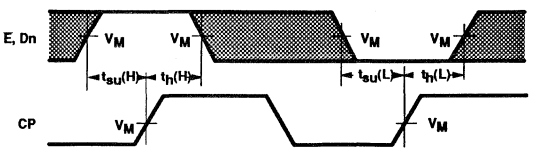
AC SETUP REQUIREMENTS FOR 74F379A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to CP	Waveform 2	3.0 3.0			3.5 3.5		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to CP	Waveform 2	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low level $\overline{E}$ to CP	Waveform 2	4.0 3.5			4.5 4.0		ns
t_h (H) t_h (L)	Hold time, high or low level $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	Waveform 1	3.5 4.5			3.5 4.5		ns

AC WAVEFORMS



Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency

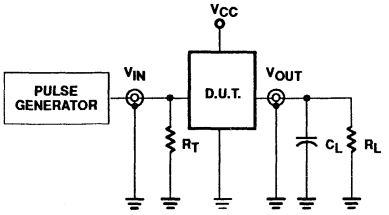


Waveform 3. Data and enable setup time and hold times

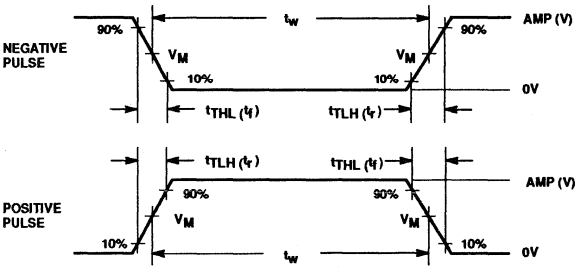
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	v_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

Document No.	853-0418
ECN No.	95907
Date of issue	March 1, 1989
Status	Product Specification
FAST Products	

FAST 74F381
Arithmetic Logic Unit

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F381	6.5 ns	59mA

FEATURES

- **Low-input loading minimizes drive requirements**
- **Performs six arithmetic and logic functions**
- **Selectable Low (clear) and High (preset) functions**
- **Carry Generate and Propagate outputs for use with Carry look-ahead generator**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F381N
20-Pin Plastic SOL	N74F381D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_3	A operand inputs	1.0/4.0	20µA/2.4mA
B_0-B_3	B operand inputs	1.0/4.0	20µA/2.4mA
S_0-S_2	Function select inputs	1.0/1.0	20µA/0.6mA
C_n	Carry input	1.0/4.0	20µA/2.4mA
$\overline{P}$	Carry Propagate output (active-Low)	50/33	1.0mA/20mA
$\overline{G}$	Carry Generate output (active-Low)	50/33	1.0mA/20mA
F_0-F_3	Outputs	50/33	1.0mA/20mA

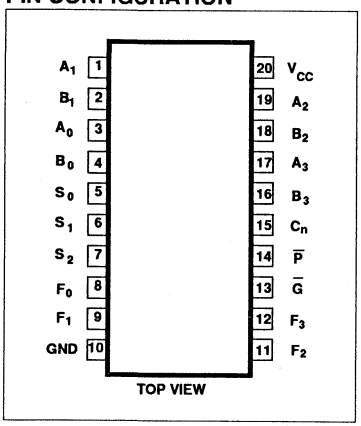
NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

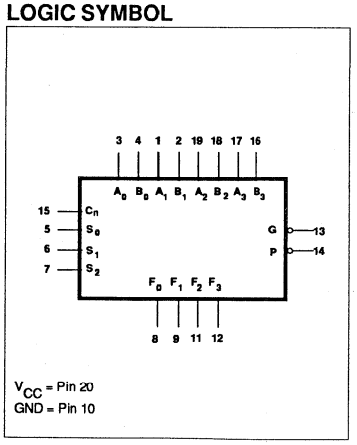
The 74F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Three additional Select (S_0-S_2) input codes force the Function outputs Low or High. Carry Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are provided for use with the 'F182 Carry Look Ahead Generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 'F382 ALU data sheet.

Signals applied to the Select inputs (S_0-S_2) determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output function levels is shown in the Function Table. The circuit performs the arithmetic functions for either active-High or active-Low operands, with output levels in the same convention. In the subtract operating modes, it is necessary to force a Carry (High for active-High operands, Low for active-Low operands) into the C_n input of the least significant package. The Carry Generate ($\overline{G}$) and Carry Propagate ($\overline{P}$) outputs supply input signals to the 'F182 Carry look-ahead generator for expansion to longer word length, as shown in Figure 1. Note that an 'F382 ALU is used for the most significant package. Typical delays for Figure 1 are given in Table 1.

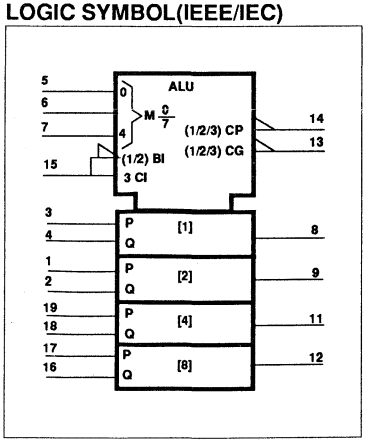
PIN CONFIGURATION



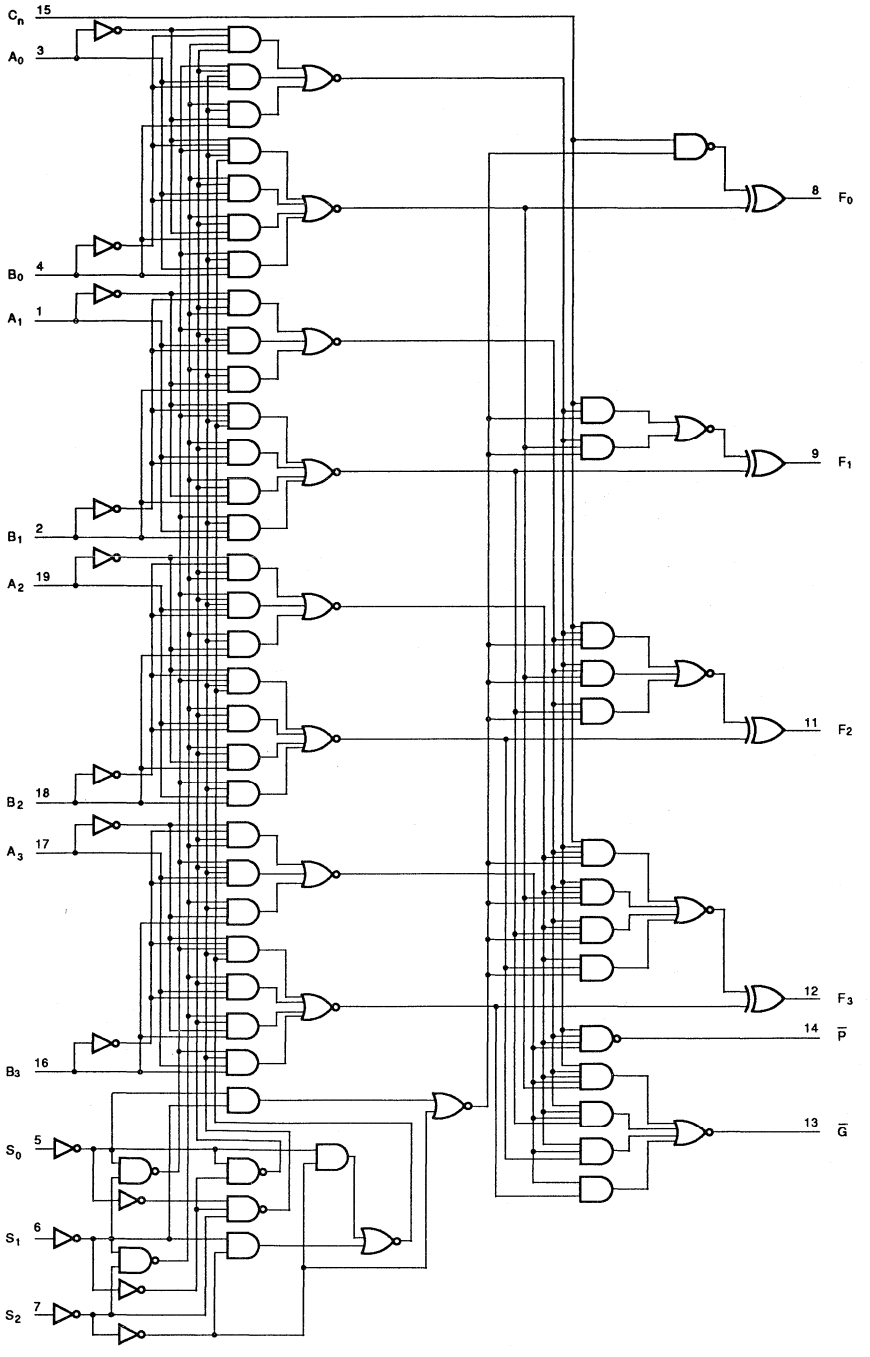
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS						OPERATING MODE
S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$	
L	L	L	X	X	X	L	L	L	L	L	L	Clear
H	L	L	L	L	L	H	H	H	H	H	L	B minus A
H	L	L	L	L	H	L	H	H	H	L	L	
H	L	L	L	H	L	L	L	L	L	H	H	
H	L	L	L	H	H	H	H	H	H	H	L	
H	L	L	H	L	L	L	L	L	L	H	L	
H	L	L	H	L	H	H	H	H	H	L	L	
H	L	L	H	H	L	H	L	L	L	H	H	
H	L	L	H	H	H	L	L	L	L	H	L	
L	H	L	L	L	L	H	H	H	H	H	L	A minus B
L	H	L	L	L	H	L	L	L	L	H	H	
L	H	L	L	H	L	L	H	H	H	L	L	
L	H	L	L	H	H	H	H	H	H	H	L	
L	H	L	H	L	L	L	L	L	L	H	L	
L	H	L	H	L	H	H	L	L	L	H	H	
L	H	L	H	H	L	H	H	H	H	L	L	
L	H	L	H	H	H	L	L	L	L	H	L	
H	H	L	L	L	L	L	L	L	L	H	H	A Plus B
H	H	L	L	L	H	H	H	H	H	H	L	
H	H	L	L	H	L	H	H	H	H	H	L	
H	H	L	L	H	H	L	H	H	H	L	L	
H	H	L	H	L	L	H	L	L	L	H	H	
H	H	L	H	L	H	L	L	L	L	H	L	
H	H	L	H	H	L	L	L	L	L	H	L	
H	H	L	H	H	H	H	H	H	H	L	L	
L	L	H	X	L	L	L	L	L	L	H	H	A ⊕ B
L	L	H	X	L	H	H	H	H	H	H	H	
L	L	H	X	H	L	H	H	H	H	H	L	
L	L	H	X	H	H	L	L	L	L	L	L	
H	L	H	X	L	L	L	L	L	L	H	H	A + B
H	L	H	X	L	H	H	H	H	H	H	H	
H	L	H	X	H	L	H	H	H	H	H	H	
H	L	H	X	H	H	H	H	H	H	H	L	
L	H	H	X	L	L	L	L	L	L	L	L	AB
L	H	H	X	L	H	L	L	L	L	H	H	
L	H	H	X	H	L	L	L	L	L	L	L	
L	H	H	X	H	H	H	H	H	H	H	L	
H	H	H	X	L	L	H	H	H	H	H	H	Preset
H	H	H	X	L	H	H	H	H	H	H	H	
H	H	H	X	H	L	H	H	H	H	H	H	
H	H	H	X	H	H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION SELECT TABLE

SELECT			OPERATING MODE
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A ⊕ B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = High voltage level
L = Low voltage level

Table 1. 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT Cn+4, OVR
A_i or B_i to $\overline{P}$	7.2 ns	7.2ns
$\overline{P}_i$ to C_{n+i} ('F182)	6.2 ns	6.2ns
C_n to F	8.1 ns	-
C_n to C_{n+4}, OVR	-	8.0ns
Total Delay	21.5 ns	21.4 ns

APPLICATION

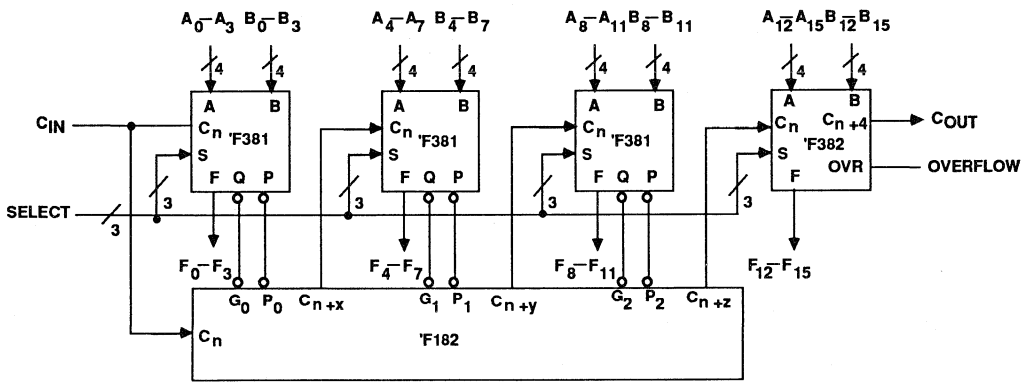


Figure 1. 16-Bit Look-Ahead Carry ALU Expansion

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	A_n, B_n, C_n	V_{CC} = MAX, V_I = 0.5V				-2.4	mA
		S_0, S_1, S_2					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			59	89	mA

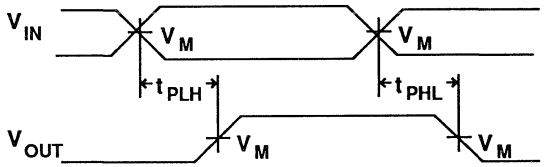
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to F_n	Waveform 1	2.5 2.5	6.0 4.5	11.0 6.5	2.5 2.5	12.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay Any A_n or B_n to any F_n	Waveform 1	3.5 3.0	7.0 6.0	13.0 9.0	3.5 3.0	16.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to F_n	Waveform 1	5.0 4.0	9.0 7.5	20.0 10.5	5.0 4.0	21.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{G}$	Waveform 1	3.5 3.0	6.5 6.0	9.0 8.5	3.5 3.0	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{P}$	Waveform 1	3.0 3.5	5.5 6.0	8.0 8.5	3.0 3.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$ or $\overline{P}$	Waveform 1	5.0 5.5	7.5 8.5	11.0 12.5	5.0 5.0	12.5 14.0	ns

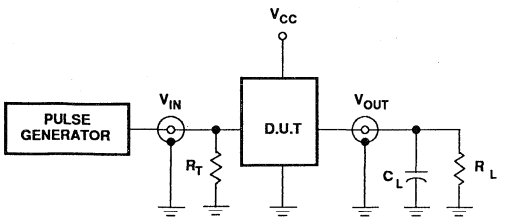
AC WAVEFORMS



Waveform 1. Propagation Delay for Non-Inverting or Inverting paths

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



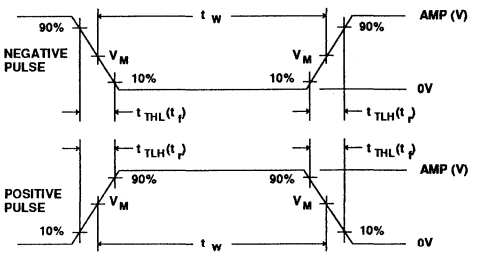
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0419
ECN No.	99966
Date of issue	July 12, 1990
Status	Product Specification
FAST Products	

FAST 74F382
Arithmetic Logic Unit

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F382	7.0 ns	54mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F382N
20-Pin Plastic SOL	N74F382D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_3	A operand inputs	1.0/4.0	20µA/2.4mA
B_0-B_3	B operand inputs	1.0/4.0	20µA/2.4mA
S_0-S_2	Function select inputs	1.0/1.0	20µA/0.6mA
C_n	Carry input	1.0/5.0	20µA/3.0mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
OVR	Overflow output	50/33	1.0mA/20mA
F_0-F_3	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

FEATURES

- **Performs six arithmetic logic functions**
- **Selectable Low (clear) and High (preset) functions**
- **Low-input loading minimizes drive requirements**
- **Carry output for ripple expansion**
- **Overflow output for Two's Complement arithmetic**

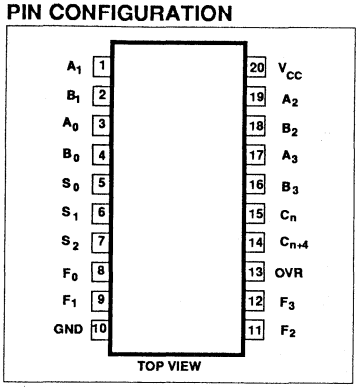
DESCRIPTION

The 74F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select (S_0-S_2) input codes force the Function outputs Low or High. An overflow output is provided for convenience in Two's Complement arithmetic.

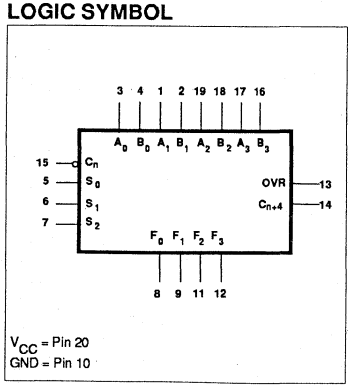
A carry output is provided for ripple expansion. For high-speed expansion using a carry look-ahead generator, refer to the 'F381 data sheet.

Signals applied to the Select inputs, S_0-S_2, determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Function Table. The circuit performs the arithmetic functions for either active-High or active-Low operands, with output levels in the same convention. In the subtract operating modes it is necessary to force a carry (High for active-High operands, Low for active-Low operands) into the C_n input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4}; a High signal on OVR indicates overflow in Two's complement operation (See Table 2 for Two's complement arithmetic). Typical delays for Figure 1 are given in Table 1. When the F382 is cascaded to handle word lengths longer than 4 bits, only the most significant overflow (OVR) output is used.

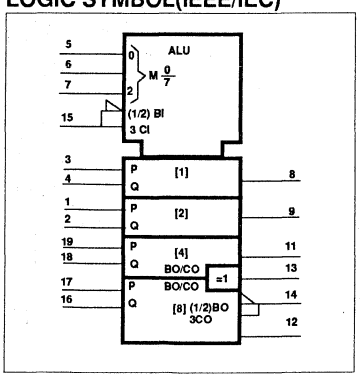
PIN CONFIGURATION



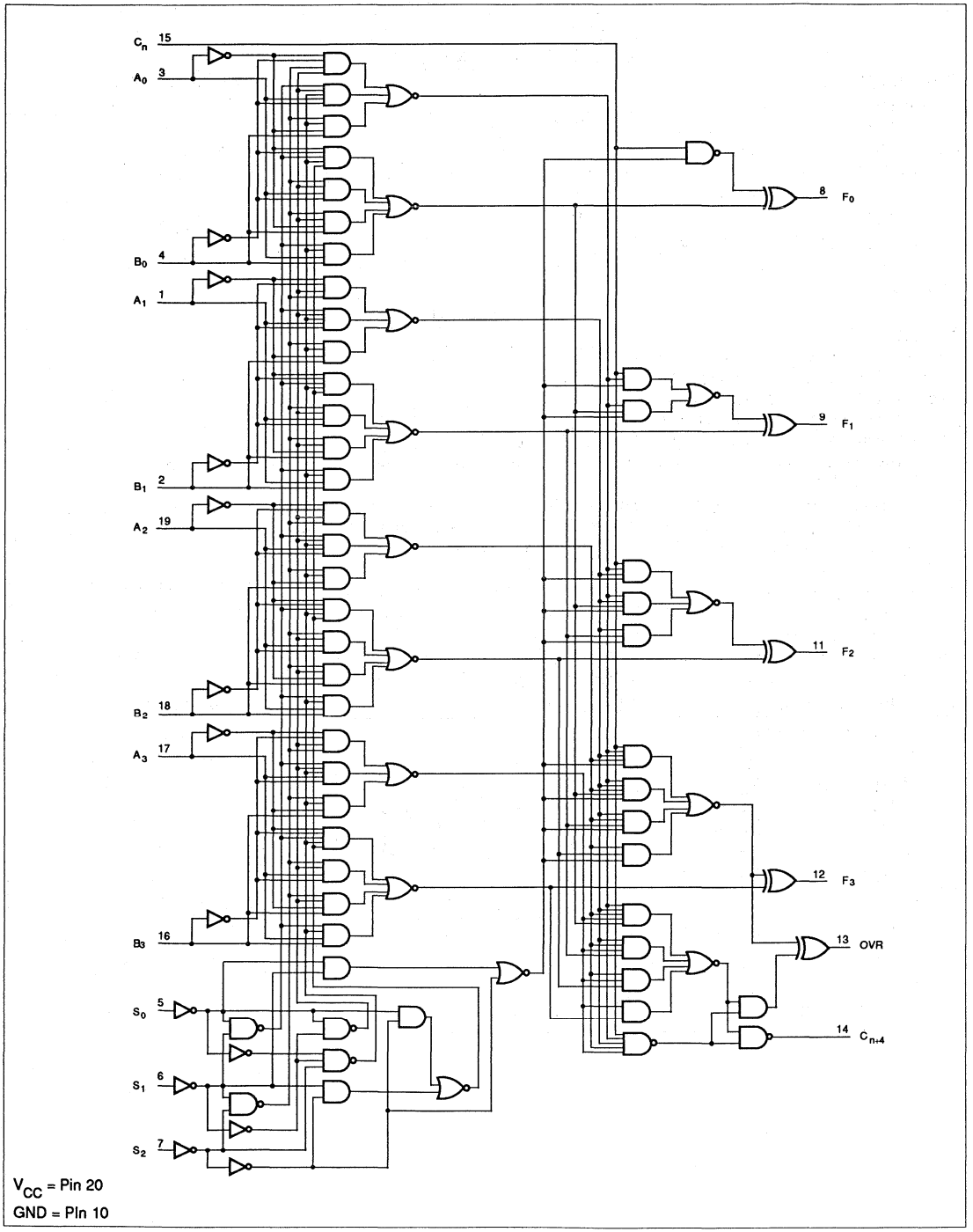
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS						OPERANDS	OPERATING MODE
S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	OVR	C_{n+4}		
L	L	L	L	X	X	L	L	L	L	H	H		Clear
L	L	L	H	X	X	L	L	L	L	H	H		
H	L	L	L	L	L	H	H	H	H	L	L	Active-Low	B minus A
H	L	L	L	L	H	L	H	H	H	L	H		
H	L	L	L	H	L	L	L	L	L	L	L		
H	L	L	L	H	H	H	H	H	H	L	L		
H	L	L	H	L	L	L	L	L	L	L	H	Active-High	
H	L	L	H	L	H	H	H	H	H	L	H		
H	L	L	H	H	L	H	L	L	L	L	L		
H	L	L	H	H	H	L	L	L	L	L	H		
L	H	L	L	L	L	H	H	H	H	L	L	Active-Low	A minus B
L	H	L	L	L	H	L	L	L	L	L	L		
L	H	L	L	H	L	L	H	H	H	L	H		
L	H	L	L	H	H	H	H	H	H	L	L		
L	H	L	H	L	L	L	L	L	L	L	H	Active-High	
L	H	L	H	L	H	H	L	L	L	L	L		
L	H	L	H	H	L	H	H	H	H	L	H		
L	H	L	H	H	H	L	L	L	L	L	H		
H	H	L	L	L	L	L	L	L	L	L	L	A Plus B	
H	H	L	L	L	H	H	H	H	H	L	L		
H	H	L	L	H	L	H	H	H	H	L	L		
H	H	L	L	H	H	L	H	H	H	L	H		
H	H	L	H	L	L	H	L	L	L	L	L		
H	H	L	H	L	H	L	L	L	L	L	H		
H	H	L	H	H	L	L	L	L	L	L	H		
H	H	L	H	H	H	H	H	H	H	L	H		
L	L	H	X	L	L	L	L	L	L	L	L	A ⊕ B	
L	L	H	X	L	H	H	H	H	H	L	L		
L	L	H	L	H	L	H	H	H	H	L	L		
L	L	H	X	H	H	L	L	L	L	H	H		
L	L	H	H	H	L	H	H	H	H	H	H		
H	L	H	X	L	L	L	L	L	L	L	L	A + B	
H	L	H	X	L	H	H	H	H	H	L	L		
H	L	H	X	H	L	H	H	H	H	L	L		
H	L	H	L	H	H	H	H	H	H	L	L		
H	L	H	H	H	H	H	H	H	H	H	H		
L	H	H	X	L	L	L	L	L	L	H	H	AB	
L	H	H	X	L	H	L	L	L	L	L	L		
L	H	H	X	H	L	L	L	L	L	H	H		
L	H	H	L	H	H	H	H	H	H	L	L		
L	H	H	H	H	H	H	H	H	H	H	H		
H	H	H	X	L	L	H	H	H	H	L	L	Preset	
H	H	H	X	L	H	H	H	H	H	L	L		
H	H	H	X	H	L	H	H	H	H	L	L		
H	H	H	L	H	H	H	H	H	H	L	L		
H	H	H	H	H	H	H	H	H	H	H	H		

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION SELECT TABLE

SELECT			OPERATING MODE
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = High voltage level
L = Low voltage level

Table 1. 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT Cn+4, OVR
A_i or B_i to C_{n+4}	6.5 ns	6.5ns
C_n to C_{n+4}	6.3 ns	6.3ns
C_n to C_{n+4}	6.3 ns	6.3ns
C_n to F	8.1 ns	-
C_n to C_{n+4}, OVR	-	8.0ns
Total Delay	27.2 ns	27.1ns

Table 2. Two's Complement Arithmetic

MSB			LSB	Numerical Value
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	-8
H	L	L	H	-7
H	L	H	L	-6
H	L	H	H	-5
H	H	L	L	-4
H	H	L	H	-3
H	H	H	L	-2
H	H	H	H	-1

H = High voltage level
L = Low voltage level

APPLICATION

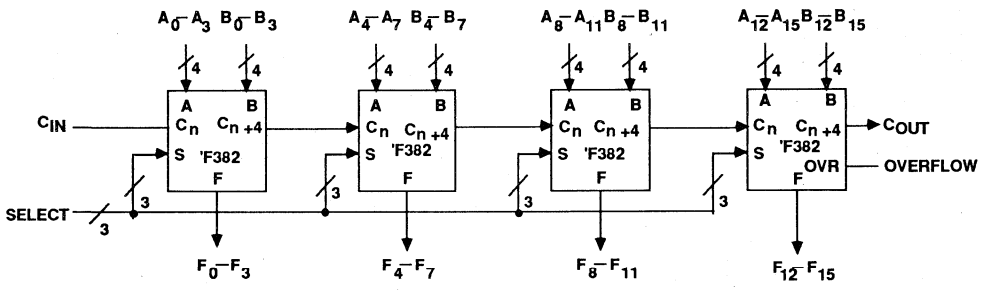


Figure 1. 16-Bit Ripple Carry ALU Expansion

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_n	V_{CC} = MAX, V_I = 0.5V				-3.0	mA
		A_0-A_3, B_0-B_3					-2.4	mA
		S_0, S_1, S_2					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			54	81	mA

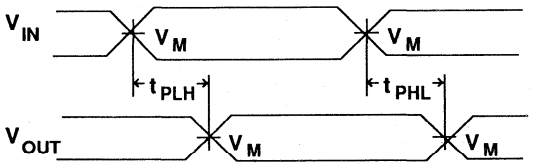
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to F_n	Waveform 1	3.0 2.5	7.0 4.5	12.0 6.5	2.5 2.5	13.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to F_n	Waveform 1	3.5 3.0	8.0 6.0	13.5 10.0	3.5 2.5	17.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to F_i	Waveform 1	5.5 5.5	9.0 7.5	15.0 10.5	5.5 5.5	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{n+4}	Waveform 1	3.5 3.5	7.0 6.5	10.5 9.5	3.5 3.5	11.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to OVR or C_{n+4}	Waveform 1	7.0 5.0	10.5 8.0	14.5 11.0	6.5 5.0	17.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Waveform 1	3.0 3.5	4.5 5.0	6.0 6.5	2.5 3.5	6.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to OVR	Waveform 1	4.5 3.0	9.0 5.0	13.5 6.5	4.0 3.0	15.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to OVR	Waveform 1	6.0 3.5	9.0 6.5	12.5 9.0	5.5 3.5	16.5 10.0	ns

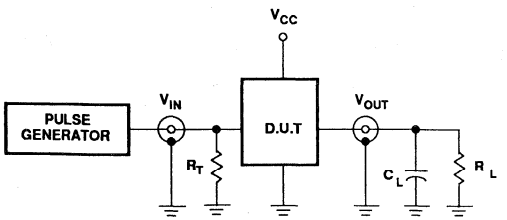
AC WAVEFORMS



Waveform 1. Propagation Delay for Non-Inverting or Inverting paths

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



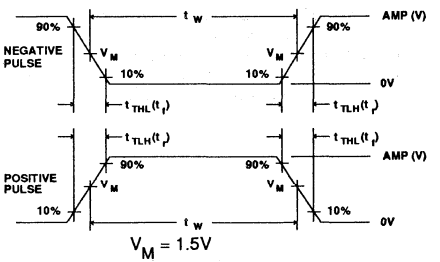
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0868
ECN No.	97678
Date of issue	September 20, 1989
Status	Product Specification
FAST Products	

FAST 74F385
Adder/Subtractor

Quad Serial Adder/Subtractor

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F385	140 MHz	55mA

FEATURES

- **Four independent adder/subtractors**
- **Two's complement arithmetic**
- **Synchronous operation**
- **Common Clear and Clock**
- **'F385 is designed for use with serial multipliers in implementing digital filters and butterfly networks in fast Fourier transforms**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F385N
20-Pin Plastic SOL	N74F385D

DESCRIPTION

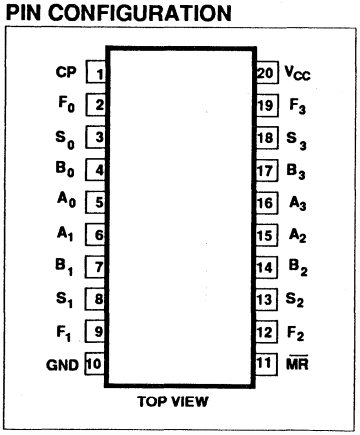
The 74F385 contain four independent adder/subtractor elements with common Clock and Master Reset. Each adder/subtractor contains a sum flip-flop and a carry flip-flop for synchronous operations. Flip-flop state changes occur on the rising edge of the Clock Pulse (CP) input signal. The Select (S) input should be Low for the Add (A plus B) mode and High for the Subtract (A minus B) mode. A Low signal on the asynchronous Master Reset ($\overline{MR}$) input clears the sum flip-flop and resets the Carry flip-flop to zero in the Add mode or presets it to one in the Subtract mode.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

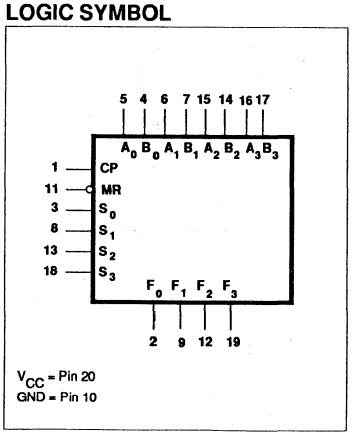
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	A operand inputs	1.0/1.0	20μA/0.6mA
B_0 - B_3	B operand inputs	1.0/1.0	20μA/0.6mA
S_0 - S_3	Function select inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active Low)	1.0/1.0	20μA/0.6mA
F_0 - F_3	Sum or difference outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

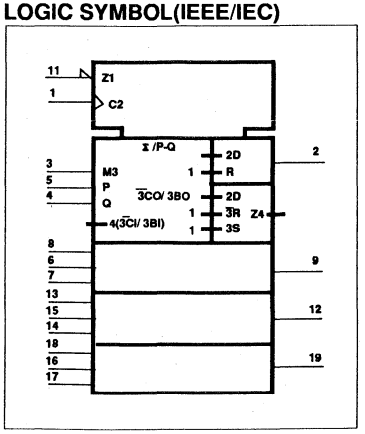
PIN CONFIGURATION



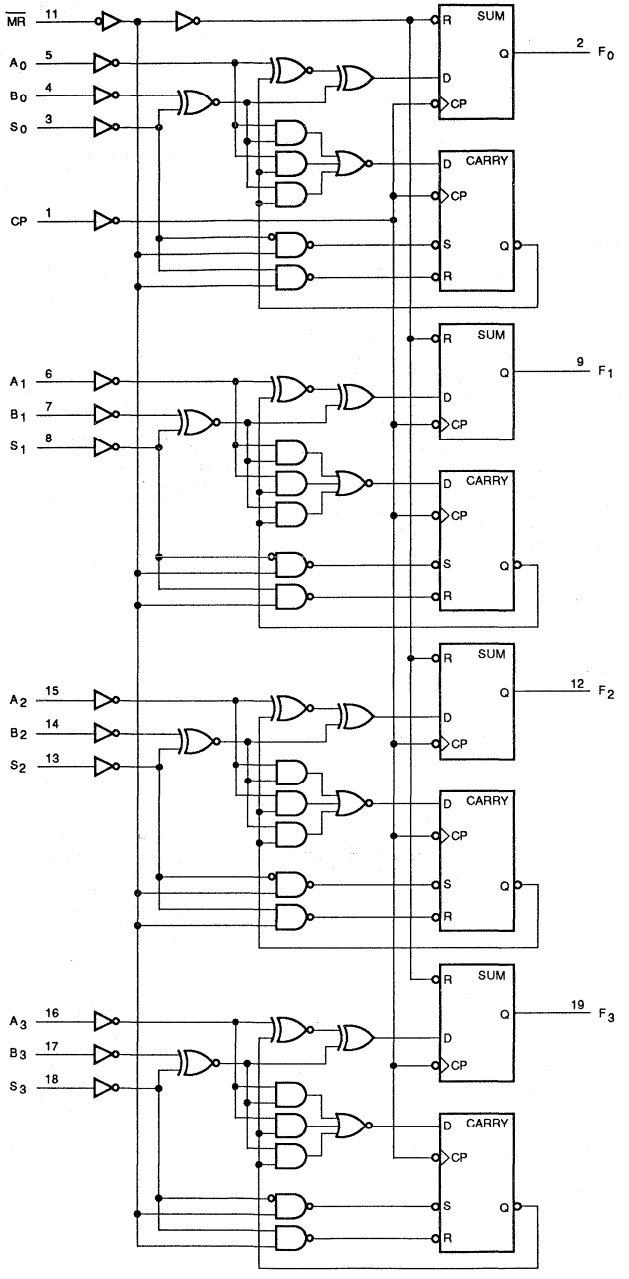
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC}=pin 20
GND=pin 10

FUNCTION TABLE

INPUTS				CARRY FLIP-FLOP STATE		OUTPUT	OPERATING MODE
$\overline{MR}$	S	A	B	Before↑	After↑	F	
L	L	X	X	L	L	L	Clear
L	H	X	X	H	H	L	
H	L	L	L	L	L	L	Add
H	L	L	L	H	L	H	
H	L	L	H	L	L	H	
H	L	L	H	H	H	L	
H	L	H	L	L	L	H	
H	L	H	L	H	H	L	
H	L	H	H	L	H	L	
H	L	H	H	H	H	H	
H	H	L	L	L	L	H	Subtract
H	H	L	L	H	H	L	
H	H	L	H	L	L	L	
H	H	L	H	H	L	H	
H	H	H	L	L	H	L	
H	H	H	L	H	H	H	
H	H	H	H	L	L	H	
H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High Clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OS}	Short-circuitoutput current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

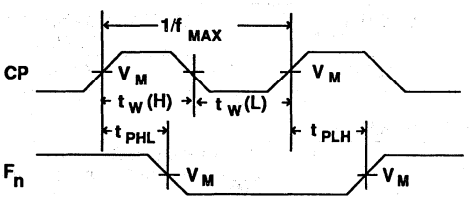
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	140		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to F_n	Waveform 1	3.0 3.5	5.0 5.5	8.0 9.0	2.5 3.5	9.0 10.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to F_n	Waveform 2	4.0	6.5	9.5	4.0	10.5	ns

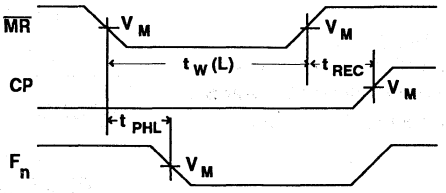
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n, B_n or S_n to CP	Waveform 3	12.0 12.0			12.0 12.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n, B_n or S_n to CP	Waveform 3	0 0			0 0		ns
t_s(H) t_s(L)	CP Pulse width High or Low	Waveform 2	6.0 6.0			6.0 6.0		ns
t_w(L)	$\overline{MR}$ Pulse width Low	Waveform 2	6.0			6.0		ns
t_{REC}	Recovery time $\overline{MR}$ to $\overline{CP}$	Waveform 2	8.5			9.5		ns

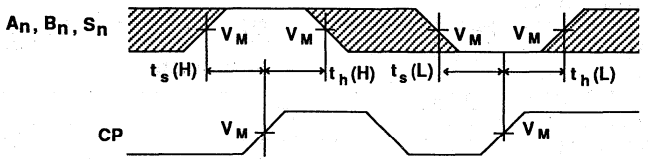
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



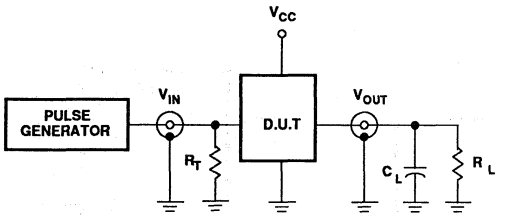
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



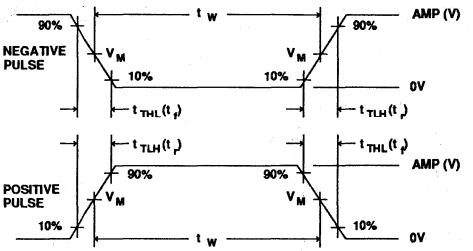
Waveform 3. Data And Select Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

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ECN No.	94977
Date of issue	November 1, 1988
Status	Product Specification
FAST Products	

FAST 74F393
Dual 4-Bit Binary Ripple Counter

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F393	125MHz	40mA

FEATURES
- **Two 4-Bit binary counters**
- **Two Master Resets to clear each 4-bit counter individually**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F393N
14-Pin Plastic SO	N74F393D

DESCRIPTION

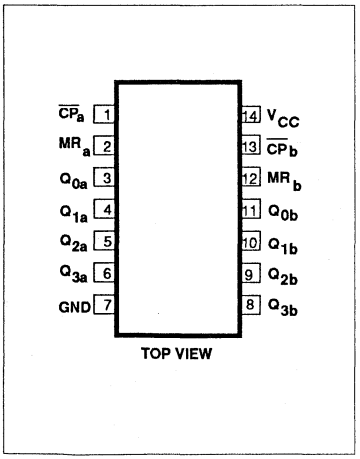
The 74F393 is a Dual Ripple Counter with separate Clock ($\overline{CP}_n$) and Master Reset Reset (MR) inputs to each counter. The two counters are identified by the "a" and "b" suffixes in the pin configuration. The operation of each half of the 'F393 is the same. The counters are triggered by a High-to-Low transition of the Clock ($\overline{CP}_a$ and $\overline{CP}_b$) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high speed address decoding. The Master Resets (MR_a and MR_b) are active High asynchronous inputs; one for each 4-bit counter. A High level in the MR input overrides the Clock and sets the outputs Low.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

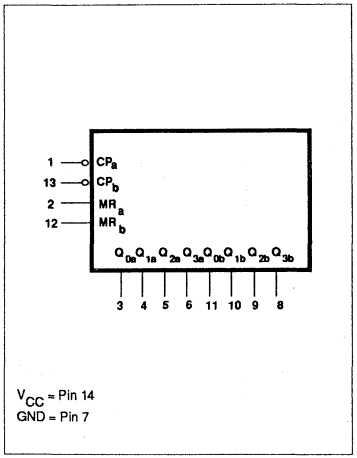
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CP}_a$, $\overline{CP}_b$	Clock inputs	1.0/1.0	20µA/0.6mA
MR_a, MR_b	Master Reset inputs	1.0/1.0	20µA/0.6mA
Q_{na} - Q_{nb}	Data outputs	50/33.3	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

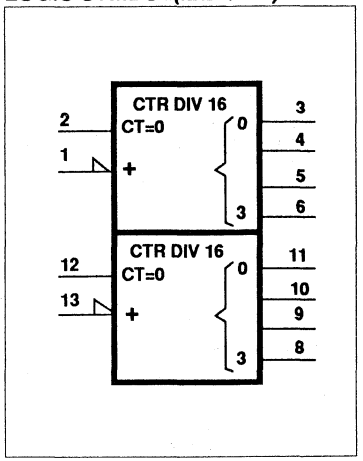
PIN CONFIGURATION



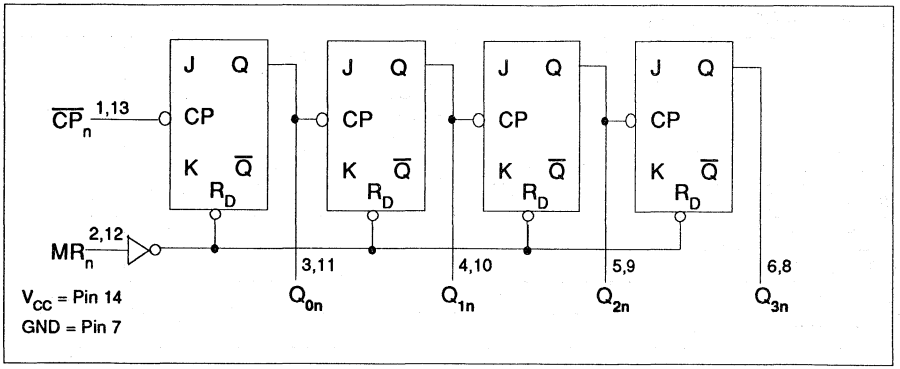
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

COUNT	OUTPUTS			
	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuitoutput current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			25	36	mA
		I_{CCL}				42	58	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable typ5
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

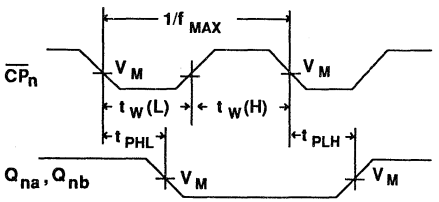
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_{0a}, Q_{0b}	Waveform 1	3.5 5.0	5.5 7.0	8.0 10.0	3.5 5.0	9.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_{1a}, Q_{1b}	Waveform 1	5.0 7.5	7.0 9.5	10.0 12.0	4.5 7.0	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_{2a}, Q_{2b}	Waveform 1	8.0 9.5	10.0 11.5	13.0 14.5	7.0 9.0	15.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_{3a}, Q_{3b}	Waveform 1	10.5 12.0	12.5 14.0	15.5 16.5	10.0 11.5	17.0 17.5	ns
t_{PHL}	Propagation delay MR to Q_{na}, Q_{nb}	Waveform 2	4.0	6.0	9.0	4.0	9.0	ns

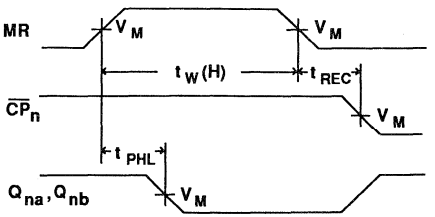
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_w(H) t_w(L)	$\overline{CP}_n$ Pulse width, High or Low	Waveform 1	4.5 3.5			5.0 4.0		ns
t_w(H)	MR Pulse width High	Waveform 2	3.5			4.5		ns
t_{REC}	Recovery time MR to $\overline{CP}_n$	Waveform 2	2.5			3.0		ns

AC WAVEFORMS



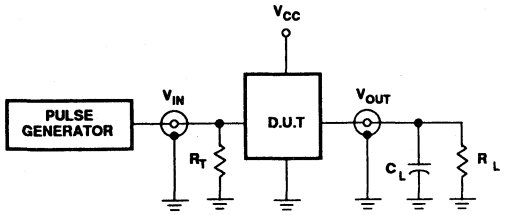
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



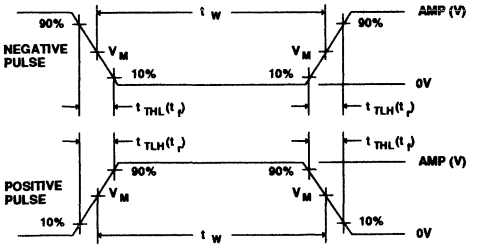
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0370
ECN No.	00780
Date of issue	October 23, 1990
Status	Product Specification
FAST Products	

FAST 74F395
Shift Register

4-Bit Cascadable Shift Register (3-state)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F395	120MHz	32mA

FEATURES

- **4-bit parallel load shift register**
- **Independent 3-state buffer outputs, Q_0-Q_3**
- **Separate Q_s output for serial expansion**
- **Asynchronous Master Reset**

DESCRIPTION

The 74F395 is a 4-bit Shift Register with serial and parallel synchronous operating modes and 3-state buffer outputs.The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is High, data is loaded from the Parallel Data inputs (D_0 - D_3) into the register synchronous with the High-to-Low transition of the Clock input (CP). When PE is Low, the data at the Serial Data input (D_s) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable one setup prior to the High-to-Low transition of the clock.

The Master Reset ($\overline{MR}$) is an asynchronous active-Low input. When Low, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, or large capacitive loads.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F395N
16-Pin Plastic SO	N74F395D

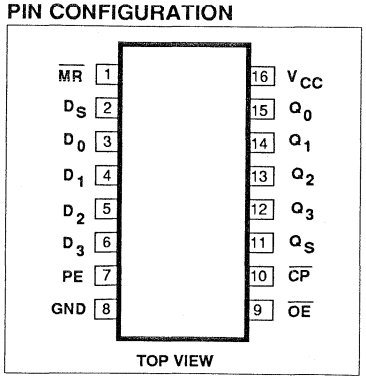
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
D_s	Serial data input	1.0/1.0	20µA/0.6mA
PE	Parallel Enable input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
Q_s	Serial expansion output	50/33	1.0mA/20mA
Q_0 - Q_3	Data outputs (3-state)	150/40	3.0mA/24mA

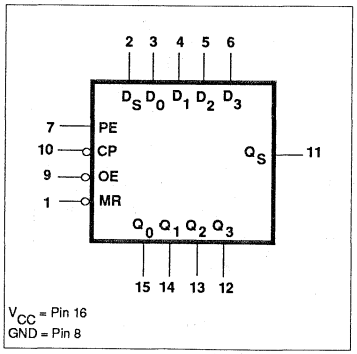
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

The active-Low Output Enable ($\overline{OE}$) controls all four 3-state buffers independent of the register operation. The data in the register appears at the outputs when $\overline{OE}$ is Low. The outputs are in High impedance "OFF" state, which means they will neither drive nor load the bus when $\overline{OE}$ is High. The output from the last stage is brought out separately. This output (Q_S) is tied to the Serial Data input (D_s) of the next register for serial expansion applications.The Q_s output is not affected by the 3-state buffer operation.

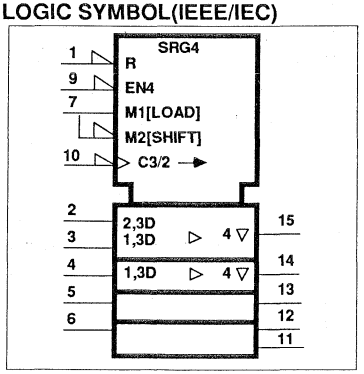
PIN CONFIGURATION



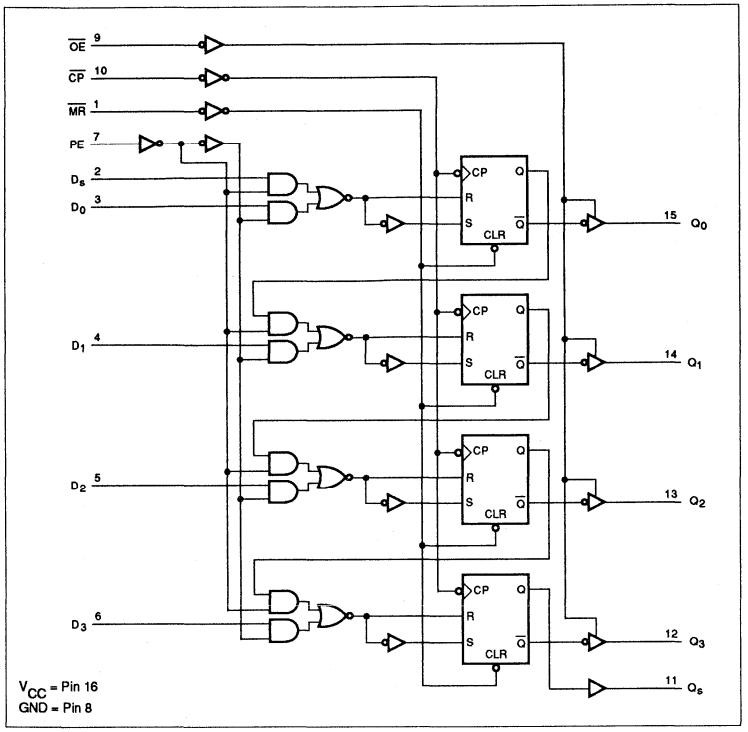
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT-FUNCTION TABLE

INPUTS					OUTPUTS				REGISTER OPERATING MODES
$\overline{MR}$	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3	
L	X	X	X	X	L	L	L	L	Reset (clear)
H	↓	l	l	X	L	q_0	q_1	q_2	Shift right
H	↓	l	h	X	H	q_0	q_1	q_2	
H	↓	h	X	l	L	L	L	L	Parallel load
H	↓	h	X	h	H	H	H	H	

INPUTS		OUTPUTS		3-STATE BUFFER OPERATING MODES
$\overline{OE}$	Q_n (Register)	Q_0, Q_1, Q_2, Q_3	Q_S	
L	L	L	L	Read
L	H	H	H	
H	L	Z	L	Disable buffers
H	H	Z	H	

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the High-to-Low clock transition
X = Don't care
Z = High impedance "OFF" state
↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_S	40	mA
		Q_0-Q_3	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_S			-1	mA
		Q_0-Q_3			-3	mA
I_{OL}	Low-level output current	Q_S			20	mA
		Q_0-Q_3			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		Q_0-Q_3		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OZH}	Off-state output current High level voltage applied	Q_0-Q_3 only	V_{CC} = MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current Low level voltage applied	Q_0-Q_3 only	V_{CC} = MAX, V_O= 0.5V					-50	µA
I_{OS}	Short-circuitoutput current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{MR}$=PE=D_n=D_s=4.5V, $\overline{OE}$=GND, CP=↓			33	48	mA
		I_{CCL}		$\overline{MR}$=$\overline{OE}$=D_n=D_s=GND, PE=4.5V, CP=↓			35	50	mA
		I_{CCZ}		$\overline{MR}$=D_n=D_s=GND, $\overline{OE}$=4.5V			32	46	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

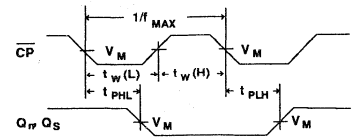
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	120		95		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n	Waveform 1	3.5 5.0	6.0 8.0	8.5 11.0	3.5 5.0	9.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_S	Waveform 1	4.5 5.5	6.0 7.5	8.5 10.0	4.0 5.0	9.5 10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.0	7.5	10.0	5.0	10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_S	Waveform 2	4.5	7.0	9.0	4.5	9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	4.0 3.5	6.5 6.0	9.0 8.0	4.0 3.5	10.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	2.5 3.5	4.5 5.5	1.0 1.0	5.5 6.5	ns

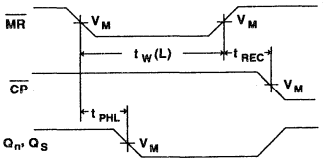
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{CP}$	Waveform 3	2.5 1.5			3.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{CP}$	Waveform 3	1.5 1.5			1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low PE to $\overline{CP}$	Waveform 3	6.5 6.0			7.0 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low PE to $\overline{CP}$	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width High or Low	Waveform 1	5.0 4.0			5.5 4.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	2.5			3.0		ns
t_{REC}	Recovery time $\overline{MR}$ to $\overline{CP}$	Waveform 2	6.0			7.0		ns

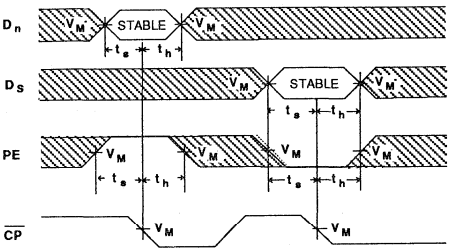
AC WAVEFORMS



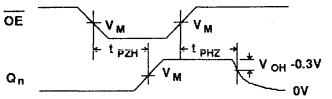
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



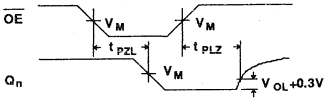
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Parallel Enable and Data Setup Time and Hold Time



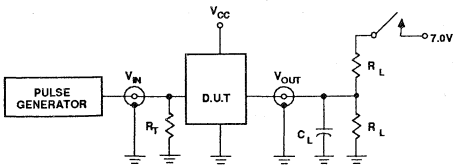
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Totem-Pole Output (Q_S)

SWITCH POSITION

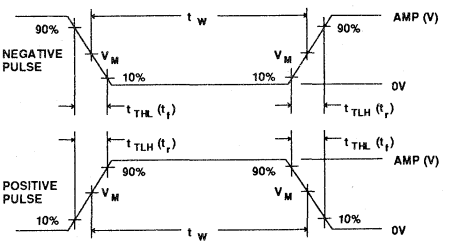
TEST	SWITCH
t_{PZL}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0028
ECN No.	96254
Date of issue	April 8, 1990
Status	Product Specification
FAST Products	

FAST 74F398, 74F399 Registers

74F398 Quad 2-Port Register With True And Complementary Outputs
74F399 Quad 2-Port Register

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F398	120MHz	25mA
74F399	120MHz	22mA

FEATURES

- **Select inputs from two data sources**
- **Fully positive edge triggered**
- **Both True and Complementary outputs-'F398**

DESCRIPTION

The 74F398 and 74F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock.

The 'F399 is the 16-pin version of the 'F398, with only the true (Q_n) outputs of the flip-flops available.

The 'F398 and 'F399 are high speed quad 2-port registers. They select 4 bits of data from either of two sources (Ports) under control of a common select input (S). The selected data is transferred to a 4-bit output register synchronous with the Low-to-High transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0n}, I_{1n}) and Select input (S) must be stable only a setup time prior to and hold time after the Low-to-High transition of the Clock input for predictable operation. The 'F398 has both Q and $\overline{Q}$ outputs.

ORDERING INFORMATION

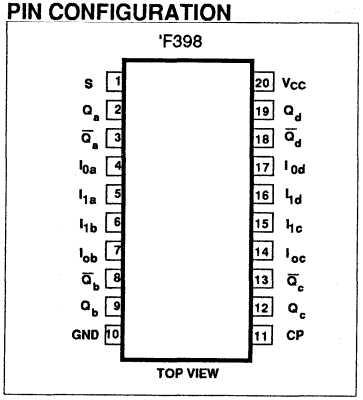
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-pin Plastic DIP	N74F398N
20-pin Plastic SOL	N74F398D
16-pin Plastic DIP	N74F399N
16-pin Plastic SO	N74F399D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

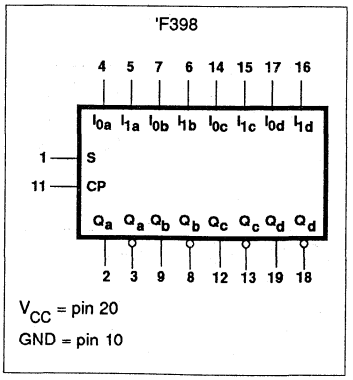
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}, I_{0b}, I_{0c}, I_{0d}	Data inputs from source 0	1.0/1.0	20µA/0.6mA
I_{1a}, I_{1b}, I_{1c}, I_{1d}	Data inputs from source 1	1.0/1.0	20µA/0.6mA
S	Common Select input	1.0/1.0	20µA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_a, Q_b, Q_c, Q_d	Register true outputs	50/33	1.0mA/20mA
$\overline{Q}_a$, $\overline{Q}_b$, Q_c, $\overline{Q}_d$	Register complementary outputs ('F398)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

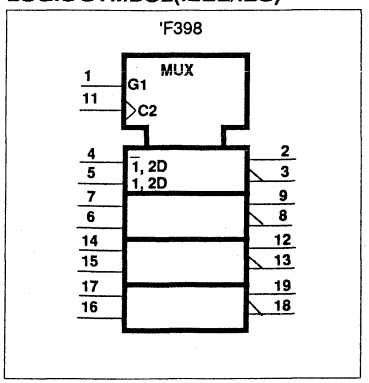
PIN CONFIGURATION



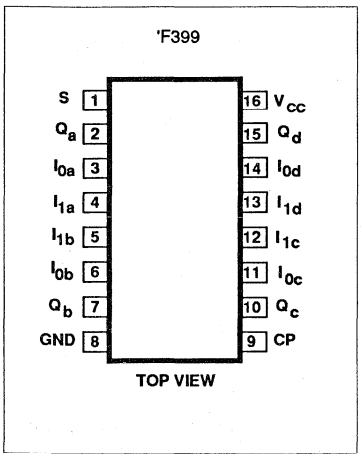
LOGIC SYMBOL



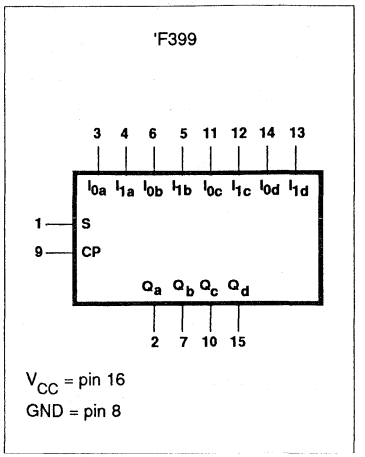
LOGIC SYMBOL(IEEE/IEC)



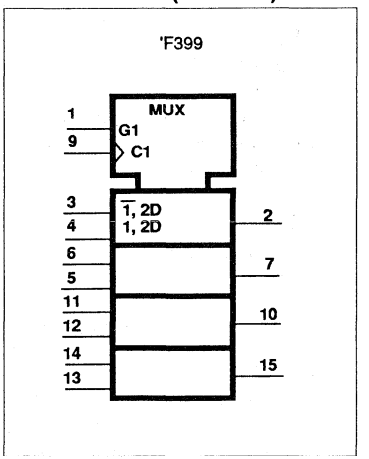
PIN CONFIGURATION



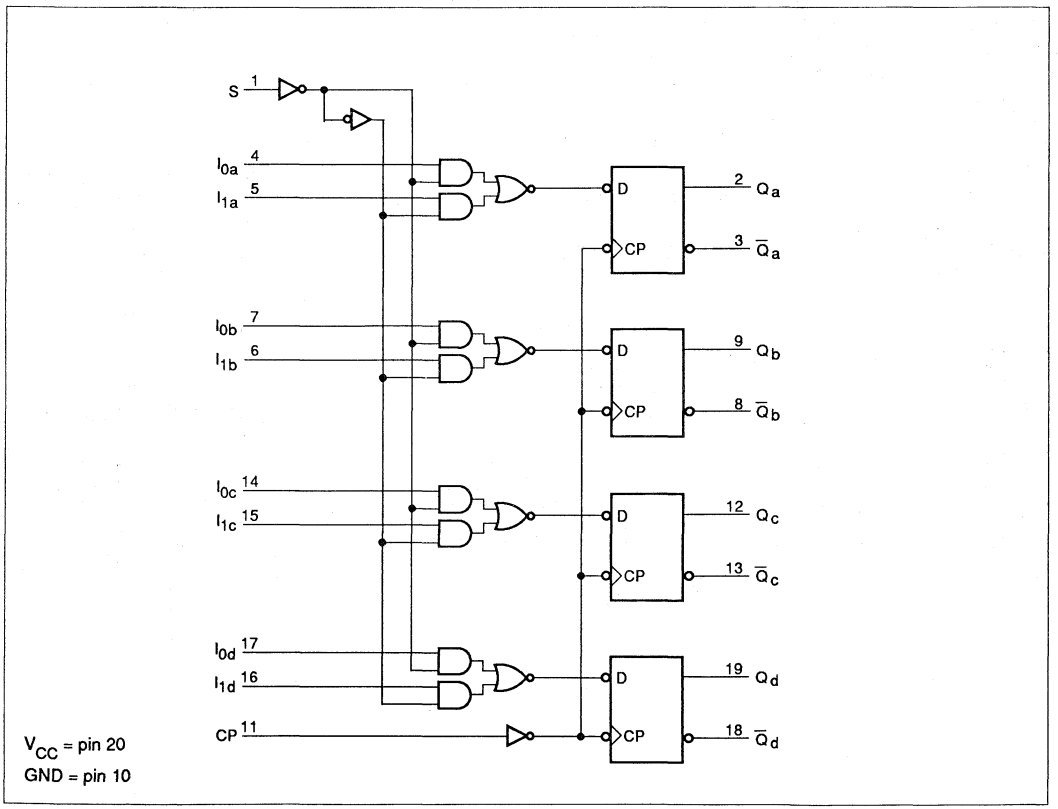
LOGIC SYMBOL



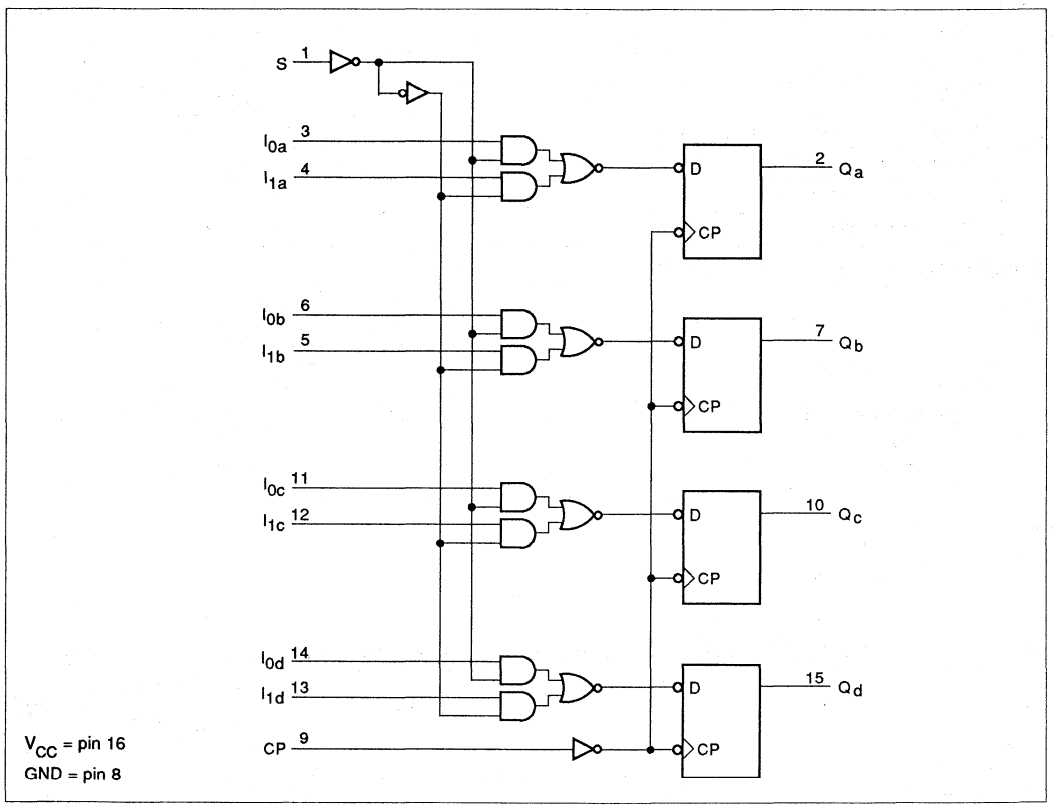
LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM for 'F398



LOGIC DIAGRAM for 'F399



FUNCTION TABLE

INPUTS				OUTPUTS	
CP	S	I_{0n}	I_{1n}	Q_n	$\overline{Q}_n$*
↑	l	l	X	L	H
↑	l	h	X	H	L
↑	h	X	l	L	H
↑	h	X	h	H	L

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
* = For 'F398 only

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	'F398	V_{CC} = MAX			25	38	mA
		'F399				22	34	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

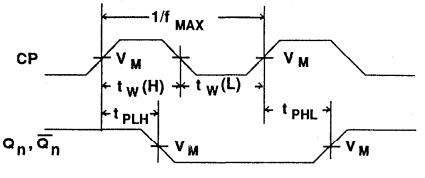
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.0 3.0	5.7 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns

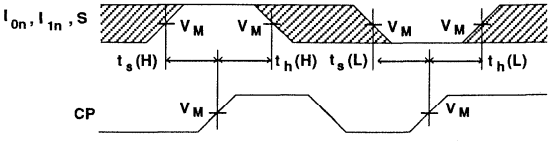
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I_{0n}, I_{1n} to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I_{0n}, I_{1n} to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to CP	Waveform 2	7.5 7.5			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS



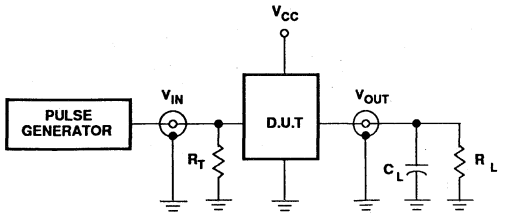
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



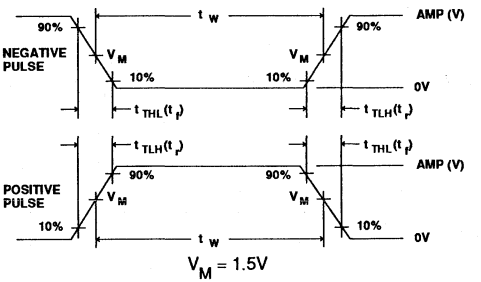
Waveform 2. Data And Select Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Register stack – 16×4 RAM 3-State output register 74F410

FEATURES

- Edge triggered output register
- ypical access time of 19.5ns
- Optimize for register stack operation
- 3–state outputs
- 18–pin package

DESCRIPTION

The 74F410 is a register oriented high speed 64–bit read/write memory organized as 16–words by 4–bits. An edge–triggered 4–bit output register allows new input data to be written while previous data is held. 3–state outputs are provided for maximum versatility.

The 74F410 is fully compatible with all TTL families.

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F410	19.5ns	45mA

FUNCTIONAL DESCRIPTION

Write operation – When the three control inputs, write enable ($\overline{WE}$), chip select ($\overline{CS}$), and clock (CP), are low the information on the data inputs (D0–D3) is written into the memory location selected by the address inputs (A0–A3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are low, the contents of the selected memory location follow these changes provided setup and hold time criteria are met.

Read operation – When $\overline{CS}$ is low, $\overline{WE}$ is high, and CP goes from low–to–high, the contents of the memory location selected by the address inputs (A0–A3) are edge–triggered into the output register.

When $\overline{WE}$ is low, $\overline{CS}$ is low, CP goes from low–to–high, the data at the data inputs is edge–triggered into the output register. The $\overline{OE}$ input controls the output buffers. When $\overline{OE}$ is high the four outputs (Q0–Q3) are in a high impedance or off state; when $\overline{OE}$ is low, the outputs are determined by the state of the output register.

ORDERING INFORMATION

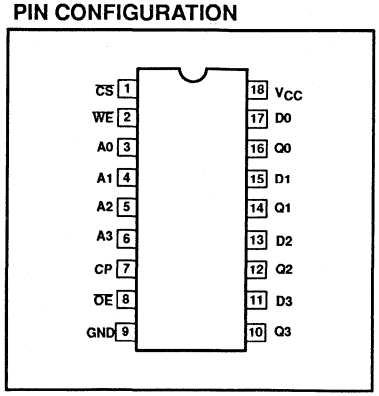
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
18–pin plastic DIP (300mil)	N74F410N

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

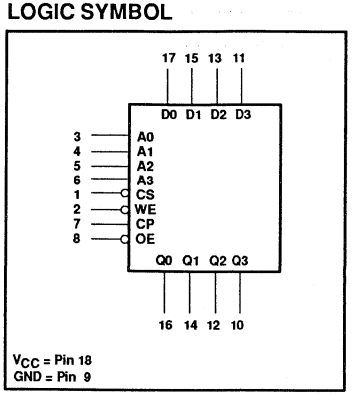
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
A0 – A3	Address inputs	1.0/1.0	20µA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/2.0	20µA/1.2mA
$\overline{CS}$	Chip select input (active low)	1.0/2.0	20µA/1.2mA
$\overline{OE}$	Output enable input (active low)	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write enable input (active low)	1.0/1.0	20µA/0.6mA
Q0 – Q3	Data outputs	150/40	3mA/24mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

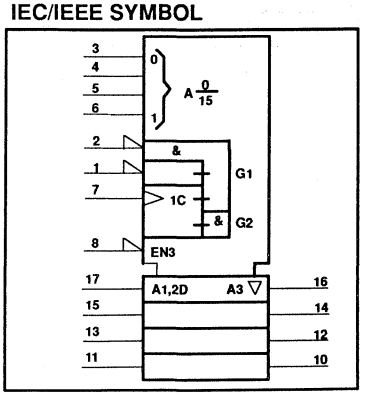
PIN CONFIGURATION



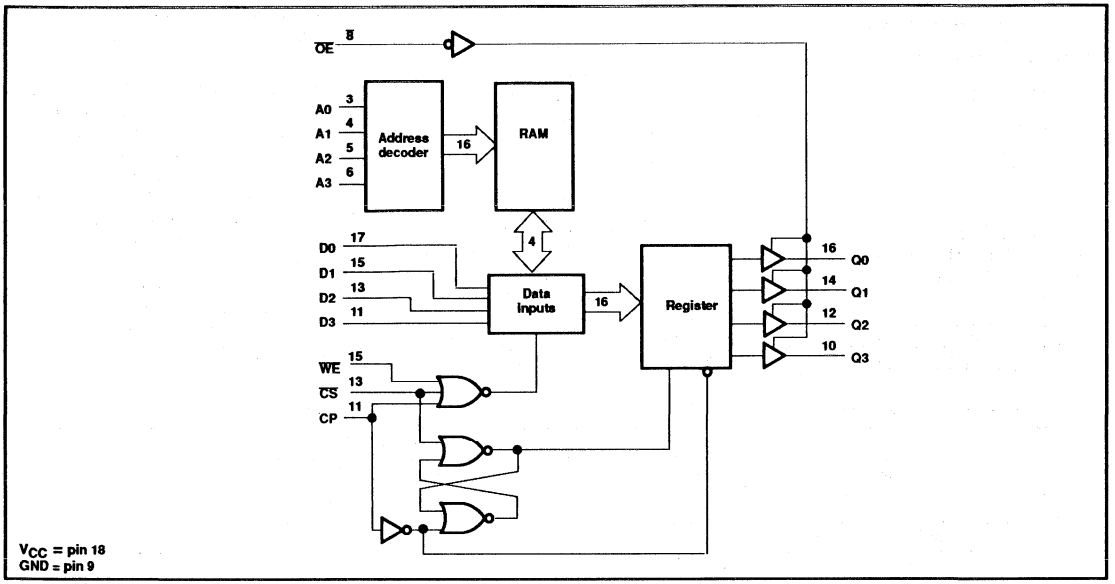
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	48	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–3	mA
I_{OL}	Low–level output current			24	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current	others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		CP, $\overline{CS}$					-1.2	mA
I_{OZH}	Offset–output current, high–level voltage applied		V_{CC} = MAX, V_I = 2.7V				50	µA
I_{OZL}	Offset–output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			45	70	mA

NOTES:

3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
4. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation dealy CP to Qn	Waveform 1	4.0 4.5	6.5 6.5	8.5 9.0	3.5 4.0	9.5 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to Qn	Waveform 3, 4	3.0 4.5	4.5 6.0	7.5 9.0	2.5 3.5	8.5 9.5	ns
t_{PHZ} t_{PHL}	Output disable time $\overline{OE}$ to Qn	Waveform 3, 4	2.0 2.0	3.5 3.5	6.0 6.5	1.5 2.0	6.5 7.0	ns

AC SETUP REQUIREMENTS FOR READ MODE

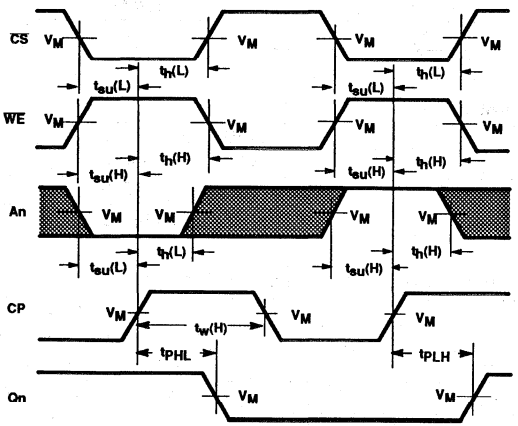
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(L)$	Setup time, low, $\overline{CS}$ to CP[1]	Waveform 1	4.0			4.5		ns
$t_h(L)$	Hold time, low, $\overline{CS}$ to CP[1]	Waveform 1	3.5			4.5		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to CP[1]	Waveform 1	13.0 13.0			15.0 15.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to CP[1]	Waveform 1	0 0			0 0		ns
$t_{su}(H)$	Setup time, high, $\overline{WE}$ to CP[1]	Waveform 1	13.0			15.0		ns
$t_h(H)$	Hold time, high, $\overline{WE}$ to CP[1]	Waveform 1	0			0		ns
$t_w(L)$	CP pulse width, low	Waveform 1	5.0			6.0		ns

NOTE:
1. Low–to–high clock transition.

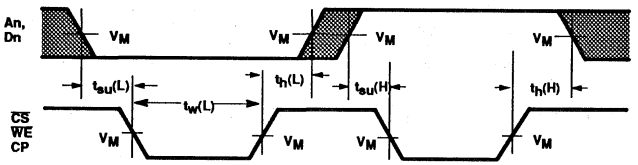
AC SETUP REQUIREMENTS FOR WRITE MODE

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Dn to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	6.0 6.0			8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Dn to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_w(L)$	$\overline{WE}$ pulse width, low	Waveform 2	7.0			8.0		ns
$t_w(L)$	$\overline{CS}$ pulse width, low	Waveform 2	6.0			7.0		ns
$t_w(L)$	CP pulse width, low	Waveform 2	7.0			8.0		ns

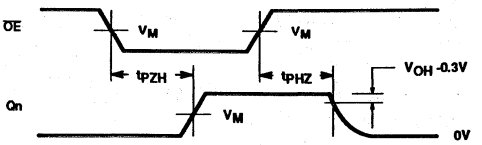
AC WAVEFORMS



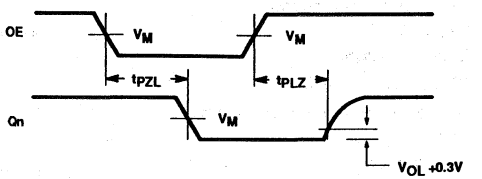
Waveform 1. Read cycle timing



Waveform 2. Write cycle timing



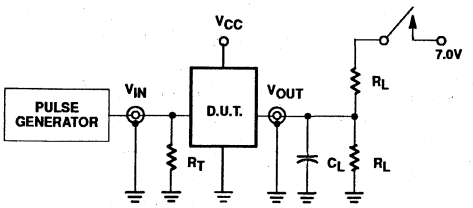
Waveform 3. 3-State output enable time to high level and output disable time from high level



Waveform 4. 3-State output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test circuit for 3–state outputs

SWITCH POSITION

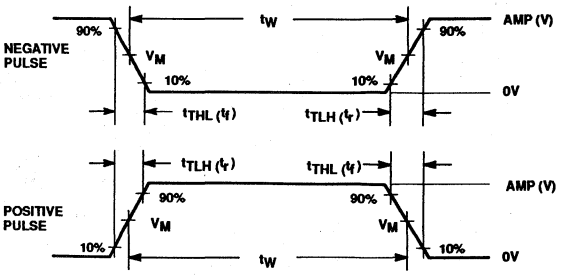
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0371
ECN No.	01122
Date of issue	November 26, 1990
Status	Product Specification
FAST Products	

FAST 74F455, 74F456 Buffers/Drivers

74F455 Octal Buffer/Driver With Parity, Inverting (3-State)
74F456 Octal Buffer/Driver With Parity, Non-Inverting (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F455	6.5ns	64mA
74F456	7.5ns	64mA

FEATURES

- **High impedance NPN base inputs for reduced loading (40µA in High and Low states)**
- **'F455 combines 'F240 and 'F280A functions in one package**
- **'F456 combines 'F244 and 'F280A functions in one package**
- **'F455 and 'F456 are center pin versions of the 'F655A and 'F656A respectively**
- **'F455 Inverting**
  'F456 Non-Inverting
- **3-state outputs sink 64mA and source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Broadside pinout simplifies PC board layout**

DESCRIPTION

The 'F455 and 74F456 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F455N, N74F456N
24-Pin Plastic SOL	N74F455D, N74F456D

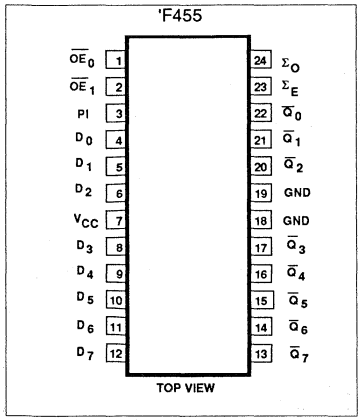
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_7	Data inputs	2.0/0.066	40µA/40µA
PI	Parity input	1.0/0.033	20µA/20µA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA
$\overline{Q}_0$- $\overline{Q}_7$	Data outputs ('F455)	750/106.7	15mA/64mA
Q_0- Q_7	Data outputs ('F456)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

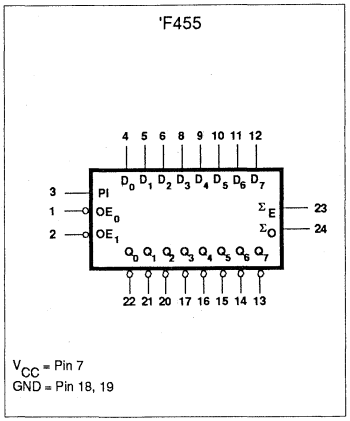
'F455



TOP VIEW

LOGIC SYMBOL

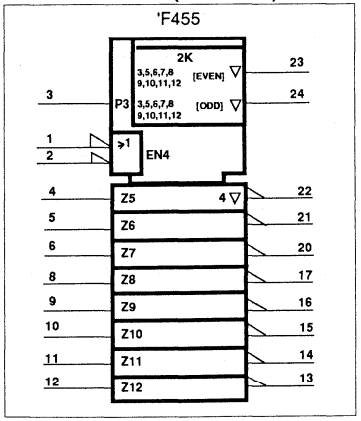
'F455



V_{CC} = Pin 7
GND = Pin 18, 19

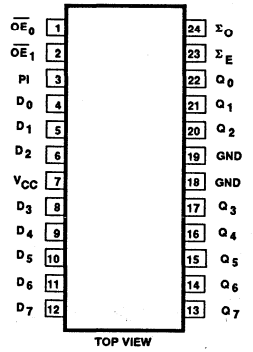
LOGIC SYMBOL(IEEE/IEC)

'F455



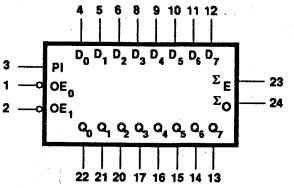
PIN CONFIGURATION

'F456



LOGIC SYMBOL

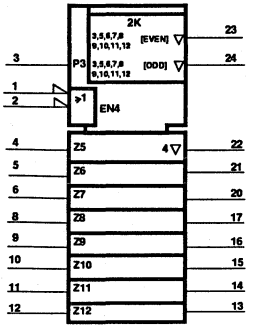
'F456



V_{CC} = Pin 7
GND = Pin 18, 19

LOGIC SYMBOL(IEEE/IEC)

'F456



FUNCTION TABLE

INPUTS			OUTPUTS	
			'F455	'F456
$\overline{OE}_0$	$\overline{OE}_1$	D_n	$\overline{Q}_n$	Q_n
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

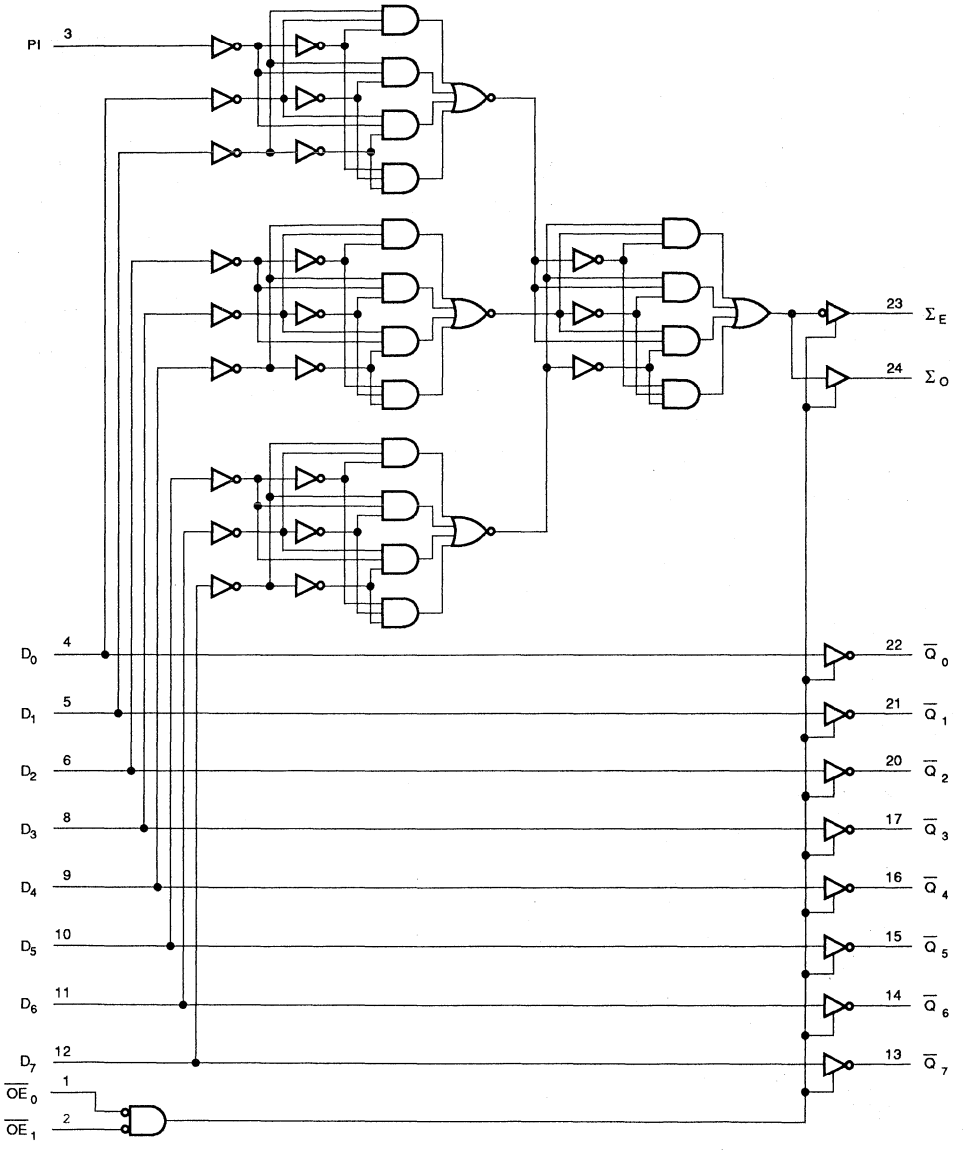
H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state

FUNCTION TABLE for PARITY OUTPUTS

INPUTS	OUTPUTS	
Number of inputs High (PI, D_0-D_7)	Σ_E	Σ_O
Even ------ 0, 2, 4, 6, 8	H	L
Odd ------1, 3, 5, 7, 9	L	H
Any $\overline{OE}_n$=High	Z	Z

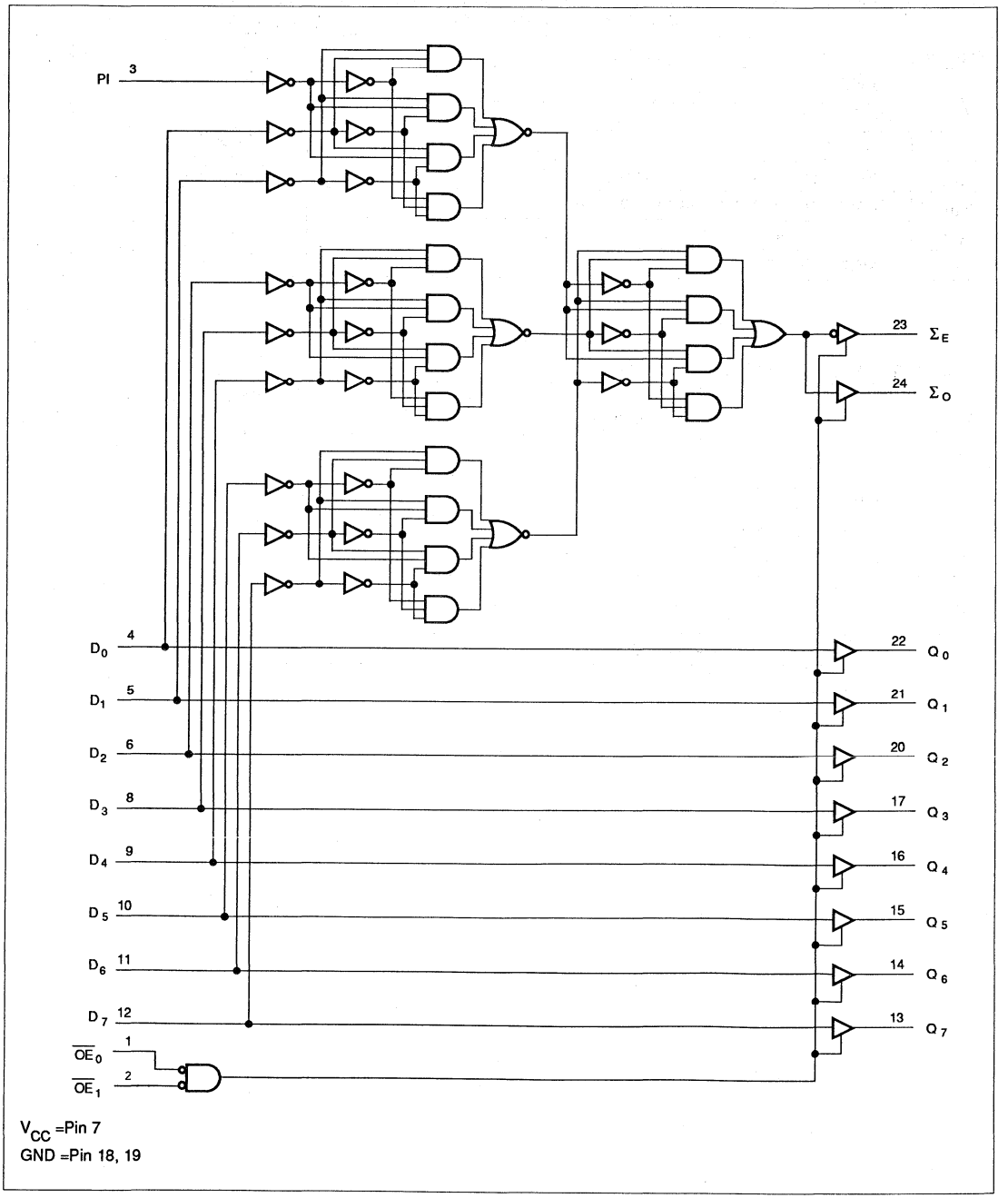
H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state

LOGIC DIAGRAM for 'F455



V_{CC} =Pin 7
GND =Pin 18, 19

LOGIC DIAGRAM for 'F456



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	D_n	V_{CC} = MAX, V_I = 2.7V					40	µA
		PI, $\overline{OE}_n$						20	µA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V					-40	µA
		PI, $\overline{OE}_n$						-20	µA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	80	mA
		I_{CCL}					78	110	mA
		I_{CCZ}					63	90	mA

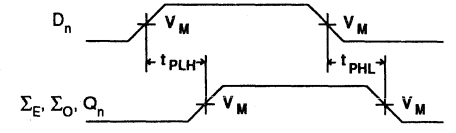
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

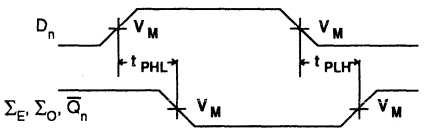
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F455	Waveform 2	2.0 1.0	4.5 2.0	6.5 4.0	2.0 1.0	7.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F456	Waveform 1	2.0 2.5	4.5 5.0	6.5 7.0	2.0 2.5	7.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Σ_E, Σ_O		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.5 4.0	4.0 8.0	8.0 10.5	2.5 4.0	9.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	ns

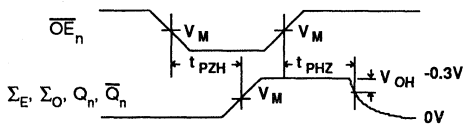
AC WAVEFORMS



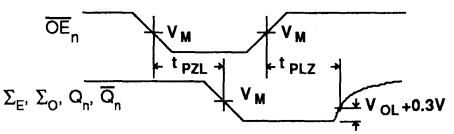
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs



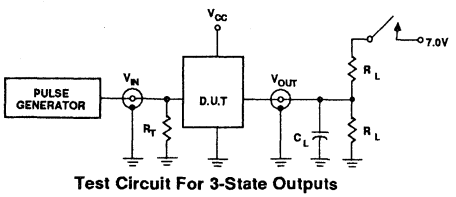
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

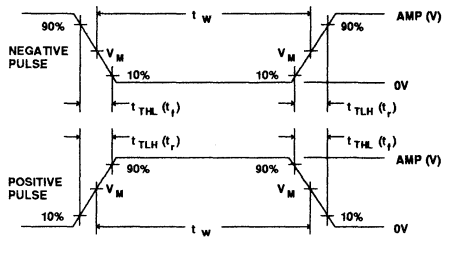
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0372
ECN No.	99601
Date of issue	May 15 , 1990
Status	Product Specification
FAST Products	

FAST 74F521
8-Bit Identity Comparator

Comparator

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F521	7.0ns	24mA

FEATURES

- **Compares two 8-bit words in 6.5ns typical**
- **Expandable to any word length**
- **High speed version of ALS688**

DESCRIPTION

The 74F521 is an expandable 8-bit comparator. It compares two words of up to 8 bits each and provides a Low output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active-Low enable input.

ORDERING INFORMATION

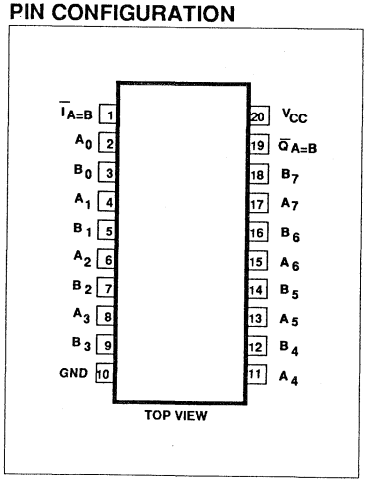
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F521N
20-Pin Plastic SOL	N74F521D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

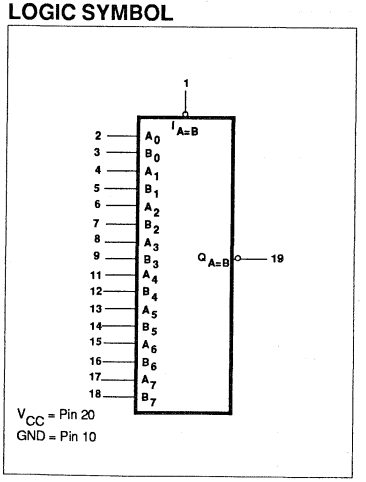
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7	Word A inputs	1.0/1.0	20µA/0.6mA
B_0- B_7	Word B inputs	1.0/1.0	20µA/0.6mA
$\overline{I}_{A=B}$	Expansion or Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Q}_{A=B}$	Identity output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

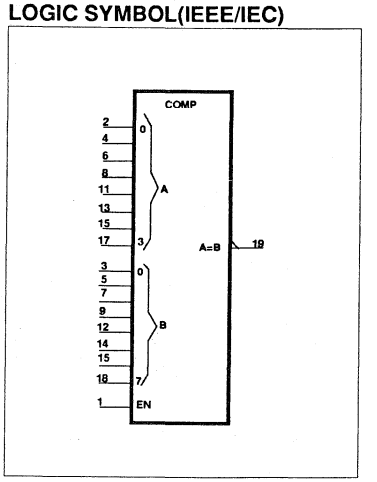
PIN CONFIGURATION



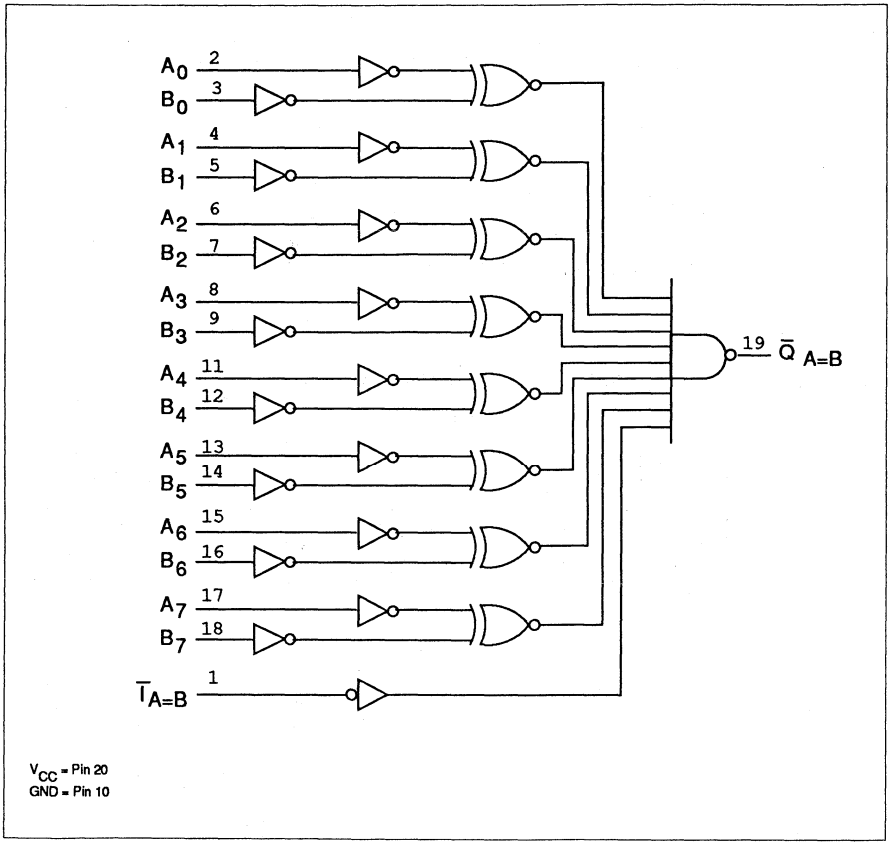
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM

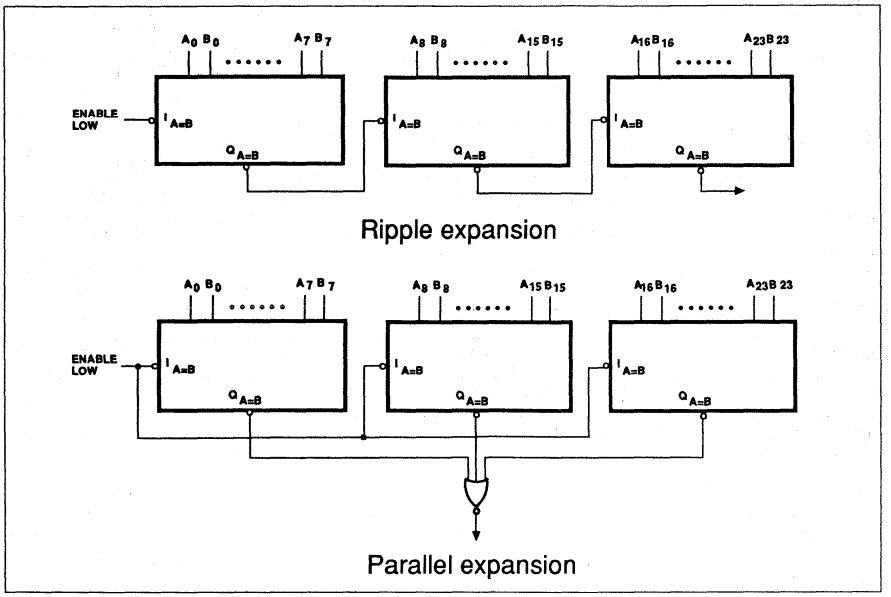


FUNCTION TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{Q}_{A=B}$
L	A=B*	L
L	A≠B	H
H	A=B*	H
H	A≠B	H

H = High voltage level
L = Low voltage level
X = Don't care
*$A_0=B_0$, $A_1=B_1$, $A_2=B_2$, etc.

APPLICATIONS



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

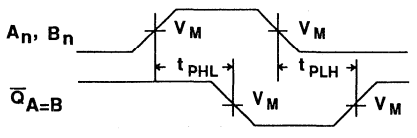
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC} ±5%V_{CC}	2.5 2.7	 3.4	 	V V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC} ±5%V_{CC}	 	0.30 0.30	0.50 0.50	V V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH} I_{CCL}	V_{CC} = MAX		 	24 24	36 36	mA mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

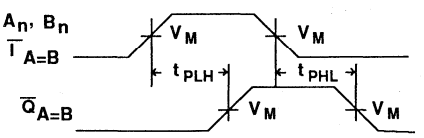
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{Q}_{A=B}$	Waveform1,2	3.5 3.0	8.0 8.0	9.5 9.0	3.5 2.5	11.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_{A=B}$ to $\overline{Q}_{A=B}$	Waveform 2	3.0 3.5	5.0 6.5	6.5 7.0	3.0 3.5	7.5 8.0	ns

AC WAVEFORMS



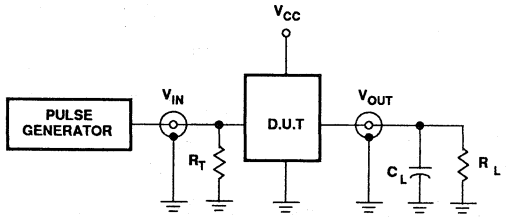
Waveform 1. For Inverting Outputs



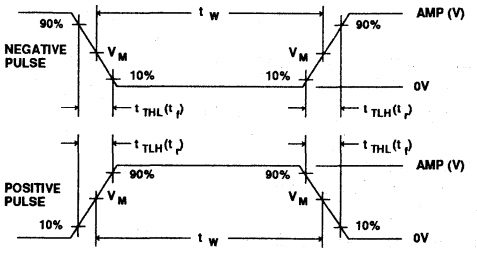
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-0373
ECN No.	00135
Date of issue	August 7, 1990
Status	Product Specification
FAST Products	

FAST 74F524 Comparator

8-Bit Register Comparator (Open Collector+3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F524	65MHz	110mA

FEATURES

- **8-Bit bidirectional register with bus-oriented input-output**
- **Independent serial input-output to register**
- **Register bus comparator with 'equal to', 'greater than' and 'less than' outputs**
- **Cascadable in groups of 8-bits**
- **Open collector comparator outputs for AND-wired expansion**
- **Two's complement or magnitude compare**

DESCRIPTION

The 74F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from MSB to LSB. All data inputs, serial and parallel, are loaded by the rising edge of the clock. The device functions are controlled by two control lines (S_0,S_1) to execute shift, load, hold and read out. An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-High, open collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow Two's Complement as well as magnitude compare. Linking inputs are

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F524N
20-Pin Plastic SOL[1]	N74F524D

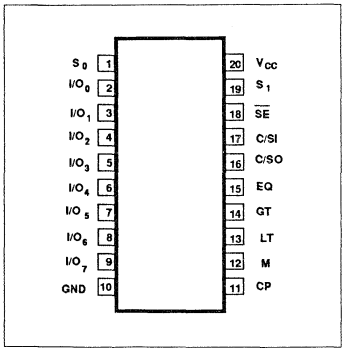
NOTE: 1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

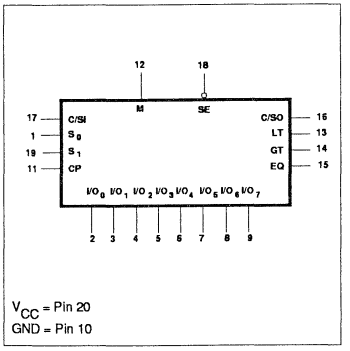
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/On	Parallel data inputs	3.5/1.0	70µA/0.6mA
S_0, S_1	Mode select inputs	1.0/1.0	20µA/0.6mA
C/SI	Status priority or serial data input	1.0/1.0	20µA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SE}$	Status enable input (active Low)	1.0/1.0	20µA/0.6mA
M	Compare mode select input	1.0/1.0	20µA/0.6mA
I/O_n	3-state parallel data outputs	150/40	3.0mA/24mA
C/SO	Status priority or serial data output	50/33	1.0mA/20mA
LT	Register less than bus output	OC/33	OC/20mA
EQ	Register equal to bus output	OC/33	OC/20mA
GT	Register greater than bus output	OC/33	OC/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

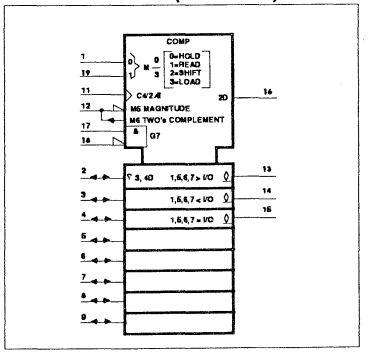
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



provided for expansion to longer words.

FUNCTIONAL DESCRIPTIONS

The 'F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus I/O_0-I/O_7. Serial data is loaded into the register from the C/SI input and may be shifted through the register and out through the C/SO output. Both parallel and serial data entry occurs on the rising edge of the clock (CP). The operation of the shift register is controlled by two signals, S_0 and S_1, according to the Select Function Table. The 3-state parallel output buffers are enabled only in the READ mode.

SELECT FUNCTION TABLE

S_0	S_1	OPERATION
L	L	HOLD-Retains data in shift register
L	H	READ- Read contents in register onto data bus
H	L	SHIFT- Allows serial shifting on next rising clock edge
H	H	LOAD-Load data on bus into register

H=High voltage level
L=Low voltage level

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF Open Collector outputs indicate whether the contents held in the shift register are 'greater than' (GT), 'less than' (LT), or 'equal to' (EQ) the data on the input bus. A High signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A mode control (M) input allows selection between a straightforward magnitude compare or a comparison between Two's complement numbers.

NUMBER REPRESENTAION SELECT TABLE

M	OPERATION
L	Magnitude compare
H	Two's Complement compare

H=High voltage level
L=Low voltage level

FUNCTION TABLE

INPUTS					OUTPUTS				OPERATING MODE
$\overline{SE}$	C/SI	S_0	S_1	Data comparison	EQ	GT	LT	C/SO	
H	H	L	L	X	H	H	H	(1)	Hold
H	L	L	L	X	H	H	H	L	
H	X	H	L	X	H	H	H	Q_0	Shift
H	H	L	H	X	H	H	H	(1)	Read
H	L	L	H	X	H	H	H	L	
H	H	H	H	X	H	H	H	(1)	Load
H	L	H	H	X	H	H	H	L	
L	L	H or L[2]	H or L[2]	O_A-O_H > I/O_0-I/O_7	L	H	H	L	Compare (GT= CT = off)
L	L	H or L[2]	H or L[2]	O_A-O_H = I/O_0-I/O_7	H	H	H	L	
L	L	H or L[2]	H or L[2]	O_A-O_H < I/O_0-I/O_7	L	H	H	L	
L	H	H or L[2]	H or L[2]	O_A-O_H > I/O_0-I/O_7	L	H	L	L	Compare (GT= CT = on)
L	H	H or L[2]	H or L[2]	O_A-O_H = I/O_0-I/O_7	H	L	L	H	
L	H	H or L[2]	H or L[2]	O_A-O_H < I/O_0-I/O_7	L	L	H	L	

(1) = High if $I/O_n = D_n$, otherwise Low

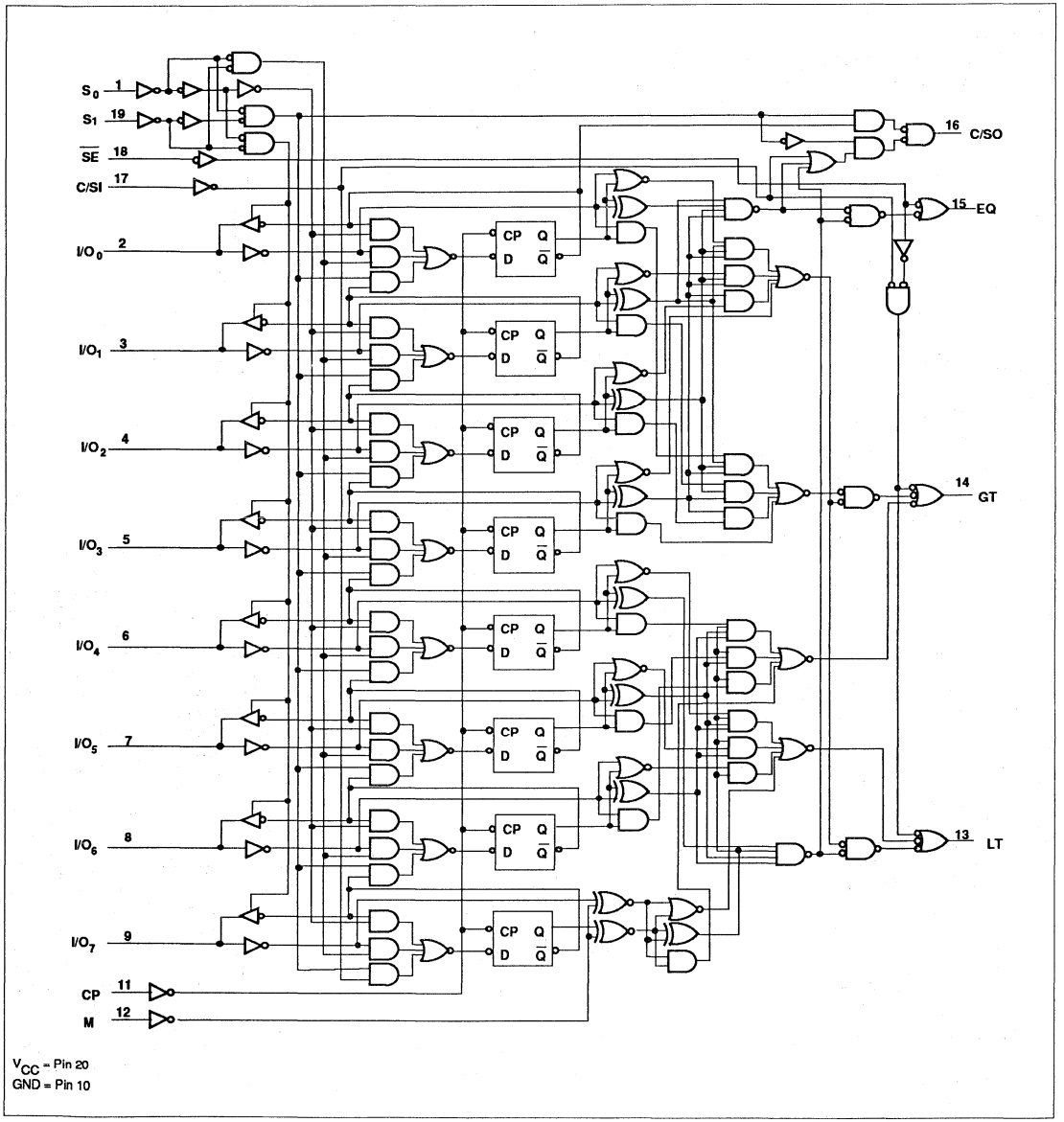
2 = Must meet setup and hold time requirements
H = High voltage level
L = Low voltage level
X = Don't care

For 'greater than' or 'less than' detection, the C/SI input must be held High,as indicated in the Function Table. The internal logic is arranged such that a Low signal on the C/SI input places the 'greater than' and 'less than' outputs in their off state. (Note that this off state serves also as the active state when C/SI is High. It is intended for use in expansion to word lengths greater than 8 bits using multiple 74F524's as explained in the next 3 paragraphs.) The C/SO output will be forced High if the 'equal to' status condition exists; otherwise, C/SO will be held Low.

Word length expansion (in groups of 8 bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see Application Figure 1). The CS/I input of the most significant device is held High while the $\overline{SE}$ input of the least significant device is held Low. The corresponding status outputs are AND-wired together. In the case of two's complement number compare, only the Mode input to the most significant device should be High. The Mode inputs to all other cascaded devices are held Low.

Suppose that an inequality condition is detected in the most signicant device. Assuming that the byte stored in the register is greater than the byte on the data bus, then the EQ and LT outputs will be pulled Low, whereas the GT output will float High. Also, the CS/O output of the most significant device will be forced Low, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go Low, whereas LT output floats High.
If an equality condition is detected in the most significant device, its C/SO output is forced High. This enables the next less significant device and disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving '**n**' cascaded 'F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35+6(**n**-2) ns.

LOGIC DIAGRAM



APPLICATION

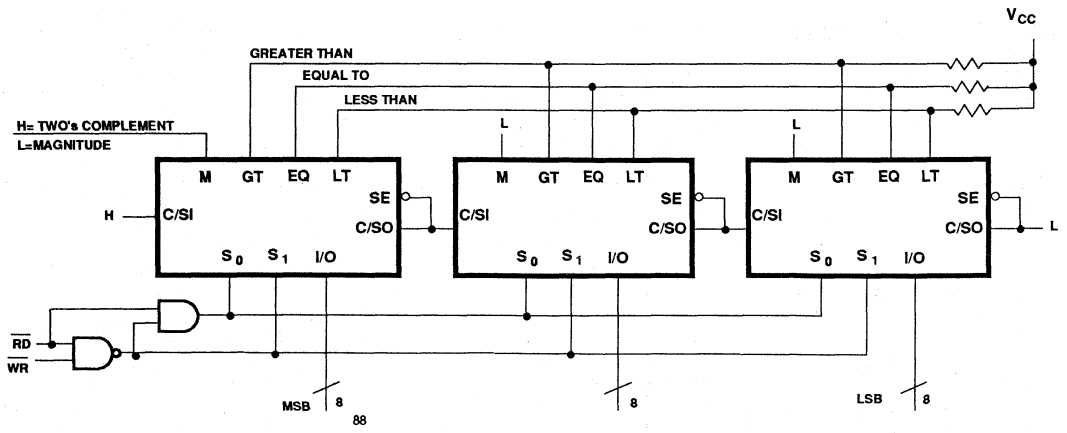


Figure 1. Cascading 'F524s for comparing longer words

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All except I/O	40	mA
		I/O only	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_K	Input clamp current				-18	mA
V_{OH}	High level output voltage	LT, EQ, GT only			4.5	V
I_{OH}	High-level output current	Not LT, EQ, GT, C/SO			-3	mA
		C/SO only			-1	mA
I_{OL}	Low-level output current	All except I/O			20	mA
		I/O only			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	LT, EQ, GT only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	C/SO only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.5			V
		I/O_n only			±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = MAX, V_I = 5.5V					1	mA
		Except I/O_n	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	Except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OZH}	Off-state output current High level voltage applied	I/O_n only	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{OZL}	Off-state output current Low level voltage applied		V_{CC} = MAX, V_O= 0.5V					-0.6	mA
I_{OS}	Short-circuitoutput current[3]	Except LT, EQ, GT	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				110	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

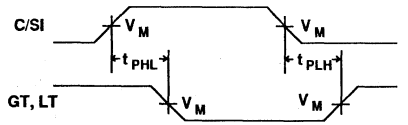
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 4	50	65		45		MHz
t_{PLH} t_{PHL}	Propagation delay I/O_n to EQ	Waveform 2	9.0 4.5	11.5 7.5	17.0 11.0	9.0 4.5	18.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to GT	Waveform 2	8.5 6.5	11.0 9.5	17.0 15.5	8.5 6.5	18.0 16.5	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to LT	Waveform 2	8.0 6.0	11.0 10.5	17.0 14.0	8.0 6.0	18.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to C/SO	Waveform 2	7.0 6.5	13.0 9.0	16.0 14.0	7.0 5.5	17.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to EQ	Waveform 4	11.0 4.0	17.0 8.0	22.0 14.0	10.0 4.0	23.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to GT	Waveform 4	11.0 10.0	16.0 16.5	20.0 21.0	10.0 10.0	21.0 22.0	ns
t_{PHL} t_{PLH}	Propagation delay CP to LT	Waveform 4	11.0 8.0	16.0 14.0	23.0 18.0	10.0 8.0	24.0 19.0	ns
t_{PLH}	Propagation delay CP to C/SO(Load)	Waveform 4	10.0	16.0	20.0	10.0	21.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to C/SO(Serial shift)	Waveform 4	5.0 4.5	10.0 9.0	13.0 11.5	5.0 4.5	14.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to GT	Waveform 1	8.0 3.0	10.5 4.5	16.0 8.5	9.0 2.5	17.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to LT	Waveform 1	8.0 3.0	10.5 6.0	17.0 8.5	8.0 2.5	18.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C/SO	Waveform 2	6.5 5.5	8.0 10.0	14.5 17.0	6.5 5.5	15.5 18.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to EQ	Waveform 2	3.5 2.5	7.0 4.5	10.5 8.0	3.5 2.5	11.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to GT	Waveform 2	6.0 3.5	8.0 5.0	13.0 8.0	6.0 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to LT	Waveform 2	5.0 3.5	8.0 5.5	12.0 8.0	5.0 3.0	13.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay C/SI toC/SO	Waveform 2	4.0 4.0	7.0 7.0	11.0 11.0	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay M to GT	Waveform 2	8.0 8.0	13.0 10.0	18.0 15.5	8.0 8.0	19.0 16.5	ns
t_{PLH} t_{PHL}	Propagation delay M to LT	Waveform 2	10.0 6.0	15.0 8.0	20.0 12.0	10.0 5.0	21.0 13.0	ns
t_{PZH} t_{PZL}	Output Enable time S_n to I/O_n	Waveform 5 Waveform 6	4.5 5.5	7.0 9.0	13.0 15.0	4.5 5.5	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output Disable time S_n to I/O_n	Waveform 5 Waveform 6	3.0 4.5	5.0 8.0	12.0 12.5	2.0 4.5	13.0 13.5	ns

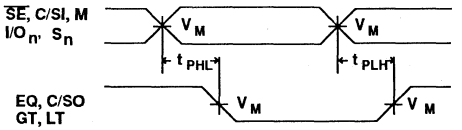
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	6.0 6.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0, S_1 to CP	Waveform 3	13.5 10.0			15.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0, S_1 to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low C/SI to CP	Waveform 3	7.0 7.0			7.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low C/SI to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 4	5.0 10.0			5.0 10.0		ns

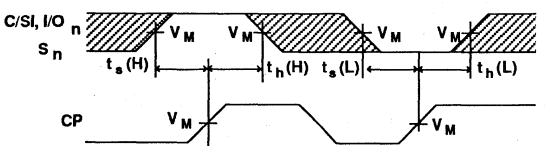
AC WAVEFORMS



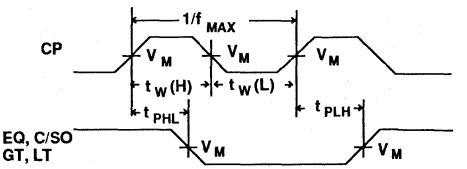
Waveform 1.
Propagation Delay for Inverting outputs



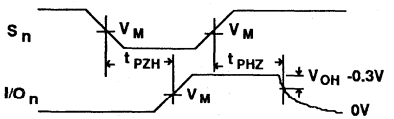
Waveform 2.
Propagation Delay for Non-Inverting outputs



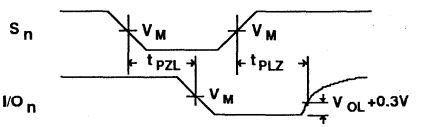
Waveform 3. Setup And Hold Times



Waveform 4. Propagation Delay, Clock To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level

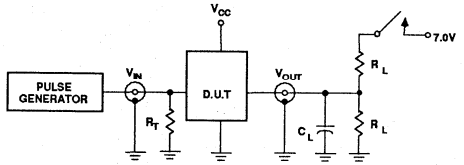


Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State and Open Collector Outputs

SWITCH POSITION

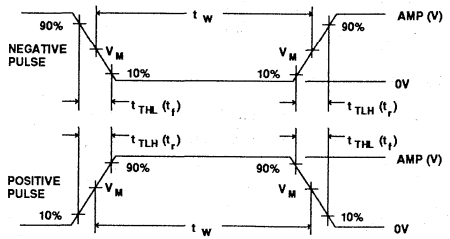
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0374
ECN No.	96611
Date of issue	May 11, 1989
Status	Product Specification
FAST Products	

FAST 74F533, 74F534 Latch/Flip-Flop

74F533 Octal Transparent Latch, Inverting (3-State)
74F534 Octal D Flip-Flop, Inverting (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F533	5.5ns	41mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F534	165MHz	51mA

FEATURES

- **8-bit transparent latch-'F533**
- **8-bit positive edge triggered register-'F534**
- **3-State output buffers**
- **Common 3-state Output register**
- **Independent register and 3-state buffer operation**

DESCRIPTION

The 74F533 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

ORDERING INFORMATION

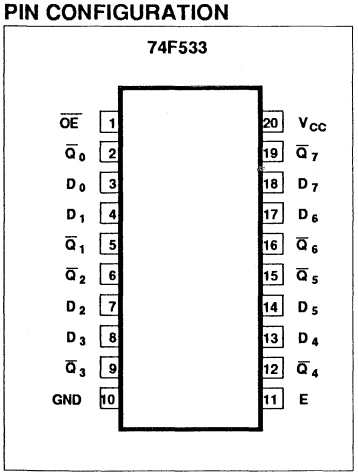
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F533N, N74F534N
20-Pin Plastic SOL	N74F533D, N74F534D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

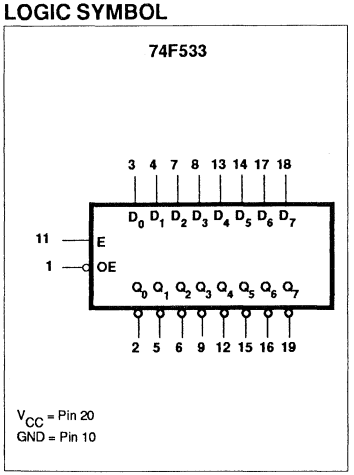
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F533)	Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F534)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

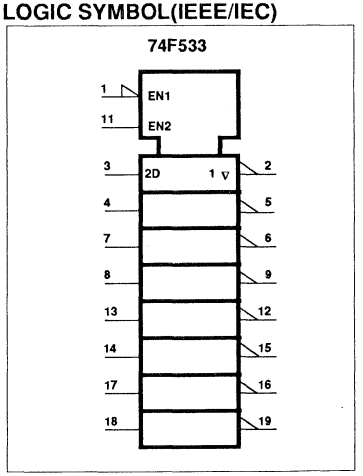
PIN CONFIGURATION



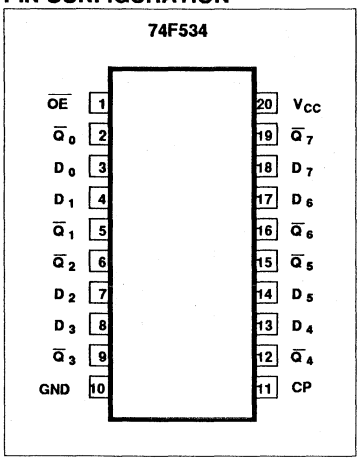
LOGIC SYMBOL



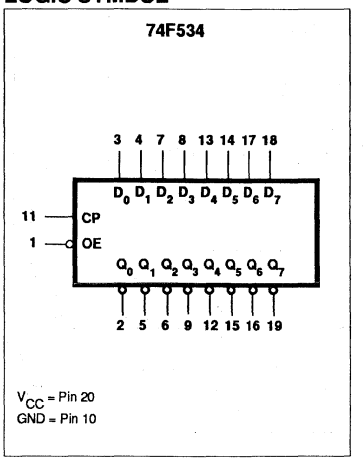
LOGIC SYMBOL(IEEE/IEC)



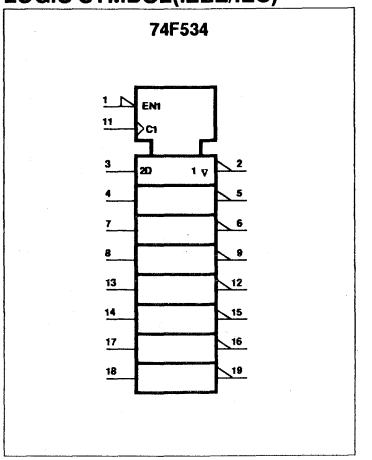
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



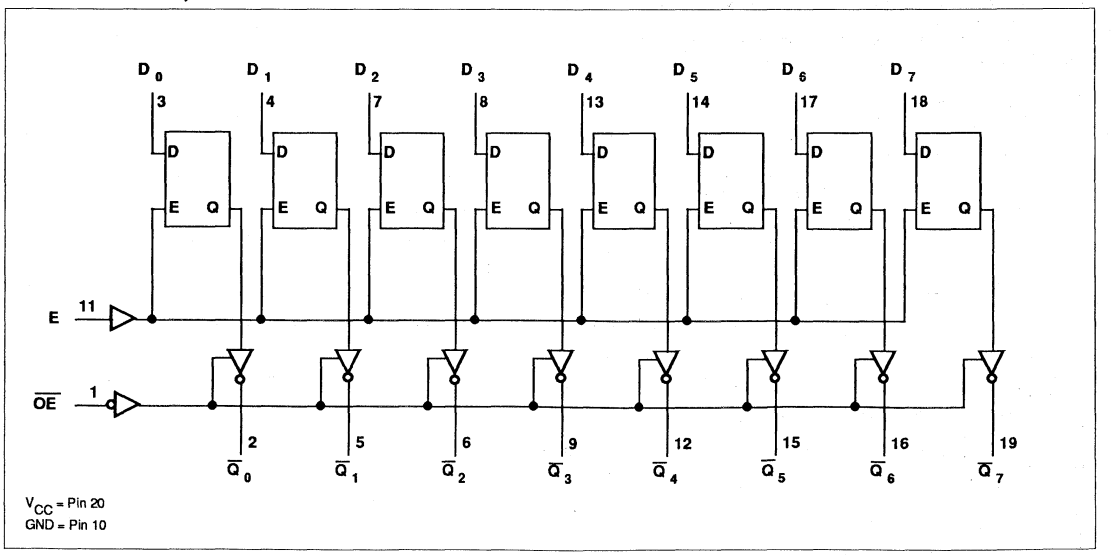
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 'F534 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

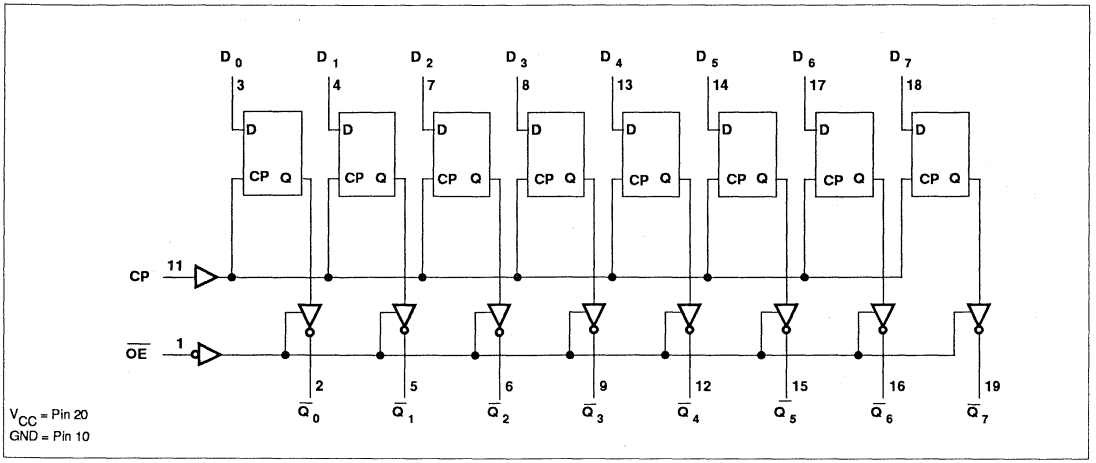
The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's $\overline{Q}$ output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 74F533



LOGIC DIAGRAM, 74F534



FUNCTION TABLE, 74F533

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	$\overline{Q}_0$ - $\overline{Q}_7$	
L	H	L	L	H	Enable and read register
L	H	H	H	L	
L	↓	l	L	H	Latch and read register
L	↓	h	H	L	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	D_n	D_n	Z	

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74F534

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	$\overline{Q}_0$ - $\overline{Q}_7$	
L	↑	l	L	H	Load and read register
L	↑	h	H	L	
L	↟	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	D_n	D_n	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↟ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	74F533	V_{CC} = MAX	$\overline{OE}$=4.5V, D_n=E=GND		41	61	mA
		74F534		$\overline{OE}$=4.5V, D_n=GND		51	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

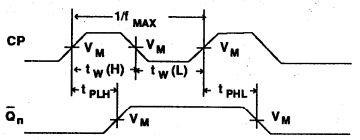
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F533	Waveform 2	4.0 3.0	6.0 4.5	8.5 7.0	4.0 3.0	9.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$		Waveform 3	5.0 3.0	6.5 4.5	9.5 7.0	5.0 3.0	10.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 5.0	7.0 7.0	2.0 2.0	8.0 8.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	3.5 3.0	6.0 5.5	2.0 2.0	7.0 6.5	ns ns
f_{MAX}	Maximum Clock frequency	74F534	Waveform 1	150	165		135		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$		Waveform 1	3.0 3.0	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 5.0	7.5 7.5	2.0 2.0	8.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	3.5 3.5	6.5 5.5	2.0 2.0	7.5 6.5	ns ns

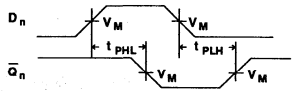
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	74F533	Waveform 4	1.5 0			1.5 0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E		Waveform 4	2.5 2.5			2.5 2.5		ns
$t_w(H)$	E Pulse width, High		Waveform 3	3.0			3.0		ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	74F534	Waveform 5	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	3.0 3.5			3.5 4.0		ns

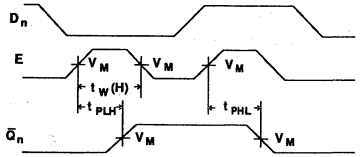
AC WAVEFORMS



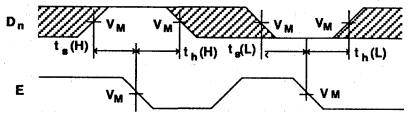
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable, and Clock Pulse Widths, and Maximum Clock Frequency



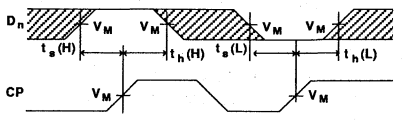
Waveform 2. Propagation Delay For Data To Output



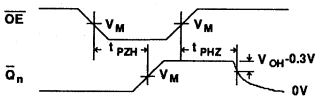
Waveform 3. Propagation Delay, Enable Input To Output, And Enable Pulse Width



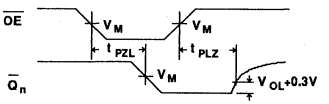
Waveform 4. Data Setup And Hold Times



Waveform 5. Data Setup And Hold Times



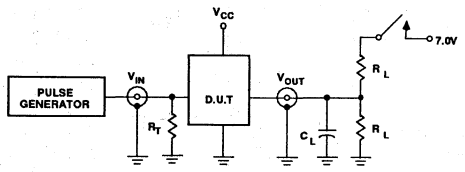
Waveform 6. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 7. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



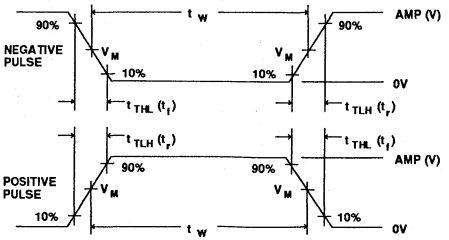
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0873
ECN No.	95586
Date of issue	January 20, 1989
Status	Product Specification
FAST Products	

FAST 74F537
1-Of-10 Decoder (3-state)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F537	9 ns	44mA

DESCRIPTION

The 74F537 is one of ten decoder/demultiplexer with four active High BCD inputs and ten mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low or active High. The 'F537 has 3-state outputs, and a High signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high impedance state. Two input Enables, active High (E_1) and active Low ($\overline{E}_0$), are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine causes all outputs to go to the inactive state (i.e., same polarity as the P input).

ORDERING INFORMATION

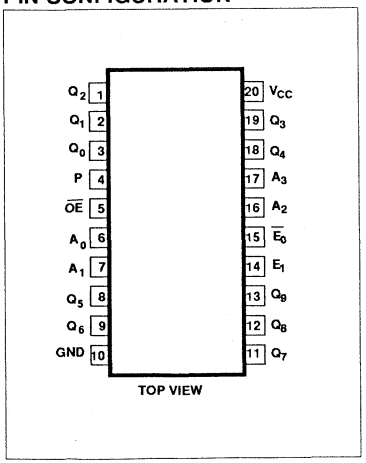
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F537N
20-Pin Plastic SOL	N74F537D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

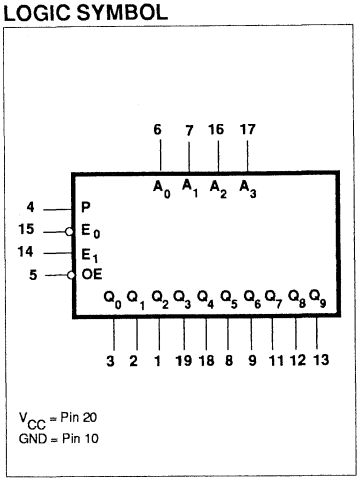
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_0$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
E_1	Enable input (active High)	1.0/1.0	20µA/0.6mA
P	Polarity control input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input	1.0/1.0	20µA/0.6mA
Q_0 - Q_9	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

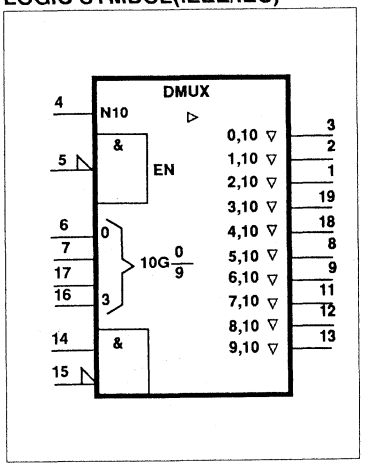
PIN CONFIGURATION



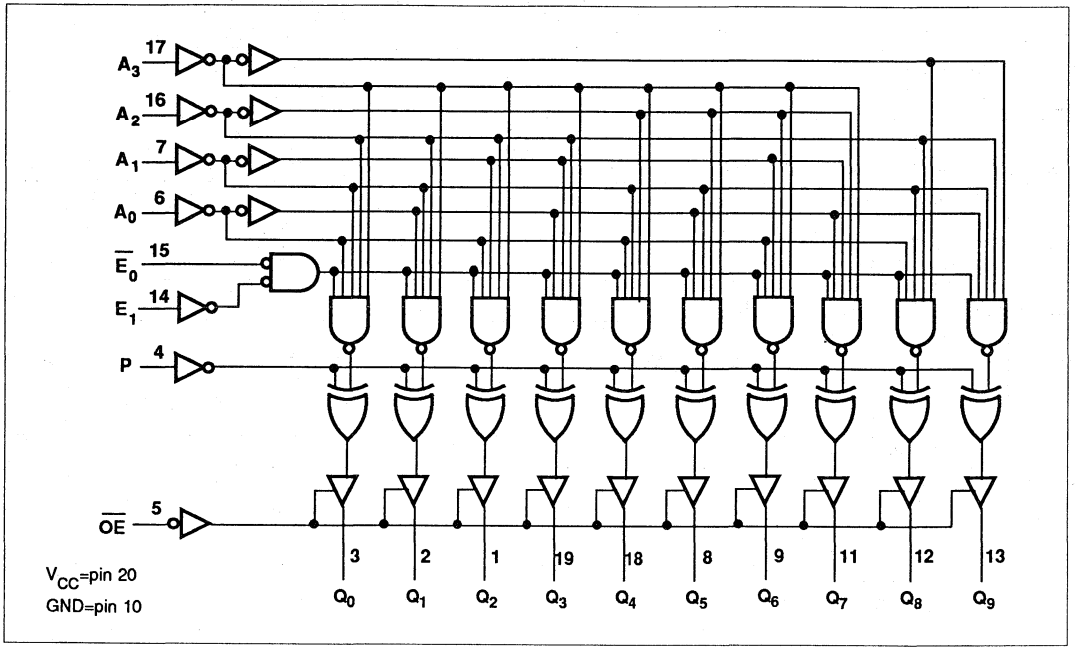
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS										OPERATING MODE
$\overline{OE}$	$\overline{E}_0$	E_1	A_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	
H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High impedance
L	H	X	X	X	X	X	Outputs equal P input										Disable
L	X	L	X	X	X	X											
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Active High output (P=L)
L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L	
L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	
L	L	H	L	H	L	H	L	L	L	L	L	H	L	L	L	L	
L	L	H	L	H	H	L	L	L	L	L	L	L	H	L	L	L	
L	L	H	L	H	H	H	L	L	L	L	L	L	L	H	L	L	
L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	
L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	
L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	X	X	L	L	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	Active Low output (P=H)
L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H	
L	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H	
L	L	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H	
L	L	H	L	H	L	H	H	H	H	H	H	L	H	H	H	H	
L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	
L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H	
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L	
L	L	H	H	X	H	X	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	X	X	H	H	H	H	H	H	H	H	H	H	

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			44	66	mA

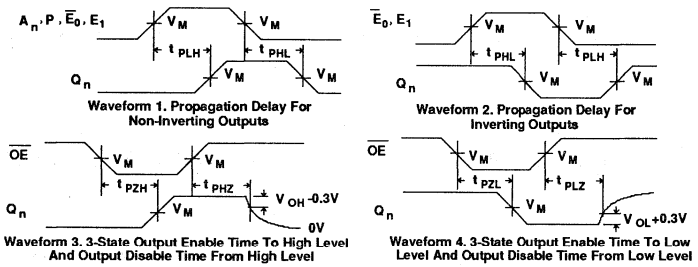
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

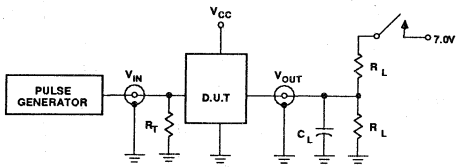
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1	4.5 3.0	9.0 7.5	14.0 11.0	4.5 3.0	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ to Q_n	Waveform 2	4.0 3.0	8.0 8.0	11.0 11.0	4.0 3.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay E_1 to Q_n	Waveform 2	6.0 4.0	8.5 8.5	11.5 11.5	6.0 4.0	13.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1	5.0 3.5	12.5 6.5	16.0 10.0	5.0 3.5	17.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	2.5 4.0	4.5 5.5	7.0 8.0	2.5 4.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	1.5 2.0	3.0 4.0	6.0 6.5	1.0 2.0	7.0 7.0	ns

AC WAVEFORMS

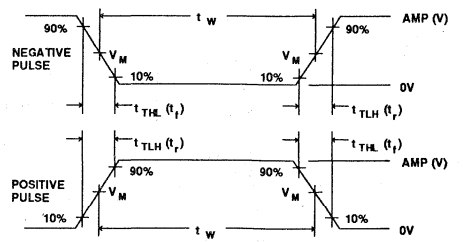


NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-1273
ECN No.	96267
Date of issue	April 6, 1989
Status	Product Specification
FAST Products	

FAST 74F538
1-Of-8 Decoder (3-state)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F538	8.5 ns	35mA

DESCRIPTION

The 74F538 decoder/demultiplexer accepts three address (A_0 - A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low or active High. The 'F538 has 3-state outputs, and a High signal on the Output Enables ($\overline{OE}_0$) inputs will force all outputs to the high impedance state. Two active High (E_2, E_2) and active Low ($\overline{E}_0$, $\overline{E}_1$) inputs are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

ORDERING INFORMATION

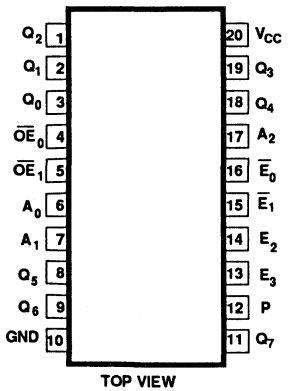
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F538N
20-Pin Plastic SOL	N74F538D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
E_2, E_3	Enable inputs (active High)	1.0/1.0	20µA/0.6mA
P	Polarity control input	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

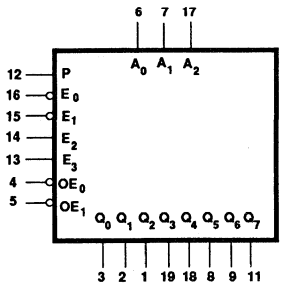
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



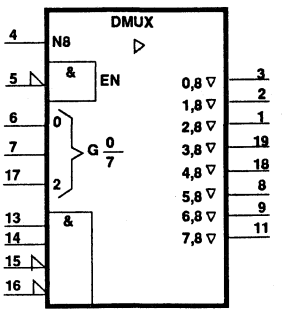
TOP VIEW

LOGIC SYMBOL

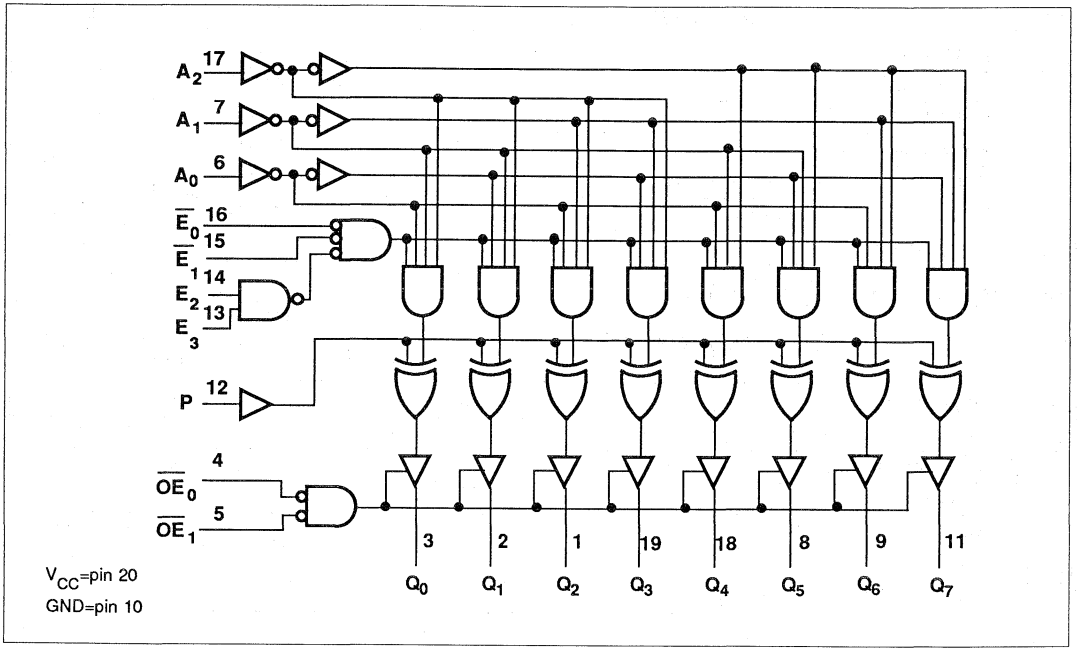


V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS								OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	High impedance
X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	
L	L	H	X	X	X	X	X	X	Outputs equal P input								Disable
L	L	X	H	X	X	X	X	X									
L	L	X	X	L	X	X	X	X									
L	L	X	X	X	L	X	X	X									
L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	Active High output (P=L)
L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L	
L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L	
L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L	
L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L	
L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L	
L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L	
L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H	
L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H	Active Low output (P=H)
L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	
L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				35	50	mA
		I_{CCZ}				35	50	mA

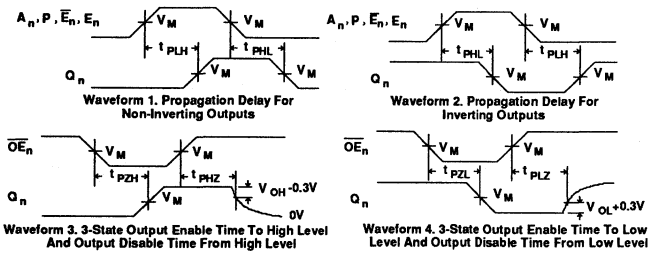
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1, 2	5.5 3.0	8.5 7.5	13.0 12.5	5.0 3.0	14.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to Q_n	Waveform 1, 2	5.5 3.0	8.5 7.5	12.0 12.0	5.0 3.0	13.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay E_2 or E_3 to Q_n	Waveform 1, 2	6.5 4.0	9.0 7.0	12.5 12.5	5.5 3.5	13.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1, 2	4.5 3.5	9.5 6.5	15.0 10.0	4.0 3.5	16.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	2.5 6.5	5.5 9.5	9.5 13.5	2.0 6.0	11.0 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	1.0 1.0	3.0 3.5	6.0 8.5	1.0 1.0	7.0 9.5	ns

AC WAVEFORMS



Waveform 1. Propagation Delay For Non-Inverting Outputs

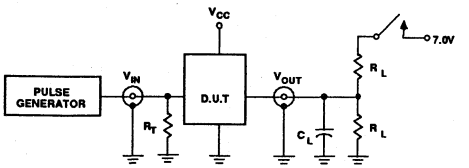
Waveform 2. Propagation Delay For Inverting Outputs

Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

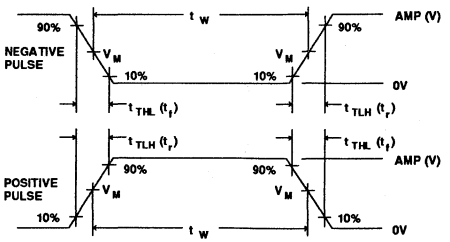
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-1274
ECN No.	98905
Date of issue	Febnruary 23, 1990
Status	Product Specification
FAST Products	

FAST 74F539
Dual 1-Of-4 Decoder (3-state)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F539	7.5 ns	40mA

DESCRIPTION

The 74F539 contains two independent decoders. Each accepts two address (A_0 - A_1) input signals and decodes them to select one of four mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low (P=H) or active High (P=L). An active-Low Enable ($\overline{E}$) is available for data demultiplexing. Data is routed to the selected output in non-inverted or inverted form in the active-Low mode or inverted form in the active-High mode.A High signal on the Output Enable ($\overline{OE}_n$) input forces the 3-state outputs to the high impedance state.

ORDERING INFORMATION

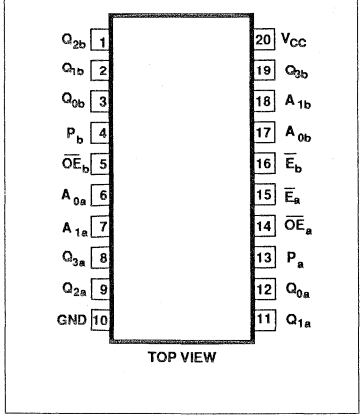
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F539N
20-Pin Plastic SOL	N74F539D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{0a} , A_{1a}	Decoder A Address inputs	1.0/1.0	20µA/0.6mA
A_{0b} , A_{1b}	Decoder B Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Enable inputs (activc Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_a$, $\overline{OE}_b$	Output enable inputs (active Low)	1.0/1.0	20µA/0.6mA
P_a, P_b	Polarity control inputs	1.0/1.0	20µA/0.6mA
Q_{0a} - Q_{3a}	Decoder A Data outputs	150/40	3.0mA/24mA
Q_{0b} - Q_{3b}	Decoder B Data outputs	150/40	3.0mA/24mA

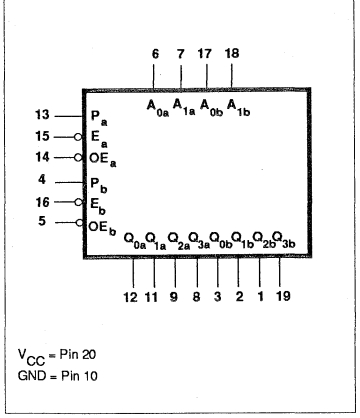
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



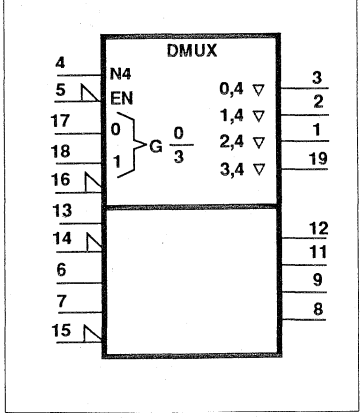
TOP VIEW

LOGIC SYMBOL

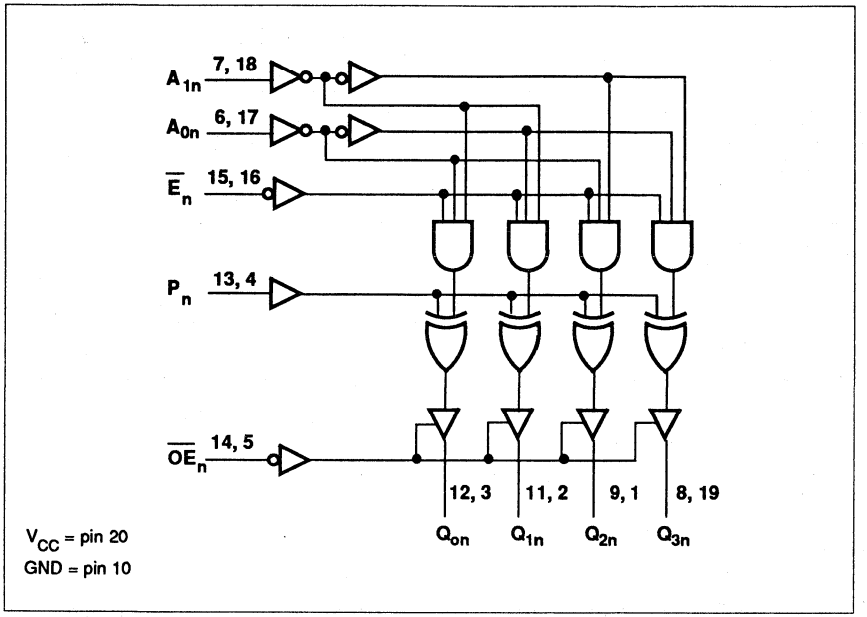


V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS				OPERATING MODE
$\overline{OE}_n$	$\overline{E}_n$	A_{1n}	A_{0n}	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}	
H	X	X	X	Z	Z	Z	Z	High impedance
L	H	X	X	$Q_n = P$				Disable
L	L	L	L	H	L	L	L	Active High output (P=L)
L	L	L	H	L	H	L	L	
L	L	H	L	L	L	H	L	
L	L	H	H	L	L	L	H	
L	L	L	L	L	H	H	H	Active Low output (P=H)
L	L	L	H	H	L	H	H	
L	L	H	L	H	H	L	H	
L	L	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off "state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		35	50	mA
		I_{CCL}			40	55	mA
		I_{CCZ}			40	60	m

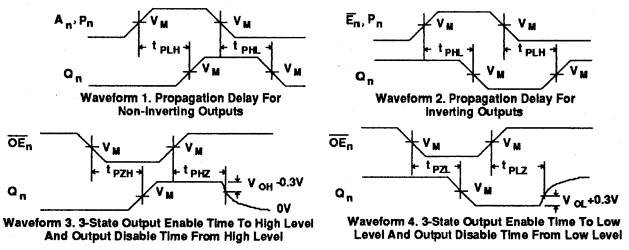
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

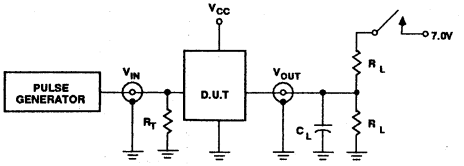
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1	4.5 3.0	8.5 8.0	12.5 12.5	4.0 3.0	13.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n	Waveform 2	5.0 3.0	7.5 7.0	11.0 11.0	4.5 3.0	12.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay P_n to Q_n	Waveform 1	4.0 3.5	6.5 5.5	9.5 9.0	3.5 3.0	10.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay P_n to Q_n (INV)	Waveform 2	6.0 4.0	11.5 6.0	14.5 9.0	5.0 4.0	15.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to Q_n	Waveform 3 Waveform 4	2.5 5.5	4.0 7.0	7.5 10.5	2.0 5.0	8.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to Q_n	Waveform 3 Waveform 4	1.5 2.0	3.0 4.0	6.0 8.0	1.0 1.5	6.5 8.5	ns

AC WAVEFORMS

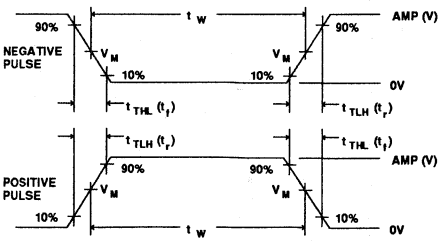


NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0068
ECN No.	98494
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F540, 74F541
Buffers

74F540 Octal Inverter Buffer (3-State)
74F541 Octal Buffer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F540	3.5ns	58mA
74F541	5.5ns	55mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Low power, light bus loading**
- **Functional similar to the 'F240 and 'F241**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **Efficient pinout to facilitate PC board layout**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION

The 74F540 and 74F541 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The devices feature input and outputs on opposite sides of the package to facilitate printed circuit board layout.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F540N, N74F541N
20-Pin Plastic SOL	N74F540D, N74F541D

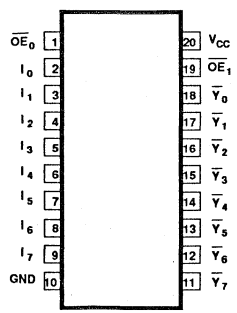
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0- I_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$ $\overline{OE}_1$	3-state output enable inputs (active Low)	1.0/0.033	20μA/20μA
Y_0- Y_7	Data outputs ('F541)	750/106.7	15mA/64mA
$\overline{Y}_0$- $\overline{Y}_7$	Data outputs ('F540)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

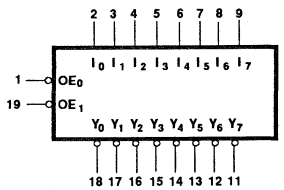
PIN CONFIGURATION

74F540



LOGIC SYMBOL

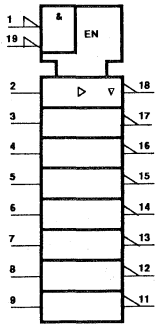
74F540



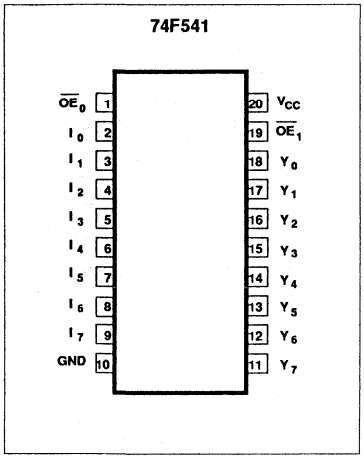
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

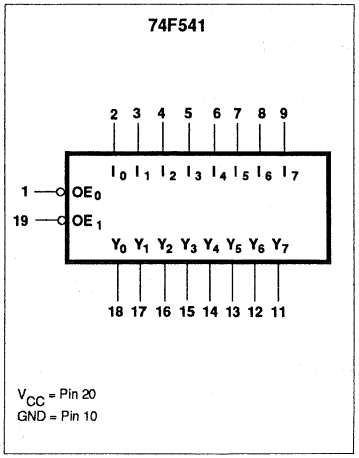
74F540



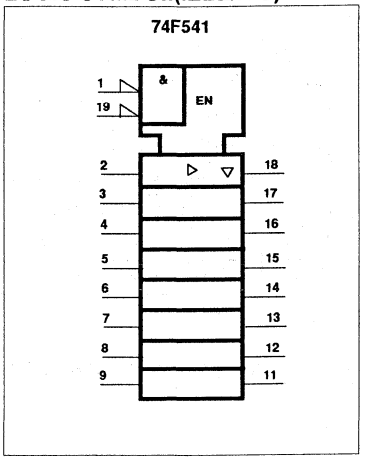
PIN CONFIGURATION



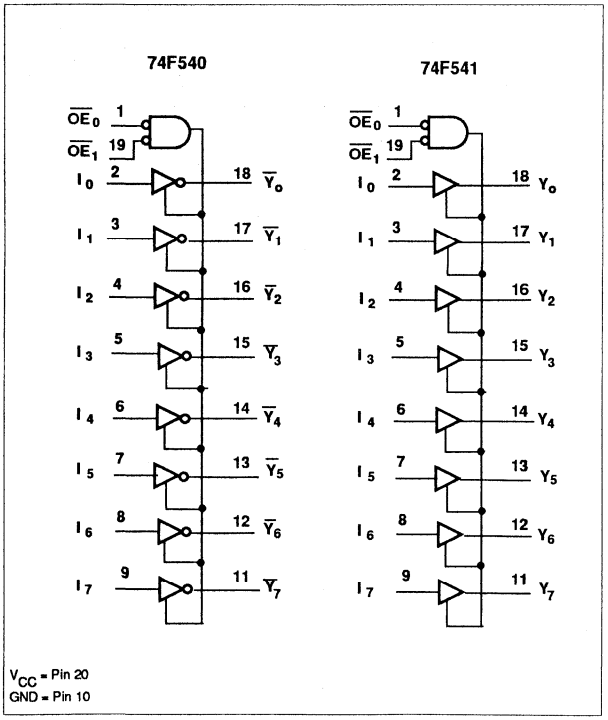
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	
			'F541	'F540
$\overline{OE}_0$	$\overline{OE}_1$	I_n	Y_n	$\overline{Y}_n$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH}=-15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F540	I_{CCH}	V_{CC} = MAX	I_n=$\overline{OE}_n$=GND			22	30	mA
			I_{CCL}		I_n=4.5V, $\overline{OE}_n$=GND			58	75	mA
			I_{CCZ}		I_n=GND, $\overline{OE}_n$=4.5V			40	55	mA
		'F541	I_{CCH}		I_n=4.5V, $\overline{OE}_n$=GND			30	40	mA
			I_{CCL}		I_n=$\overline{OE}_n$=GND			55	72	mA
			I_{CCZ}		I_n=GND, $\overline{OE}_n$=4.5V			45	58	mA

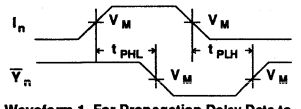
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

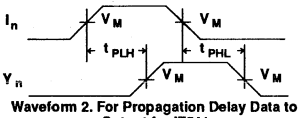
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				$T_A = +25°C$, $V_{CC} = 5V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	74F540	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.0 4.0	3.5 7.5	6.5 9.5	2.0 4.0	7.0 10.0	ns
t_{PZH} t_{PZL}	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	74F541	Waveform 2	2.5 3.5	5.0 6.0	6.5 7.0	2.5 3.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	3.0 3.0	5.5 6.5	7.0 8.5	3.0 3.0	7.5 9.5	ns
t_{PZH} t_{PZL}	Output Disable time from High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns

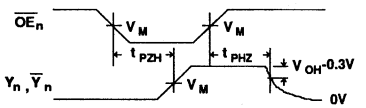
AC WAVEFORMS



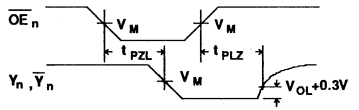
Waveform 1. For Propagation Delay Data to Output for 'F540



Waveform 2. For Propagation Delay Data to Output for 'F541



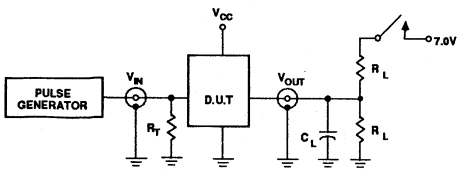
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

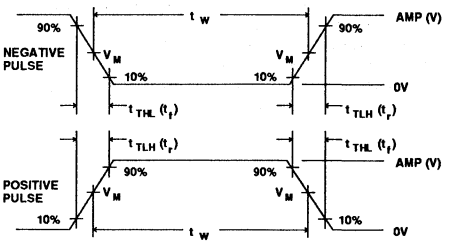
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Bus transceivers | FAST 74F543, 74F544

74F543 octal registered transceiver, non-inverting (3-State)

74F544 octal registered transceiver, inverting (3-State)

FEATURES

- Combines 74F245 and 74F373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- 'F543 non-inverting
  'F544 inverting
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24mA and source 3mA
- B outputs sink 64mA and source 15mA
- 300 mil wide 24-pin Slim DIP package
- 3-State outputs for bus-orientated applications

DESCRIPTION

The 74F543 and 74F544 octal registered transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable (LEAB, LEBA) and Output Enable (OEAB, OEBA) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. While the 'F543 has non-inverting data path, the 'F544 inverts data in both directions. The A outputs are guaranteed to sink 24mA while the B outputs are rated for 64mA.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F543	6.0ns	80mA
74F544	6.5ns	95mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-pin plastic slim DIP (300mil)	N74F543N, N74F544N
24-pin plastic SOL	N74F543D, N74F544D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F543 'F544	A_0 - A_7	Port A, 3-State inputs	3.5/1.0	70µA/0.6mA
	B_0 - B_7	Port B, 3-State inputs	3.5/1.0	70µA/0.6mA
	$\overline{OEAB}$	A-to-B Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{OEBA}$	B-to-A Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{EAB}$	A-to-B Enable input (Active Low)	1.0/2.0	20µA/1.2mA
	$\overline{EBA}$	B-to-A Enable input (Active Low)	1.0/2.0	20µA/1.2mA
	$\overline{LEAB}$	A-to-B Latch Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{LEBA}$	B-to-A Latch Enable input (Active Low)	1.0/1.0	20µA/0.6mA
'F543	A_0 - A_7	Port A, 3-State outputs	150/40	3.0mA/24mA
	B_0 - B_7	Port B, 3-State outputs	750/106.7	15mA/64mA
'F544	$\overline{A_0}$ - $\overline{A_7}$	Port $\overline{A}$, 3-State outputs	150/40	3.0mA/24mA
	$\overline{B_0}$ - $\overline{B_7}$	Port $\overline{B}$, 3-State outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

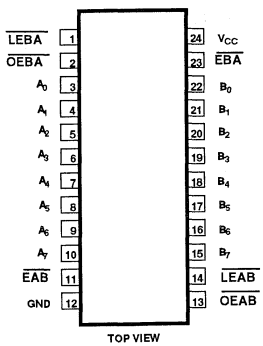
FUNCTIONAL DESCRIPTION

The 'F543 and 'F544 contain two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) input must be Low in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the Function Table. With $\overline{EAB}$ Low, a Low

(continued)

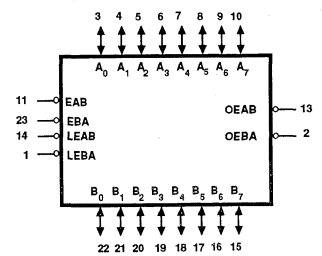
PIN CONFIGURATION

'F543



LOGIC SYMBOL

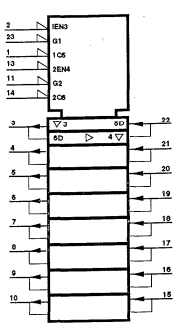
'F543



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

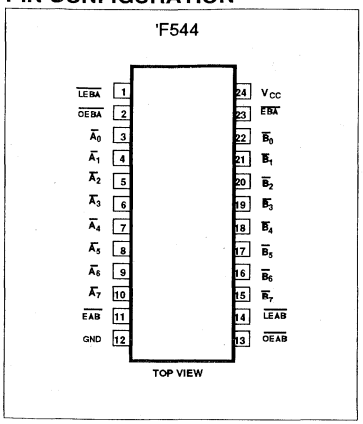
'F543



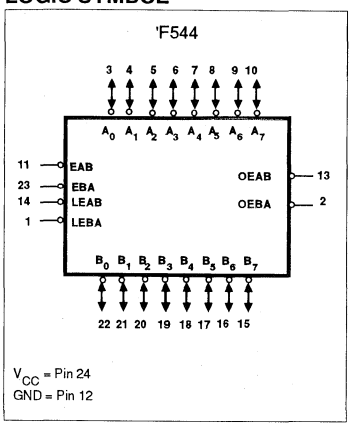
signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B latches transparent; a subsequent Low-to High transition of the LEAB signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With EAB and OEAB both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the EBA, LEBA, and OEBA inputs.

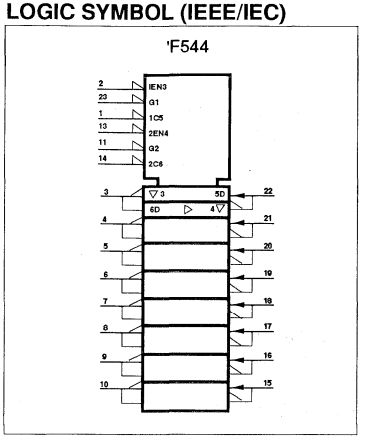
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

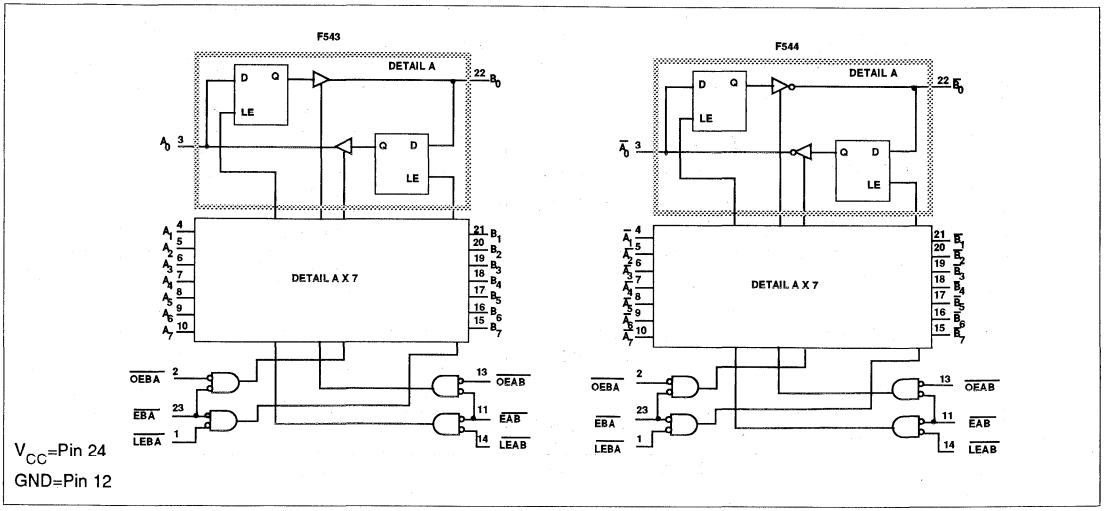


FUNCTION TABLE for 'F543 and 'F544

INPUTS				OUTPUTS		STATUS
OEXX	EXX	LEXX	DATA	'F543	'F544	
H	X	X	X	Z	Z	Disabled
X	H	X	X	Z	Z	Disabled
L	↑	L	h	Z	Z	Disabled + Latch
L	↑	L	l	Z	Z	
L	L	↑	h	H	L	Latch + Display
L	L	↑	l	L	H	
L	L	L	H	H	L	Transparent
L	L	L	L	L	H	
L	L	H	X	NC	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of LEXX or EXX (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of LEXX or EXX (XX=AB or BA)
↑ =Low-to-High transition of LEXX or EXX (XX=AB or BA)
X = Don't care
NC = No change
Z =High impedance "off" state

LOGIC DIAGRAM



V_{CC}=Pin 24
GND=Pin 12

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7, $\overline{A}_0$-$\overline{A}_7$	48	mA
		B_0-B_7, $\overline{B}_0$-$\overline{B}_7$	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7, $\overline{A}_0$-$\overline{A}_7$			-3	mA
		B_0-B_7, $\overline{B}_0$-$\overline{B}_7$			-15	mA
I_{OL}	Low-level output current	A_0-A_7, $\overline{A}_0$-$\overline{A}_7$			24	mA
		B_0-B_7, $\overline{B}_0$-$\overline{B}_7$			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	A_0-A_7, $\overline{A_0}$-$\overline{A_7}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7, $\overline{B_0}$-$\overline{B_7}$		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7, $\overline{A_0}$-$\overline{A_7}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7, $\overline{B_0}$-$\overline{B_7}$		I_{OL}=64mA	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	OEAB, OEBA, EAB	V_{CC} =MAX, V_I =7.0V					100	µA
		Others	V_{CC} =5.5, V_I =5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		EAB, EBA						-1.2	mA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZH} + I_{IL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-600	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7, $\overline{A_0}$-$\overline{A_7}$	V_{CC} = MAX			-60		-150	mA
		B_0-B_7, $\overline{B_0}$-$\overline{B_7}$				-100		-225	mA
I_{CC}	Supply current (total)	'F543	I_{CCH}	V_{CC} = MAX			70	105	mA
			I_{CCL}				95	135	mA
			I_{CCZ}				95	135	mA
		'F544	I_{CCH}	V_{CC} = MAX			80	110	mA
			I_{CCL}				105	140	mA
			I_{CCZ}				100	135	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F543

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.5 2.5	4.0 4.5	7.0 7.5	2.5 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to A_n	Waveform 1,2	5.0 4.0	7.0 6.0	10.0 9.0	4.5 4.0	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to B_n	Waveform 1,2	6.0 4.5	8.5 6.5	11.5 9.5	5.5 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to A_n or $\overline{OEAB}$ to B_n	Waveform 4 Waveform 5	2.0 3.5	4.0 5.0	7.5 8.5	1.5 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to A_n or $\overline{OEAB}$ to B_n	Waveform 4 Waveform 5	1.0 1.5	3.0 4.0	6.5 7.5	1.0 1.0	7.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to A_n or $\overline{EAB}$ to B_n	Waveform 4 Waveform 5	4.5 5.0	7.0 7.0	10.5 10.5	4.0 4.5	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to A_n or $\overline{EAB}$ to B_n	Waveform 4 Waveform 5	2.5 4.5	5.0 7.0	8.5 11.0	2.0 3.0	9.5 12.0	ns

AC SETUP REQUIREMENTS for 74F543

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	0.0 2.5			0.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	0.0 1.5			0.0 2.0		ns
t_s(H) t_s(L)	Setup time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	1.0 2.5			1.5 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	0.0 1.5			0.0 2.0		ns
t_w(L)	Latch enable Pulse width, Low	Waveform 3	4.0			4.5		ns

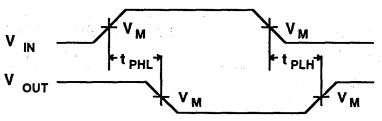
AC ELECTRICAL CHARACTERISTICS for 74F544

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A_n}$ to B_n or $\overline{B_n}$ to A_n	Waveform 1	3.0 3.0	6.5 5.0	9.5 8.0	3.0 3.0	10.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to $\overline{A_n}$	Waveform 1,2	4.0 4.0	7.0 7.0	9.5 9.5	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to $\overline{B_n}$	Waveform 1,2	5.0 4.0	8.0 7.5	11.5 9.5	4.0 4.0	12.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to $\overline{A_n}$ or $\overline{OEAB}$ to $\overline{B_n}$	Waveform 4 Waveform 5	2.0 3.5	4.0 5.5	7.0 8.5	1.5 3.0	7.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to $\overline{A_n}$ or $\overline{OEAB}$ to $\overline{B_n}$	Waveform 4 Waveform 5	1.0 1.5	4.0 4.0	6.5 6.5	1.0 1.5	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to $\overline{A_n}$ or $\overline{EAB}$ to $\overline{B_n}$	Waveform 4 Waveform 5	4.0 4.5	7.0 8.0	9.5 11.0	3.5 4.5	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to $\overline{A_n}$ or $\overline{EAB}$ to $\overline{B_n}$	Waveform 4 Waveform 5	2.5 4.5	5.0 8.5	8.0 11.5	2.5 4.0	9.0 11.5	ns

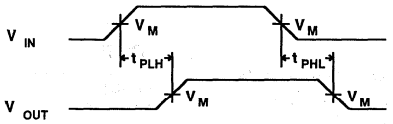
AC SETUP REQUIREMENTS for 74F544

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{A_n}$ to $\overline{LEAB}$ or $\overline{B_n}$ to $\overline{LEBA}$	Waveform 3	1.5 1.5			2.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{A_n}$ to $\overline{LEAB}$ or $\overline{B_n}$ to $\overline{LEBA}$	Waveform 3	1.5 2.0			2.5 2.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{A_n}$ to $\overline{EAB}$ or $\overline{B_n}$ to $\overline{EBA}$	Waveform 3	1.5 1.5			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{A_n}$ to $\overline{EAB}$ or $\overline{B_n}$ to $\overline{EBA}$	Waveform 3	1.5 2.0			2.0 2.0		ns
$t_w(L)$	Latch enable Pulse width, Low	Waveform 3	4.0			4.5		ns

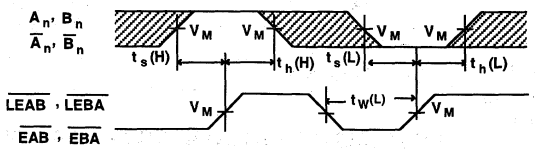
AC WAVEFORMS



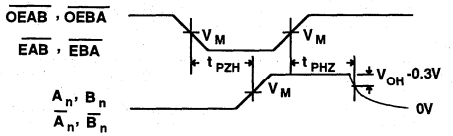
Waveform 1. Propagation Delay For Inverting Output



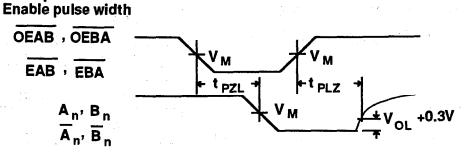
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup And Hold Times And Latch Enable pulse width



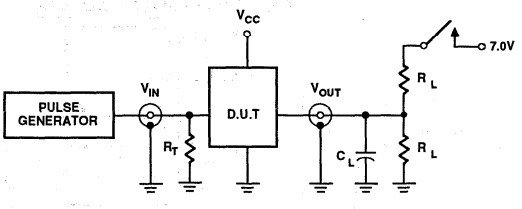
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



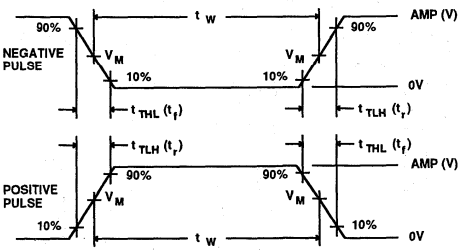
Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0375
ECN No.	98992
Date of issue	March 1, 1990
Status	Product Specification
FAST Products	

FAST 74F545
Transceiver

Octal Bidirectional Transceiver (With 3-State Inputs/Outputs)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F545	4.0ns	87mA

FEATURES

- **High impedance NPN base inputs for reduced loading (70μA in High and Low states) output**
- **Higher drive than 8304**
- **8-bit bidirectional data flow reduces system package count**
- **3-state inputs/outputs for interfacing with bus orientated systems**
- **24 mA and 64mA bus drive capability on A and B ports, respectively**
- **Transmit/Receive and Output Enable simplify control logic**
- **Pin for pin replacement for Intel 8286**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F545N
20-Pin Plastic SOL	N74F545D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	3.5/0.117	70μA/70μA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.067	40μA/40μA
T/$\overline{R}$	Transmit/Receive input	2.0/0.067	40μA/40μA
A_0- A_7	Port A 3-state outputs	150/40	3.0mA/24mA
B_0- B_7	Port B 3-state outputs	750/107	15mA/64mA

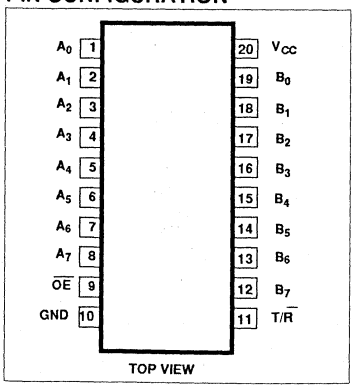
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

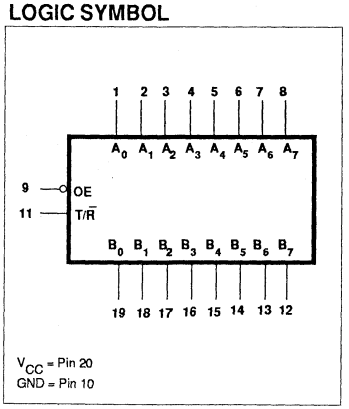
The 74F545 is an 8-bit, 3-state, high speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA bus drive capability on the A ports and 64mA bus drive capbility on the B ports. One input, Transmit/Receive (T/$\overline{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a 3-state condition.

The 74F545 performs the same function as the 74F245, the only difference being package pin assignment.

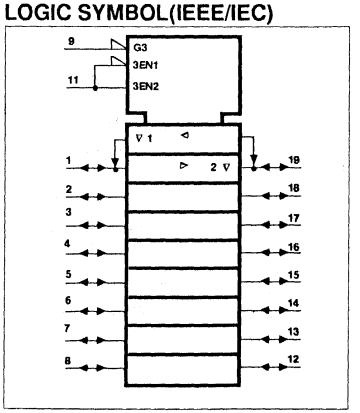
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

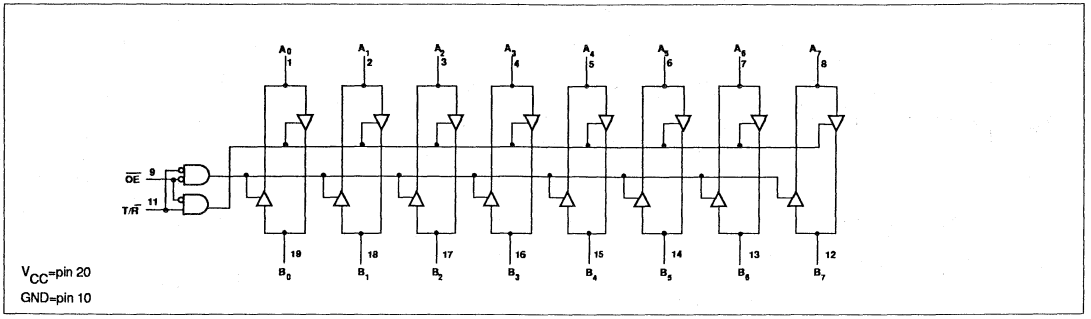


FUNCTION TABLE

INTPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



V_{CC}=pin 20
GND=pin 10

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I =5.5V					1.0	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-40	µA
I_{OZH} +I_{IH}	Off state output current, High-level voltage applied		V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL}+I_{IL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-70	µA
I_{OS}	Short circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	µA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX	T/$\overline{R}$=A_n=4.5V, $\overline{OE}$=GND			84	100	mA
		I_{CCL}		$\overline{OE}$=T/$\overline{R}$=B_n=GND			96	120	mA
		I_{CCZ}		T/$\overline{R}$=B_n=GND, $\overline{OE}$=4.5V			96	120	mA

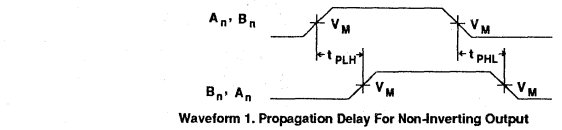
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.

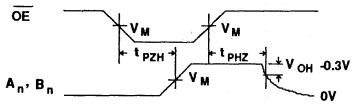
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	1.5 2.5	3.5 4.5	5.5 6.5	1.5 2.5	6.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	6.0 5.5	8.5 8.0	10.5 9.5	6.0 5.5	11.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Level	Waveform 2 Waveform 3	2.5 2.0	5.0 4.5	7.0 6.5	2.5 2.0	8.0 7.5	ns

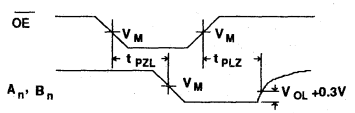
AC WAVEFORMS



Waveform 1. Propagation Delay For Non-Inverting Output



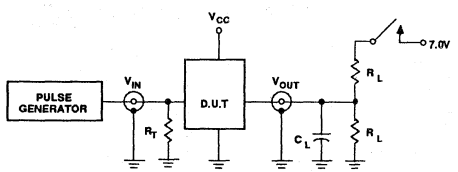
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

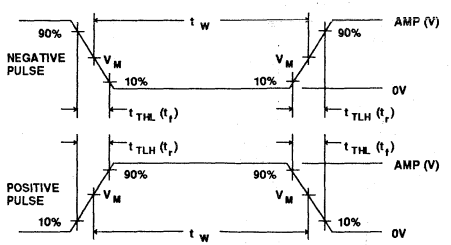
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-1098
ECN No.	01347
Date of issue	January 2, 1991
Status	Product Specification
FAST Products	

FAST 74F552 Transceiver

Octal Registered Transceiver With Parity and Flags (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F552	85MHz	120mA

FEATURES

- **8-Bit bidirectional I/O port with handshake**
- **Register status flag flip-flops**
- **Separate clock enable and output enable**
- **Parity generation and parity check**
- **B outputs and parity output sink 64mA**

DESCRIPTION

The 74F552 Octal Registered Transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock (CPR, CPS) and Clock Enable ($\overline{CER}$, $\overline{CES}$) inputs, as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the Output Enable returns to High after reading the output port. Each register has a separate Output Enable ($\overline{OEAS}$, $\overline{OEBR}$) for its 3-state buffer. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A port to the B port, a parity bit is generated. On the other hand, when data is transferred from the B port to the A port, the parity of input data on B_0-B_7 is checked.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600mil)	N74F552N
28-Pin Plastic SOL[1]	N74F552D

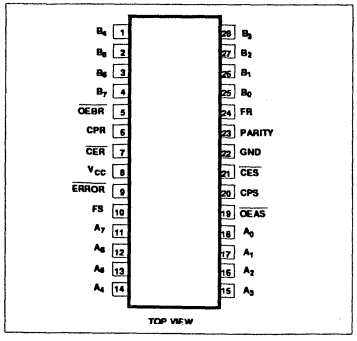
NOTE: Thermal mounting technique are recommended. See AN SMD-100 ProcessApplications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

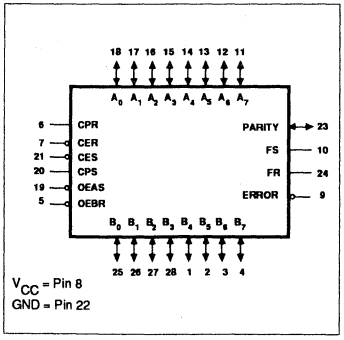
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A Data inputs	3.5/1.0	70µA/0.6mA
B_0 - B_7	B Data inputs	3.5/1.0	70µA/0.6mA
CPR	R registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
CPS	S registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{CER}$	R registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CES}$	S registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OEBR}$	A-to-B Output Enable input (active Low) and clear FS output (active Low)	1.0/2.0	20µA/1.2mA
$\overline{OEAS}$	B-to-A Output Enable input (active Low) and clear FR output (active Low)	1.0/2.0	20µA/1.2mA
PARITY	Parity bit transceiver input	3.5/1.0	70µA/0.6mA
	Parity bit transceiver output	750/106.7	15mA/64mA
$\overline{ERROR}$	Parity check output (active Low)	50/33.3	1.0mA/20mA
A_0 - A_7	A Data outputs	150/40	3.0mA/24mA
B_0 - B_7	B Data outputs	750/106.7	15mA/64mA
FR	A-to-B Status Flag output (active High)	50/33.3	1.0mA/20mA
FS	B-to-A Status Flag output (active High)	50/33.3	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

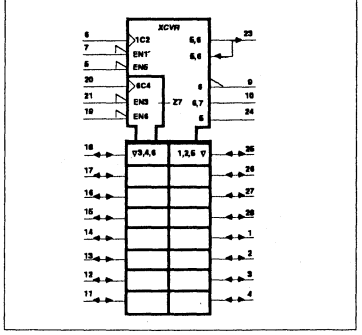
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTIONAL DESCRIPTION

Data applied to the A inputs are entered and stored on the rising edge of the CPR clock pulse, provided that the $\overline{CER}$ is Low; simultaneously, the status flip-flop is set and the A-to-B flag (FR) output goes High. As the $\overline{CER}$ returns to High, the data will be held in R register. This data entered from the A inputs will appear at the B port I/O pins after the $\overline{OEBR}$ has gone Low. When $\overline{OEBR}$ is Low, a parity bit appears at the PARITY pin, which will be set High when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR, by changing the signal at the $\overline{OEBR}$ pin from Low to High. Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A Low at the $\overline{CES}$ pin and a Low-to-High transition at the CPS pin enters the B input data and the parity input data into the S register and the parity register respectively and set the flag output FS to HIgh. A Low signal at the $\overline{OEAS}$ pin enables the A port I/O pins and a Low-to-High transition of the $\overline{OEAS}$ signal clears the FS flag. When $\overline{OEAS}$ is Low, the parity check output $\overline{ERROR}$ will be High if there is an odd number of 1s at the Q outputs of the S registers and the parity register.

R or S REGISTER FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
A_n or B_n	CPX	$\overline{CEX}$	INTERNAL Q	
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	
X	↕	L	NC	Keep old data

H= High voltage level
L= Low voltage level
NC=No change
X=Don't care
X=R or S for CPX and $\overline{CEX}$
↑ =Low-to-High transition
↕ =Not Low-to-High transition

OUTPUT CONTROL TABLE

INPUT	OUTPUTS		OPERATING MODE
$\overline{OEXX}$	INTERNAL Q	A_n or B_n	
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	

H= High voltage level
L= Low voltage level
X=Don't care
XX=AS or BR
Z =High impedance "off" state

R or S FLAG FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{CEX}$	CPX	$\overline{OEXX}$	FR or FS	
H	X	↕	NC	Hold flag
L	↑	↕	H	Set flag
X	X	↑	L	Clear flag

H= High voltage level
L= Low voltage level
NC=No change
X=Don't care
X=R or S for CPX and $\overline{CEX}$
XX=AS or BR
↑ =Low-to-High transition
↕ =Not Low-to-High transition

PARITY GENERATION FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
$\overline{OEBR}$	CPR	Number of Highs in The Q outputs of the R register	PARITY	
H	X	X	Z	Hold data
L	↑	0,2,4,6,8	H	Load data
L	↑	1,3,5,7	L	

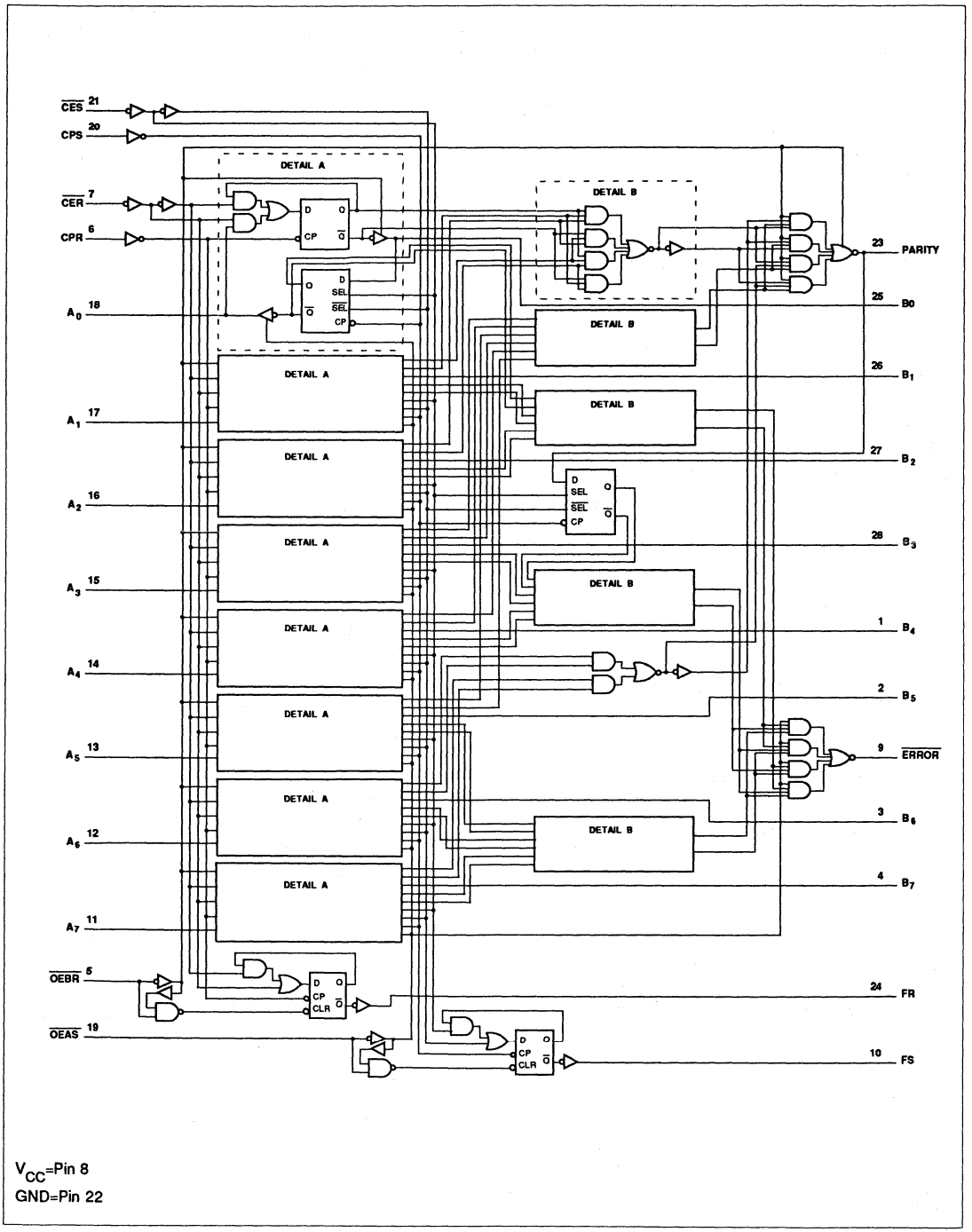
H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state
↑ =Low-to-High transition

PARITY CHECK FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
$\overline{OEAS}$	CPS	PARITY	Number of Highs in The Q outputs of the R register	$\overline{ERROR}$	
H	X	X	X	H	Parity check
L	↑	L	0,2,4,6,8	L	
L	↑	L	1,3,5,7	H	
L	↑	H	0,2,4,6,8	H	
L	↑	H	1,3,5,7	L	

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High transition

LOGIC DIAGRAM



V_{CC}=Pin 8
GND=Pin 22

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to $+V_{CC}$	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	FR, FS, $\overline{ERROR}$	40	mA
		A_0- A_7	48	mA
		B_0- B_7, PARITY	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	FR, FS, $\overline{ERROR}$			-1	mA
		A_0- A_7			-3	mA
		B_0- B_7, PARITY			-15	mA
I_{OL}	Low-level output current	FR, FS, $\overline{ERROR}$			20	mA
		A_0- A_7			24	mA
		B_0- B_7, PARITY			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	FR, FS, $\overline{ERROR}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		A_0- A_7		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0- B_7, PARITY		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	FR, FS, $\overline{ERROR}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=20mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
		A_0- A_7		I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0- B_7, PARITY		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		A_0- A_7, B_0- B_7, PARITY	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	others except A_0- A_7, B_0- B_7, PARITY	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{OEAS}$, $\overline{OEBA}$						-1.2	mA
I_{OZH}+ I_{IH}	Off-state output current, High-level voltage applied	A_0- A_7, B_0- B_7, PARITY	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{OZL}+ I_{IL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	µA
I_{OS}	Short-circuit Output current[3]	A_0-A_7, FS, FR, $\overline{ERROR}$	V_{CC} = MAX			-60		-150	mA
		B_0-B_7, PARITY				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				115	170	mA
		I_{CCL}					125	185	mA
		I_{CCZ}					120	180	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

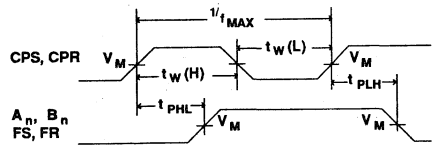
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	Waveform 1	70	85		60		MHz
t_{PLH} t_{PHL}	Propagation delay CPS to A_n or CPR to B_n	Waveform 1	3.5 4.0	5.0 6.0	8.0 9.0	3.0 3.5	8.5 9.0	ns
t_{PLH}	Propagation delay CPS to FS or CPR to FR	Waveform 1	3.0	5.0	7.5	2.5	8.5	ns
t_{PHL}	Propagation delay $\overline{OEAS}$ to FS or $\overline{OEBR}$ to FR	Waveform 2	4.0	6.0	8.5	3.5	9.0	ns
t_{PLH} t_{PHL}	Propagation delay CPS to $\overline{ERROR}$	Waveform 4	6.5 7.5	13.0 11.5	16.5 15.0	6.0 7.0	18.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CPR to PARITY	Waveform 4	6.5 10.5	8.5 13.5	11.0 17.0	5.5 10.0	12.5 18.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEAS}$ to $\overline{ERROR}$	Waveform 3	3.5 3.0	5.5 5.0	8.0 7.0	3.0 2.5	8.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEAS}$ to A_n or $\overline{OEBR}$ to B_n	Waveform 7 Waveform 8	2.5 4.0	4.0 6.5	7.0 9.5	2.0 4.0	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEAS}$ to A_n or $\overline{OEBR}$ to B_n	Waveform 7 Waveform 8	2.0 2.0	4.0 3.5	7.0 7.0	1.5 1.5	8.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBR}$ to PARITY	Waveform 7 Waveform 8	2.0 4.0	4.0 5.5	7.0 8.0	2.0 3.0	7.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disnable time $\overline{OEBR}$ to PARITY	Waveform 7 Waveform 8	2.0 2.0	4.0 4.0	7.0 7.5	2.0 2.0	7.5 8.0	ns

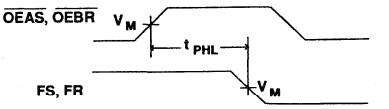
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n or PARITY to CPS or CPR	Waveform 5	7.5 4.5			8.5 5.5		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n or PARITY to CPS or CPR	Waveform 5	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{CES}$ to CPS or $\overline{CER}$ to CPR	Waveform 5	7.0 7.0			7.5 7.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{CES}$ to CPS or $\overline{CER}$ to CPR	Waveform 5	0 0			0 0		ns
t_w(H) t_w(L)	CPS or CPR Pulse width, High or Low	Waveform 1	5.0 6.5			6.5 7.5		ns
t_{REC}	Recovery time $\overline{OEBR}$ to CPR or $\overline{OEAS}$ to CPS	Waveform 6	14.5			16.5		ns

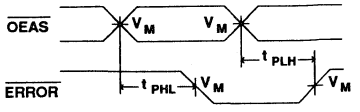
AC WAVEFORMS



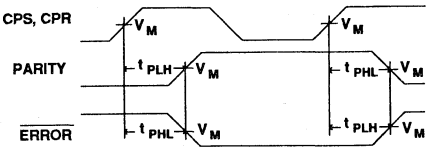
Waveform 1. Propagation Delay, Clock input to output and maximum clock frequency



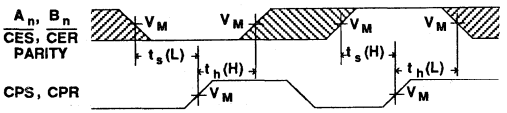
Waveform 2. Propagation Delay, Output Enable to Flag output



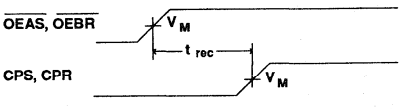
Waveform 3. Propagation Delay, Output Enable to ERROR



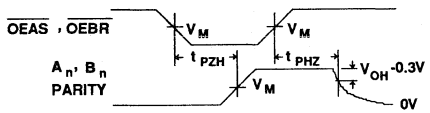
Waveform 4. Propagation Delay, Clock to PARITY and ERROR



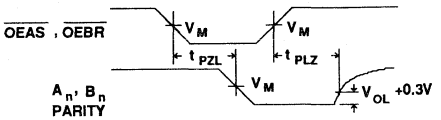
Waveform 5. Data Setup And Hold Times



Waveform 6. Recovery time from Output Enable to Clock



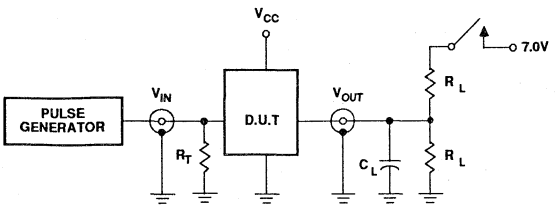
Waveform 7. 3-State Output Enable Time To High Level And Output Disable Time From High Level



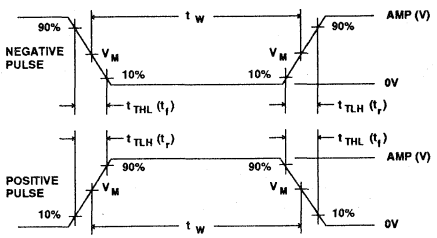
Waveform 8. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0166
ECN No.	98169
Date of issue	November 27, 1989
Status	Product Specification
FAST Products	

FAST 74F563, 74F564
Latch/Flip-Flop

74F563 Octal Transparent Latch (3-State)
74F564 Octal D Flip-Flop (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F563	5.0ns	40mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F564	180MHz	50mA

FEATURES

- **74F563 is broadside pinout version of 74F533**
- **74F564 is broadside pinout version of 74F534**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus interfacing**
- **Common Output Enable**
- **74F573 and 74F574 are non-inverting versions of 74F563 and 74F564 respectively**
- **These are High-Speed replacements for N8TS807 and N8TS808**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F563N, N74F564N
20-Pin Plastic SOL	N74F563D, N74F564D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F563)	Latch Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F564)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{O}_0$-$\overline{O}_7$	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F563 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.
The 74F563 is functionally identical to the 74F533 but has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F564 is functionally identical to the 74F534 but has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's $\overline{Q}$ output.

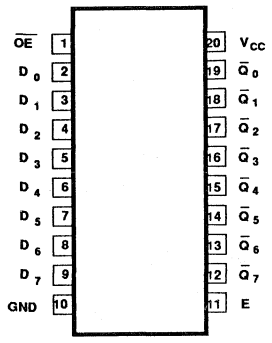
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the register operation. When $\overline{OE}$ is Low, data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

Latch/Flip-Flop

FAST 74F563, 74F564

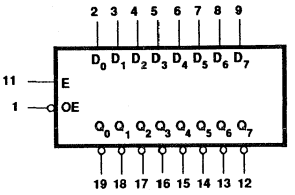
PIN CONFIGURATION

74F563



LOGIC SYMBOL

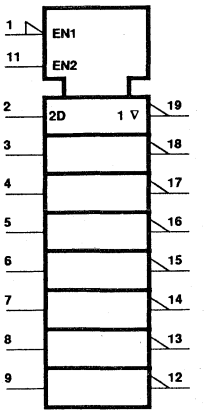
74F563



V_{CC} = Pin 20
GND = Pin 10

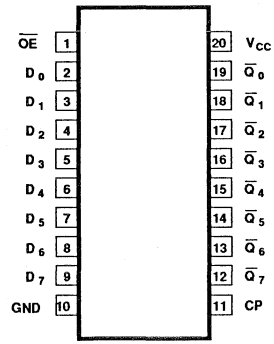
LOGIC SYMBOL(IEEE/IEC)

74F563



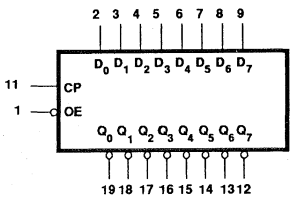
PIN CONFIGURATION

74F564



LOGIC SYMBOL

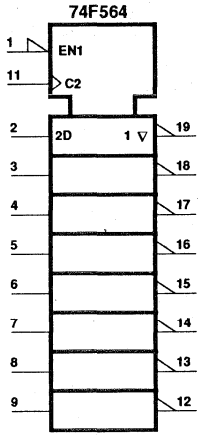
74F564



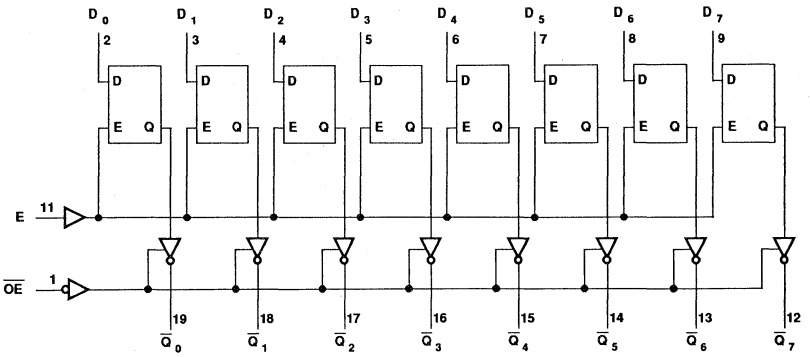
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

74F564

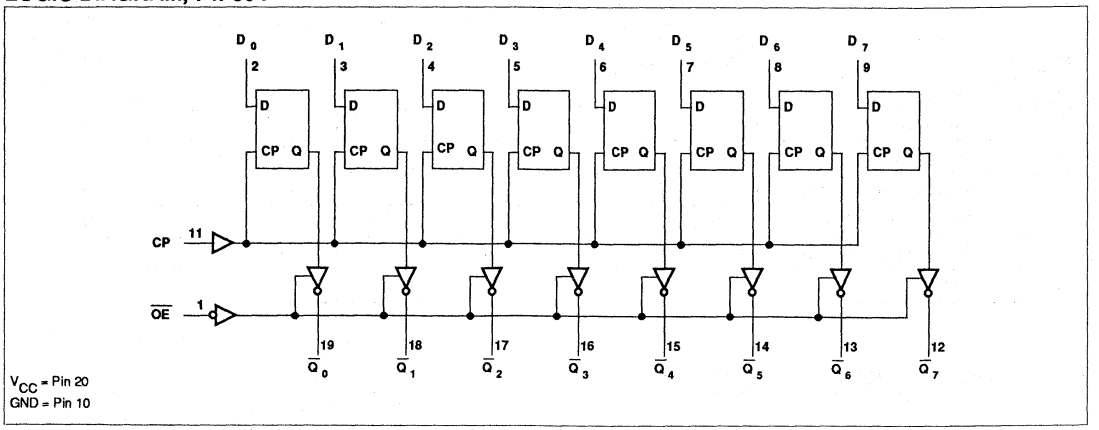


LOGIC DIAGRAM, 74F563



V_{CC} = Pin 20
GND = Pin 10

LOGIC DIAGRAM, 74F564



FUNCTION TABLE, 74F563

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n		$\overline{Q}_0$ - $\overline{Q}_7$	
L	H	L	L	H	Enable and read register
L	H	H	H	L	
L	↓	l	L	H	Latch and read register
L	↓	h	H	L	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	D_n	D_n	Z	

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74F564

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n		$\overline{Q}_0$ - $\overline{Q}_7$	
L	↑	l	L	H	Load and read register
L	↑	h	H	L	
L	↑	X	NC	NC	Hold
H	↑	X	NC	Z	Disable outputs
H	↑	D_n	D_n	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↑ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F563	V_{CC} = MAX			30	45	mA
		I_{CCL}					40	60	mA
		I_{CCZ}					45	65	mA
		I_{CCH}	74F564	V_{CC} = MAX			45	65	mA
		I_{CCL}					50	75	mA
		I_{CCZ}					55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

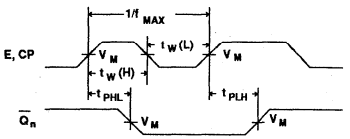
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F563	Waveform 2	4.0 2.5	5.5 4.0	8.5 6.5	3.5 2.0	9.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$		Waveform 1	5.0 3.0	6.5 5.0	9.5 7.0	4.5 3.0	10.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	7.5 8.0	2.5 3.5	8.5 8,5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.5 1.5	3.0 3.0	6.0 5.5	1.0 1.0	7.0 6.0	ns
f_{MAX}	Maximum Clock frequency	74F564	Waveform 1	160	180		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$		Waveform 1	3.5 3.5	5.0 5.0	8.0 8.0	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.5 4.0	4.5 5.5	7.5 8.0	2.0 3.5	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns

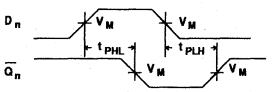
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time D_n to E	74F563	Waveform 3	1.0 1.0			1.0 1.0		ns
t_h(H) t_h(L)	Hold time D_n to E		Waveform 3	3.0 2.5			3.0 2.5		ns
t_w(H)	E Pulse width, High		Waveform 1	3.5			3.5		ns
t_s(H) t_s(L)	Set-up time D_n to CP	74F564	Waveform 3	2.0 2.0			2.0 2.5		ns
t_h(H) t_h(L)	Hold time D_n to CP		Waveform 3	1.0 1.0			1.5 1.5		ns
t_w(H) t_w(L)	CP Pulse width, High or Low		Waveform 1	3.5 3.5			3.5 3.5		ns

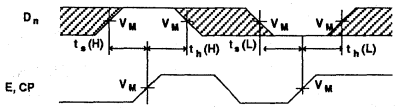
AC WAVEFORMS



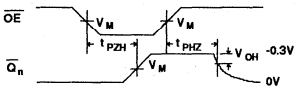
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable, and Clock Pulse Widths, and Maximum Clock Frequency



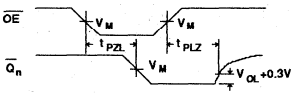
Waveform 2. Propagation Delay For Data To Outputs



Waveform 3. Data Setup And Hold Times



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

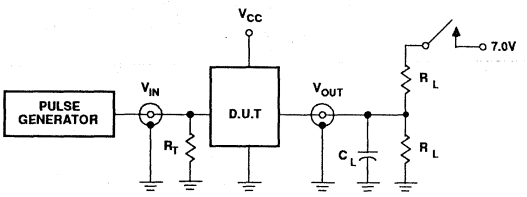


Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

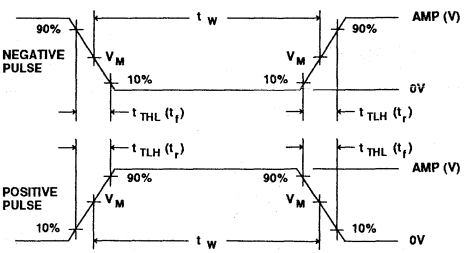
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0376
ECN No.	96252
Date of issue	April 6, 1989
Status	Product Specification
FAST Products	

FAST 74F568, 74F569 Counters

'F568 4-Bit Bidirectional Decade Synchronous Counter (3-state)
'F569 4-Bit Bidirectional Binary Synchronous Counter (3-state)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F568	115MHz	40mA
74F569	115MHz	40mA

FEATURES

- **4-bit bidirectional counting**
  - **'F568 Decade counter**
  - **'F569 Binary counter**
- **Synchronous counting and loading**
- **Look ahead carry capability for easy cascading**
- **Preset capability for programmable operation**
- **Master Reset ($\overline{MR}$) overrides all other inputs**
- **Synchronous Reset ($\overline{SR}$) overrides counting and parallel loading**
- **Clock Carry ($\overline{CC}$) output to be used as a clock for flip-flops, register and counters**
- **3-state outputs for bus organized systems**

DESCRIPTION

The 74F568 and 74F569 are fully synchronous Up/Down Counters. The 74F568 is a BCD decade counter; the 74F569 is a binary counter. They feature preset capability for programmable operation, carry look ahead for easy cascading, and U/$\overline{D}$ input to control the direction of counting. For maximum flexibility

ORDERING INFORMATION

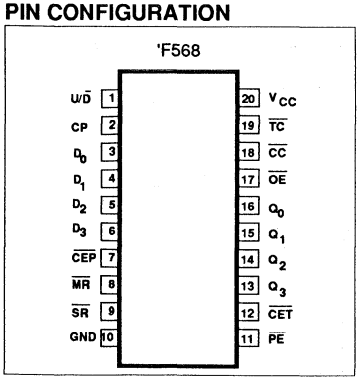
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic Dip	N74F568N, N74F569N
20-Pin Plastic Dip	N74F568D, N74F569D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

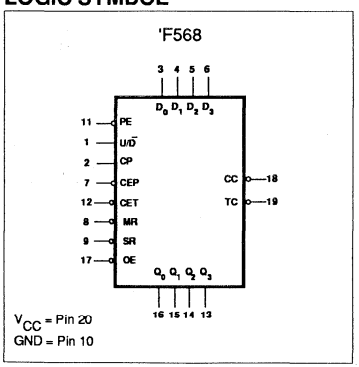
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/2.0	20µA/1.2mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset (active Low)	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA
$\overline{CC}$	Clocked Carry output (active Low)	50/33	1.0mA/20mA
Q_0 -Q_3	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

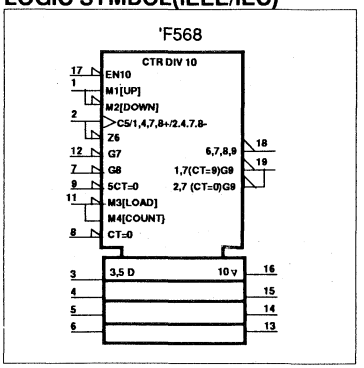
PIN CONFIGURATION



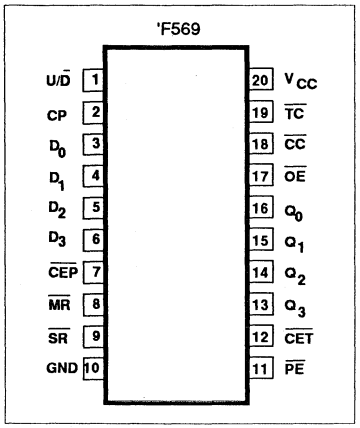
LOGIC SYMBOL



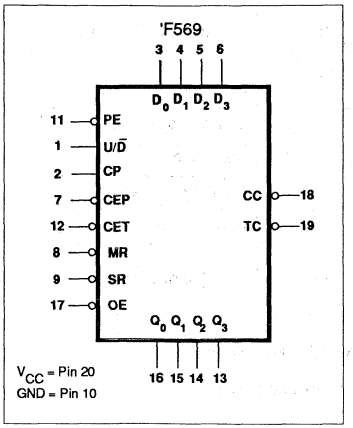
LOGIC SYMBOL(IEEE/IEC)



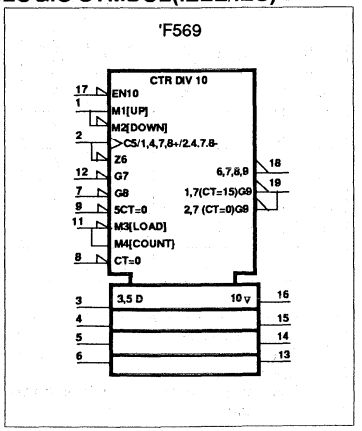
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

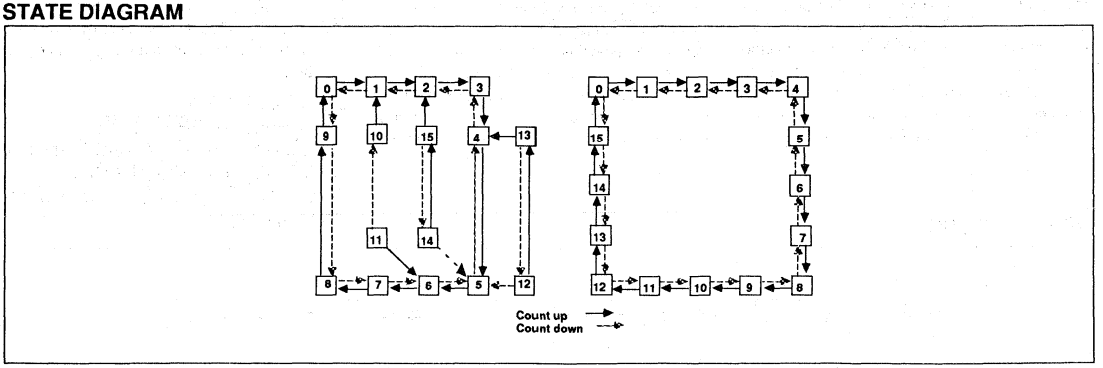


there are both Synchronous and Master Reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by rising edge of the clock. A High signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

FUNCTIONAL DESCRIPTION

The 74F568 counts modulo-10 in the BCD(8421) sequence. From state 0 (LLLL) it increments to 9 (HLLH) in the up mode; in the down mode it will decrement 9 to 0. The 74F569 counts in the modulo-16 binary sequence. From state 0 (LLLL) it will increment to 15 in the up mode; in the down mode it will decrement from 15 to 0. The clock inupts of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the Low-to-High transition of the Clock Pulse(CP) input

STATE DIAGRAM



The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Six control inputs-Master Reset ($\overline{MR}$) Synchronous Reset ($\overline{SR}$), Count Enable Trickle ($\overline{CET}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$), and the Up/Down(U/$\overline{D}$) input determine the mode of operation, as shown in the Function Table.

A Low signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs Low. A Low signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q output to go Low on the next rising edge of CP. A Low signal on $\overline{PE}$ overrides counting and allows information on the parallel data (D_n) inputs to be loaded into the flipflops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$, and $\overline{PE}$ High, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are Low. Conversely, a High signal on either $\overline{CEP}$ and $\overline{CET}$ inhibits counting. The 'F568 and 'F569 use edge triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or U/$\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed. Two types of outputs are provided as overflow/underflow indicators. The Terminal Count($\overline{TC}$) output is normally High and goes Low provided $\overline{CET}$ is Low, when the counter reaches zero in the down mode, or reaches maximum (9 for 'F568 and 15 for 'F569) in the up mode.

$\overline{TC}$ will then remain Low until a state change

FUNCTION TABLE

INPUTS							OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	CP	
L	X	X	X	X	X	X	Asynchronous reset
h	I	X	X	X	X	↑	Synchronous reset
h	h	I	X	X	X	↑	Parallel load
h	h	h	I	I	h	↑	Count up (increment)
h	h	h	I	I	I	↑	Count down (decrement)
h	H	H	H	X	X	X	Hold (do nothing)
h	H	H	X	H	X	X	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
I = Low voltage level one setup prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

occurs, whether by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed.

To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure 1 shows the connections for a simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry look ahead connections in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the up mode, or min to max in the down mode, to start its final cycle. Since this takes 10 ('F568) or 16 ('F569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, register or counters.

For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ ouTput is normally High. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are Low, the $\overline{CC}$ output will go Low, when the clock next goes Low and will stay Low until the clock goes High again; as shown in the $\overline{CC}$ Function Table. When the Output Enable ($\overline{OE}$) is Low, the parallel data outputs Q_0 - Q_3 are active and follow the flip-flop Q outputs. A High signal on $\overline{OE}$ forces Q_0 - Q_3 to the High impedance state but does not prevent counting, loading or resetting.

LOGIC EQUATIONS:

Count Enable=$\overline{CEP}$•$\overline{CET}$•$\overline{PE}$

Up: $\overline{TC}$= Q_0•$\overline{Q}_1$•$\overline{Q}_2$•Q_3•(Up)•$\overline{CET}$ for 'F568

Up: $\overline{TC}$= Q_0•Q_1•Q_2•Q_3•(Up)•$\overline{CET}$ for 'F569

Down: $\overline{TC}$= $\overline{Q}_0$•$\overline{Q}_1$•$\overline{Q}_2$•$\overline{Q}_3$•(Down)•$\overline{CET}$ for 'F568 and 'F569

APPLICATIONS

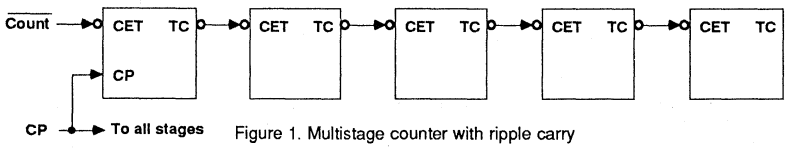


Figure 1. Multistage counter with ripple carry

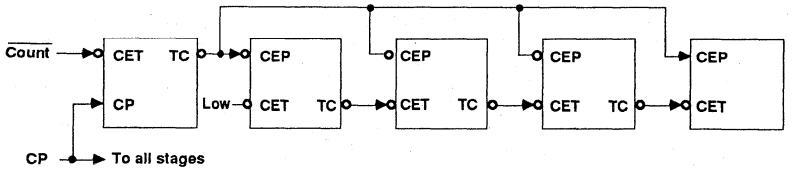


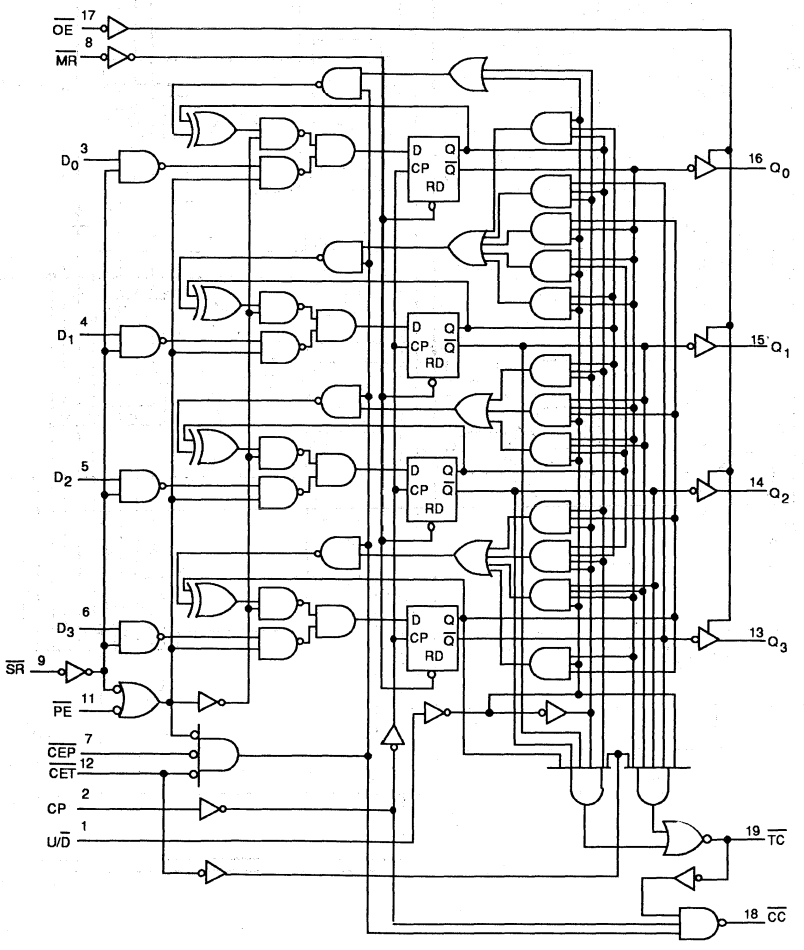
Figure 2. Multistage counter with look ahead carry

$\overline{CC}$ FUNCTION TABLE

INPUTS						OUTPUT
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊓	⊓

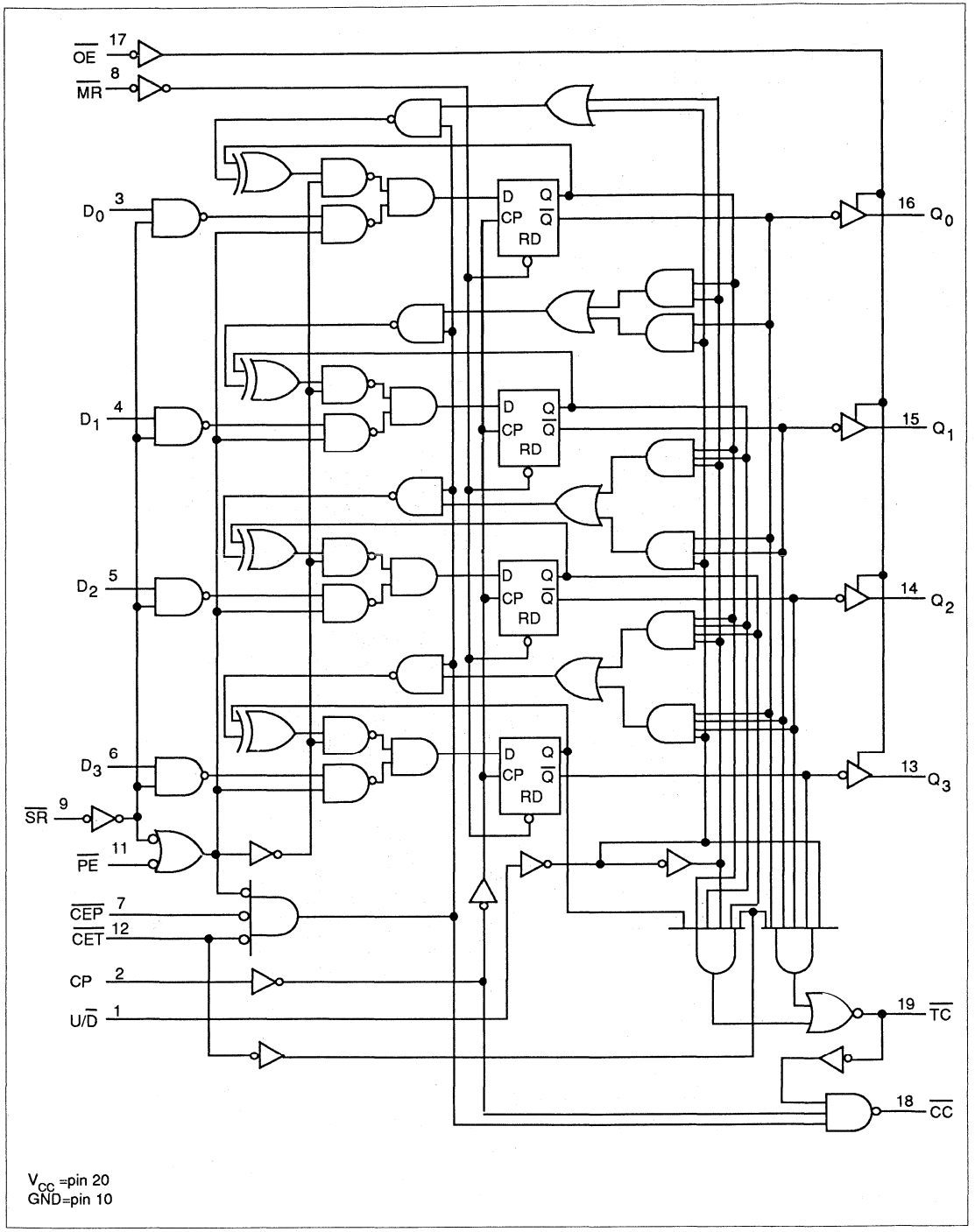
* = $\overline{TC}$ is generated internally
H = High voltage level
L = Low voltage level
X = Don't care
⊓ = Low pulse

LOGIC DIAGRAM for 'F568



V_{CC} = pin 20
GND= pin 10

LOGIC DIAGRAM for 'F569



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$, $\overline{CC}$	40	mA
		Q_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$, $\overline{CC}$			-1	mA
		Q_n			-3	mA
I_{OL}	Low-level output current	$\overline{TC}$, $\overline{CC}$			20	mA
		Q_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CET}$, $\overline{PE}$					-1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			38	60	mA
		I_{CCL}				43	62	mA
		I_{CCZ}				40	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

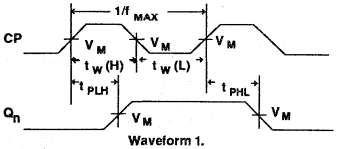
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Q_n	Waveorm 1	100	115		90		MHz
		$\overline{CC}$, $\overline{TC}$	Waveform 2	50	65		45		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, High or Low)		Waveform 1	3.0 4.0	6.0 7.5	9.5 11.0	3.0 4.0	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		Waveform 2	5.5 4.0	10.0 7.5	15.0 11.0	5.5 4.0	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$		Waveform 3	1.5 2.5	3.0 5.0	6.0 8.0	1.0 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F568	Waveform 4	2.5 5.0	5.0 10.0	9.0 15.0	2.0 5.0	10.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F569	Waveform 4	4.0 4.0	7.5 6.5	11.0 11.0	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{CC}$		Waveform 2	2.5 2.0	4.5 4.0	7.5 6.5	2.0 2.0	6.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CEP}$, $\overline{CET}$ to $\overline{CC}$		Waveform 2	2.0 3.5	4.0 5.5	7.0 9.0	1.5 3.0	7.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n		Waveform 5	6.0	8.0	11.0	5.5	12.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{CC}$		Waveform 4	4.5 5.0	9.0 11.0	12.0 16.0	4.0 5.0	13.5 17.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{TC}$, $\overline{CC}$		Waveform 5	8.0	11.0	15.0	7.5	16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SR}$ to $\overline{CC}$		Waveform 3	5.5 7.5	8.0 9.5	11.0 12.0	5.0 7.0	12.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PE}$ to $\overline{CC}$		Waveform 3	3.0 4.0	5.0 6.0	8.0 8.5	2.5 4.0	8.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{OE}$ to Q_n		Waveform 10 Waveform 11	2.0 4.5	4.0 6.5	7.0 9.5	2.0 4.0	7.5 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level $\overline{OE}$ to Q_n		Waveform 10 Waveform 11	1.5 1.5	3.5 3.5	6.5 6.0	1.5 1.5	7.5 6.5	ns

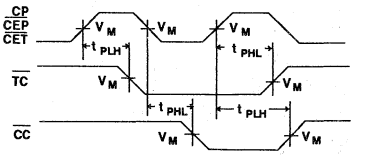
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 6	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 6	2.0 2.0			2.5 2.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 7	5.0 5.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 7	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP		Waveform 6	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP		Waveform 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F568	Waveform 8	11.0 16.5			12.5 17.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F569	Waveform 8	10.0 8.0			12.5 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP		Waveform 8	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SR}$ to CP		Waveform 9	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SR}$ to CP		Waveform 9	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	7.0 5.0			8.0 6.0		ns
$t_w(H)$	$\overline{MR}$ Pulse width, Low		Waveform 5	4.5			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP		Waveform 5	6.0			7.0		ns

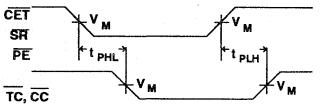
AC WAVEFORMS



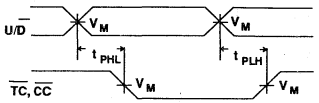
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



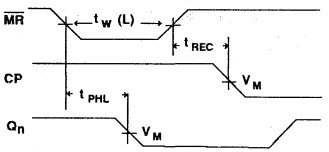
Waveform 2.
Propagation Delay, CP, CET, and $\overline{CEP}$ to $\overline{CC}$ and CP to $\overline{TC}$



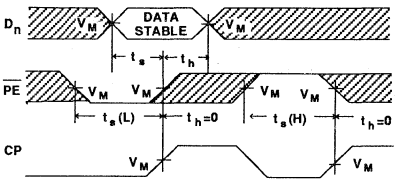
Waveform 3.
Propagation Delay, $\overline{CET}$ to $\overline{TC}$ and $\overline{SR}$ or $\overline{PE}$ to $\overline{CC}$



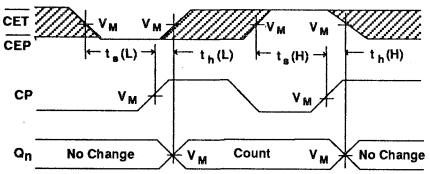
Waveform 4.
Propagation Delay, U/D to $\overline{TC}$ and $\overline{CC}$



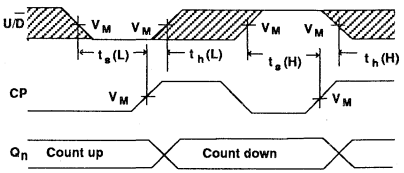
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



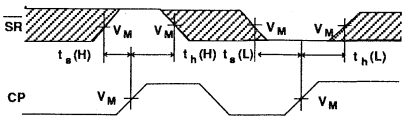
Waveform 6.
Data Parallel Data And Parallel Enable Setup And Hold Times



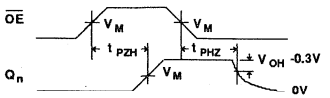
Waveform 7.
Count Enable Data Setup And Hold Times



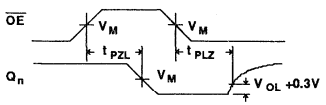
Waveform 8.
Up/Down Control Setup And Hold Times



Waveform 9. Synchronous Reset Setup And Hold Times



Waveform 10. 3-State Output Enable Time To High Level And Output Disable Time From High Level

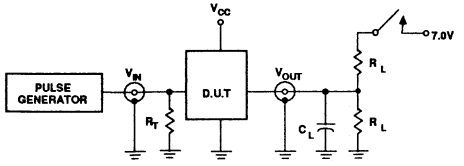


Waveform 11. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

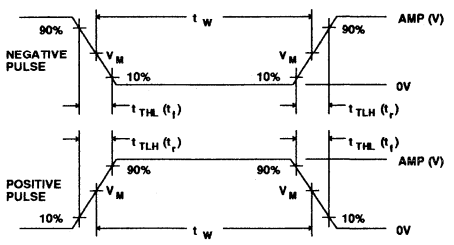
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0083
ECN No.	97897
Date of issue	October 16, 1989
Status	Product Specification
FAST Products	

FAST 74F573, 74F574 Latch/Flip-Flop

74F573 Octal Transparent Latch (3-State)
74F574 Octal D Flip-Flop (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F573	5.0ns	35mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F574	180MHz	50mA

FEATURES

- **74F573 is broadside pinout version of 74F373**
- **74F574 is broadside pinout version of 74F374**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus interfacing**
- **Common Output Enable**
- **74F563 and 74F564 are inverting version of 74F573 and 74F574 respectively**
- **3-State Outputs glitch free during power-up and power-down**
- **These are High-Speed replacements for N8TS805 and N8TS806**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F573N, N74F574N
20-Pin Plastic SOL	N74F573D, N74F574D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F573)	Latch enable input (active falling edge)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F574)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F573 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.
The 74F573 is functionally identical to the 74F373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

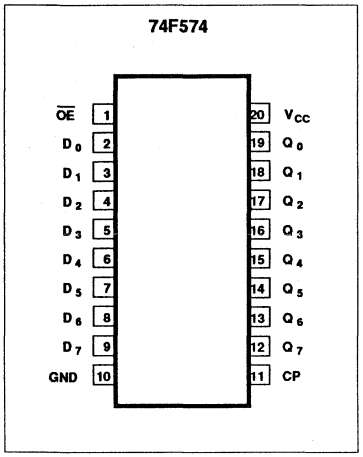
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F574 is functionally identical to the 74F374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

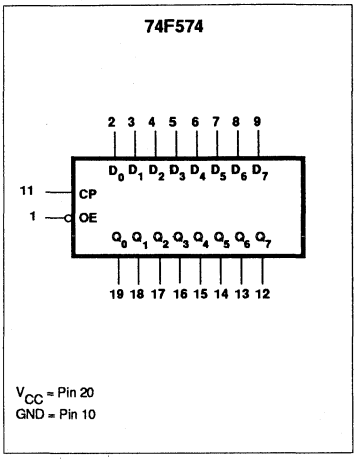
It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

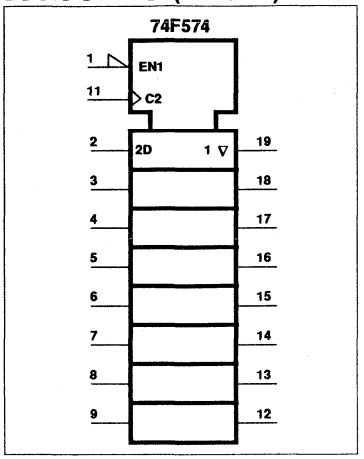
PIN CONFIGURATION



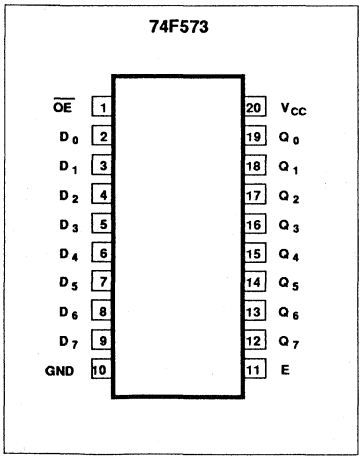
LOGIC SYMBOL



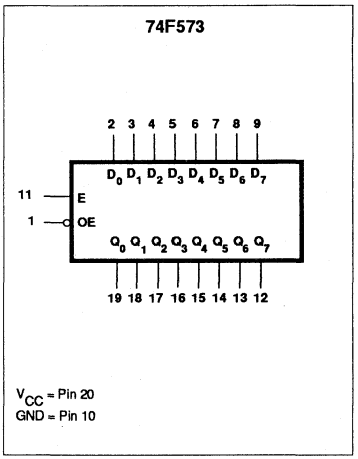
LOGIC SYMBOL(IEEE/IEC)



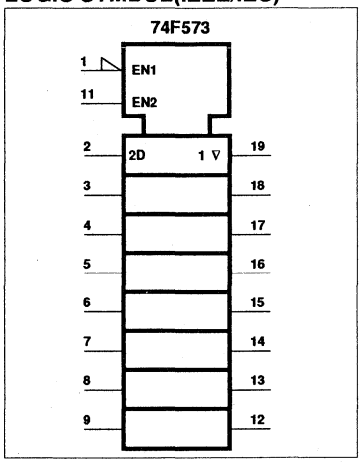
PIN CONFIGURATION



LOGIC SYMBOL



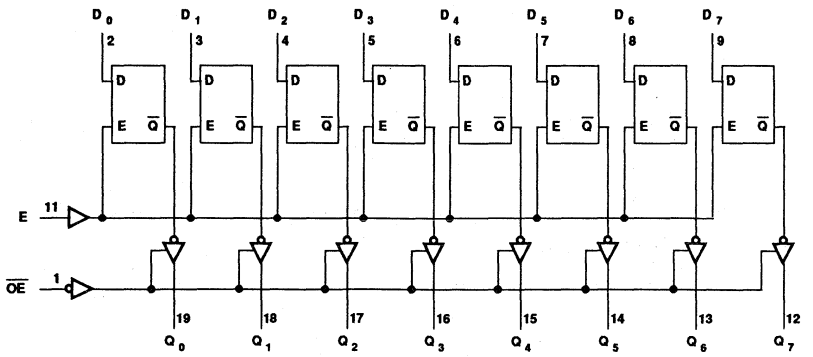
LOGIC SYMBOL(IEEE/IEC)



October 16, 1989

853-0083-97897

LOGIC DIAGRAM, 74F573



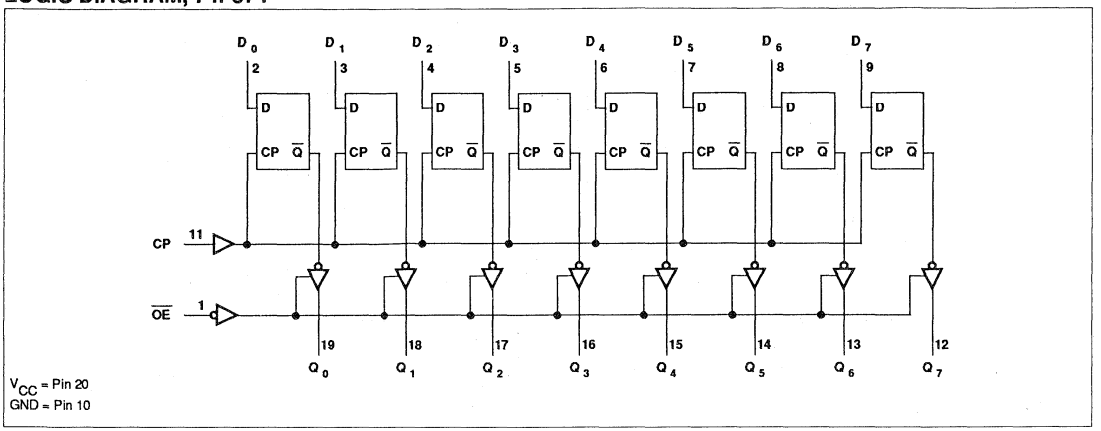
V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE, 74F573

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	Q_0 - Q_7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	D_n	D_n	Z	

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM, 74F574



FUNCTION TABLE, 74F574

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↑	X	NC	NC	Hold
H	↑	D_n	D_n	Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F573	V_{CC} = MAX			30	40	mA
		I_{CCL}					35	50	mA
		I_{CCZ}					40	60	mA
		I_{CCH}	74F574	V_{CC} = MAX			45	65	mA
		I_{CCL}					50	70	mA
		I_{CCZ}					55	85	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

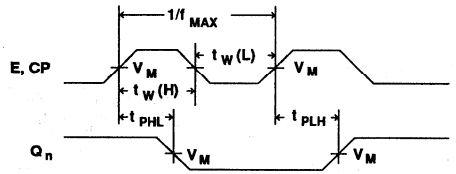
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F573	Waveform 2	3.0 1.0	5.5 3.5	8.0 6.0	2.5 1.0	9.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 1	4.5 3.0	8.5 5.0	11.5 7.0	4.0 2.5	12.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 5 Waveform 6	2.5 2.5	5.5 5.5	9.5 8.0	2.0 2.0	10.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 5 Waveform 6	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	6.5 5.5	ns
f_{MAX}	Maximum Clock frequency	74F574	Waveform 1	160	180		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 5 Waveform 6	2.5 3.0	4.5 5.0	7.5 8.0	2.0 3.0	7.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 5 Waveform 6	1.0 1.0	3.0 2.5	5.5 5.5	1.0 1.0	6.0 6.0	ns

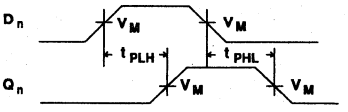
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time D_n to E	74F573	Waveform 4	0.0 1.5			0.0 2.0		ns
t_h(H) t_h(L)	Hold time D_n to E		Waveform 4	2.5 4.0			2.5 4.0		ns
t_w(H)	E Pulse width, High		Waveform 1	3.0			3.5		ns
t_s(H) t_s(L)	Set-up time D_n to CP	74F574	Waveform 3	2.5 2.5			3.0 3.0		ns
t_h(H) t_h(L)	Hold time D_n to CP		Waveform 3	0 0			0 0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low		Waveform 1	3.0 3.5			3.0 4.0		ns

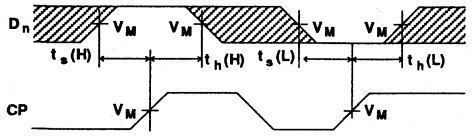
AC WAVEFORMS



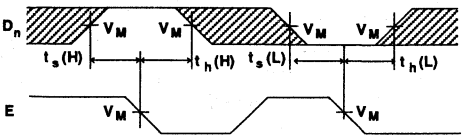
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable, and Clock Pulse Widths, and Maximum Clock Frequency



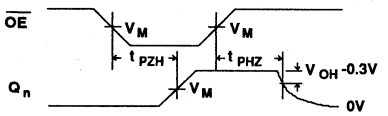
Waveform 2. Propagation Delay For Data To Outputs



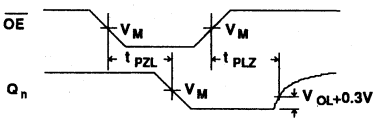
Waveform 3. Data Setup And Hold Times



Waveform 4. Data Setup And Hold Times



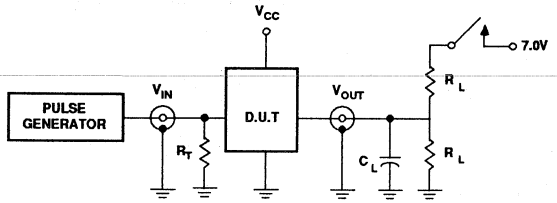
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



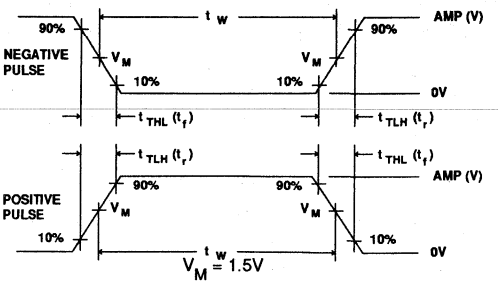
Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Components-Signetics

Document No.	853-0377
ECN No.	06639
Date of issue	May 4, 1992
Status	Product Specification
FAST Products	

FAST 74F579 Counter

8-Bit Bidirectional Binary Counter (3-state)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100mA

FEATURES

- **Fully synchronous operation**
- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built in cascading carry capability**
- **U/$\overline{D}$ pin to control direction of counting**
- **Separate pins for Master Reset and Synchronous operation**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 115MHz typ**
- **Supply current 100mA typ**
- **See 'F269 for 24 pin separate I/O port version**
- **See 'F779 for 16 pin version**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic Dip	N74F579N
20-Pin Plastic SOL	N74F579D

DESCRIPTION

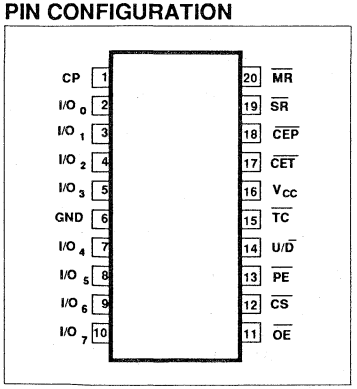
The 74F579 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-state I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

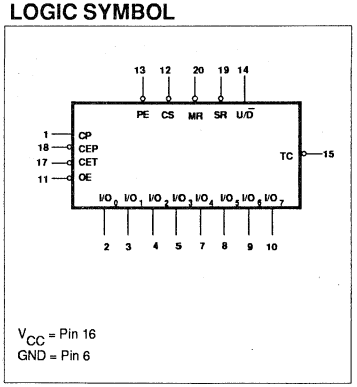
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70µA/0.6mA
	Data outputs	150/40	3.0mA/24mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

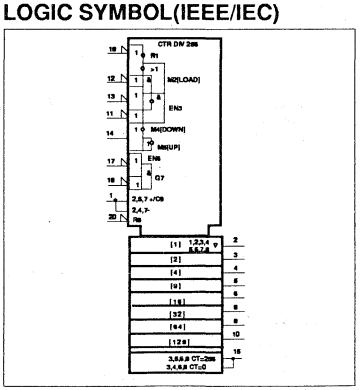
PIN CONFIGURATION



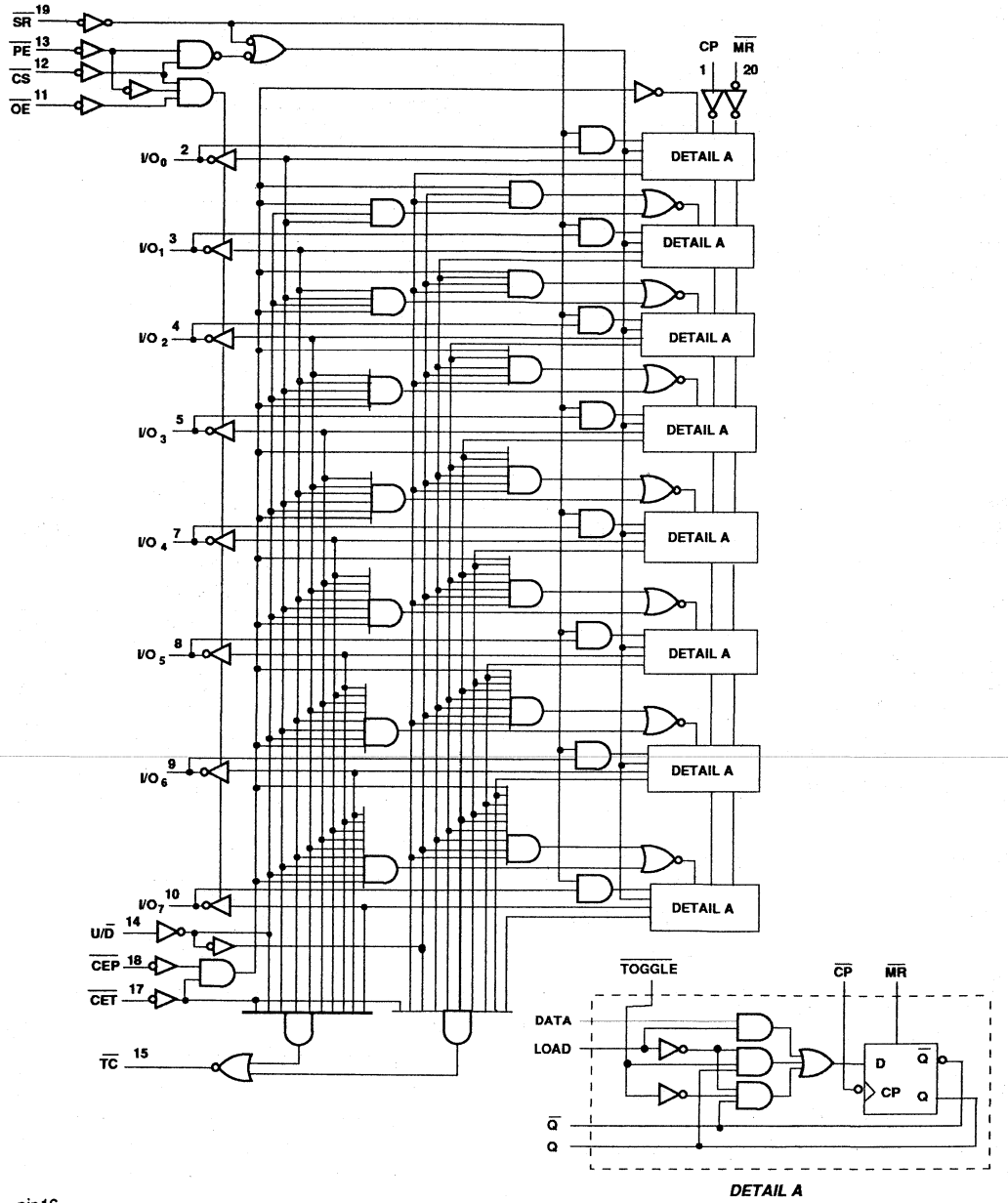
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} =pin16
GND=pin 6

FUNCTION TABLE

INPUTS									OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	CP	
X	X	H	X	X	X	X	X	X	I/O_0 to I/O_7 in high impedance ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O_0 to I/O_7 in high impedance
X	X	L	H	X	X	X	L	X	Flip-flop output appears on I/O_n lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held High)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = $\overline{CS}$ and $\overline{PE}$ should never be Low voltage level at the same time..

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O_0	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN (V_{IL}=0.0V, V_{IH}=4.5V for $\overline{MR}$,CP inputs)	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4	3.3		V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = MAX, V_I = 5.5V					1	mA
		others	V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
$I_{OZH}+I_{IH}$	Off state output current, High-level voltage applied	I/O_n	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{OZL}+I_{IL}$	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				95	135	mA
		I_{CCL}					105	145	mA
		I_{CCZ}					105	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

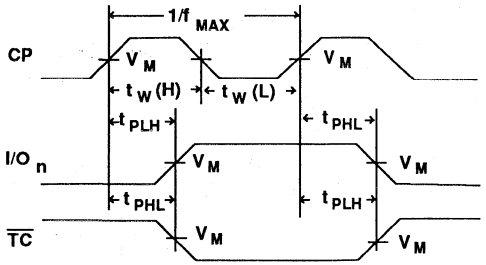
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	4.5 5.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 4	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 3	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	8.5 8.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	7.0	9.0	5.0	10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{TC}$	Waveform 4	4.0 6.0	6.5 8.0	9.0 10.5	4.0 6.0	10.5 12.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	4.0 5.5	5.0 7.0	8.5 10.5	3.5 5.0	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	5.0 7.5	7.5 9.5	3.0 4.5	9.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	4.5 6.5	8.0 10.0	3.0 4.5	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 2.5	4.0 4.0	7.5 7.5	3.0 2.0	9.0 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	2.5 4.5	4.0 5.5	7.0 9.0	2.5 4.0	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	1.0 2.0	2.5 4.0	4.0 7.0	1.0 2.0	5.5 8.0	ns

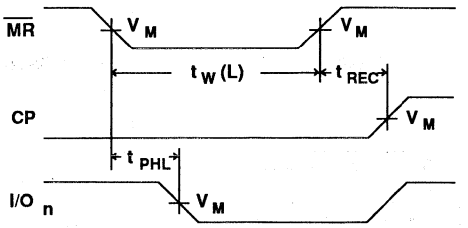
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $U/\overline{D}$ to CP	Waveform 5	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $U/\overline{D}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	9.5 9.5			10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 9.0			5.5 10.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.5 4.5			4.5 4.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

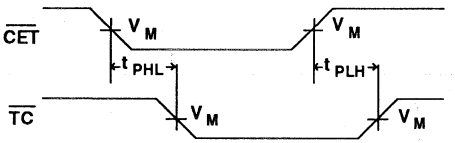
AC WAVEFORMS



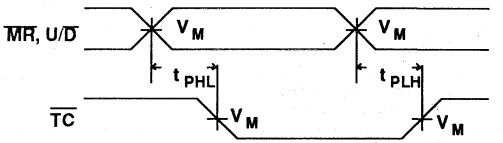
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



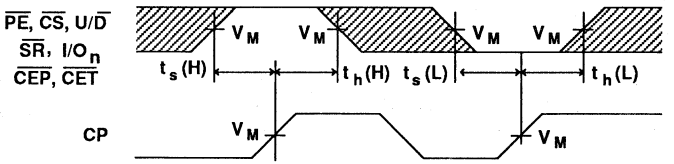
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



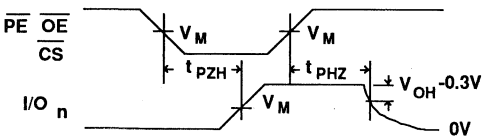
Waveform 3.
Propagation Delay, CET input to Terminal Count Output



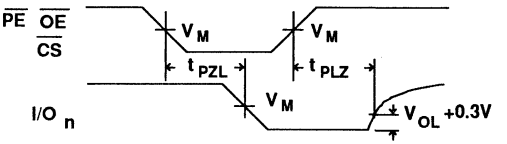
Waveform 4. Propagation Delay, U/D and MR inputs to Terminal Count Output



Waveform 5. Setup And Hold Times



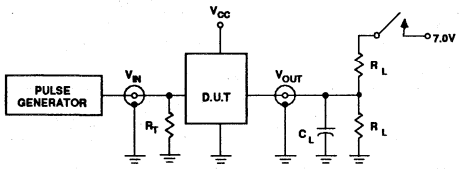
Waveform 6. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 7. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

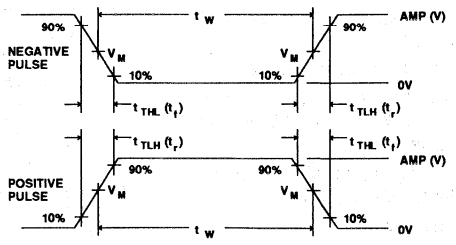
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-1096
ECN No.	99392
Date of issue	April 18, 1990
Status	Product Specification
FAST Products	

FAST 74F595
Shift Register

8-Bit Shift Register with Output Latches (3-state)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F595	130MHz	65mA

FEATURES

- **Low noise, no switching feedthru current**
- **Controlled output edge rates**
- **High impedance PNP base inputs for reduced loading (20µA in High and Low states)**
- **8-bit serial-in, parallel-out shift register with storage**
- **3-state outputs**
- **Shift register has direct clear**
- **Guaranteed shift frequency-DC to 100MHz**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F595N
16-Pin Plastic SO	N74F595D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_S	Serial data input	1.0/0.033	20µA/20µA
SHCP	Shift register clock pulse input (active rising edge)	1.0/0.033	20µA/20µA
STCP	Storage register clock pulse input (active rising edge)	1.0/0.033	20µA/20µA
$\overline{SHR}$	Shift register reset input (active Low)	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input (active Low)	1.0/0.033	20µA/20µA
Q_S	Serial expansion output	50/33	1.0mA/20mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

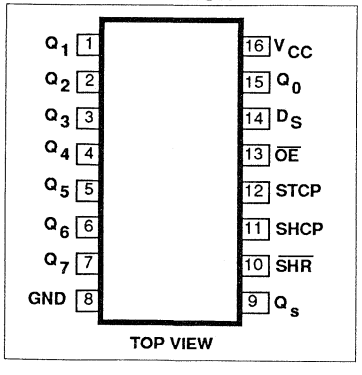
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

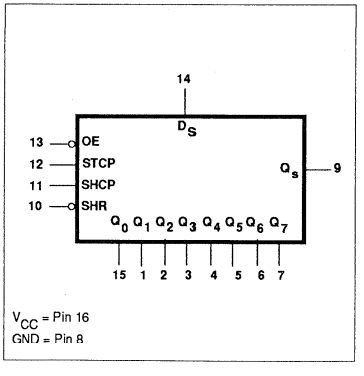
The 74F595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct overriding clear, serial input and serial output pins for cascading. Both the shift register and storage register clocks are positive edge-triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

This device uses patented circuitry to control system noise and internal ground bounce. This is done by eliminating switching feedthru current and controlling both Low-to-High and High-to-Low slew rates.

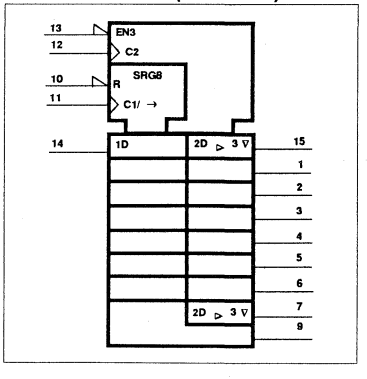
PIN CONFIGURATION



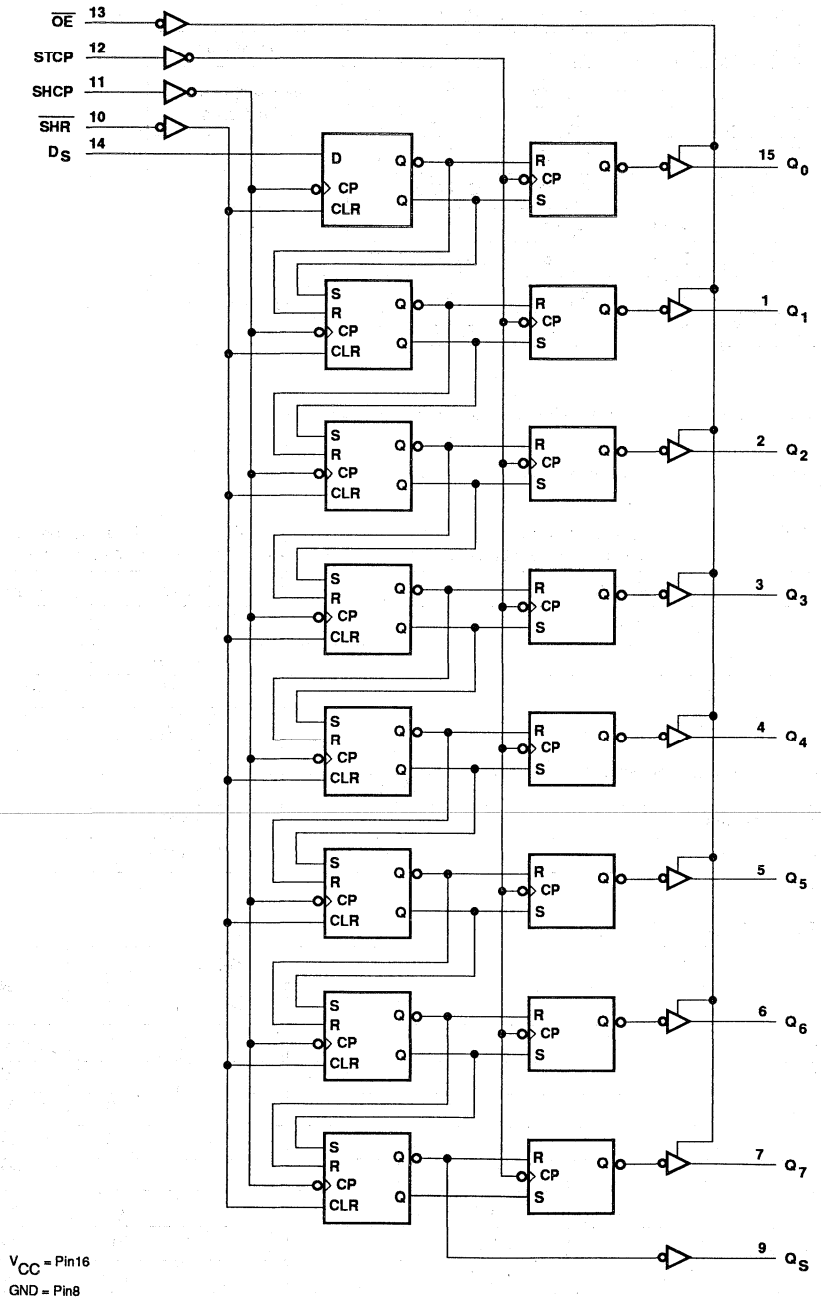
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT - FUNCTION TABLE

INPUTS					INTERNAL SHIFT REGISTERS		INTERNAL STORAGE REGISTER	OUTPUTS		OPERATING MODE
$\overline{OE}$	$\overline{SHR}$	SHCP	STCP	D_S	O_0	$O_1 - O_7$	$Q_0 - Q_7$	$Q_0 - Q_7$	Q_S	
H	H	↕	↕	X	O_0	$O_1 - O_7$	$Q_0 - Q_7$	Z	Q_7	No change
H	L	X	↕	X	L_0	L	$Q_0 - Q_7$	Z	L	Clear shift register, hold latch
L	L	X	↕	X	L_0	L	$Q_0 - Q_7$	$Q_0 - Q_7$	L	
H	H	↑	↕	d_s	D_s	$o_0 - o_6$	$Q_0 - Q_7$	Z	o_6	Shift
L	H	↑	↕	d_s	D_s	$o_0 - o_6$	$Q_0 - Q_7$	$Q_0 - Q_7$	o_6	
H	H	↕	↑	X	O_0	$O_1 - O_7$	$o_0 - o_7$	Z	Q_7	Store
L	H	↕	↑	X	O_0	$O_1 - O_7$	$o_0 - o_7$	$o_0 - o_7$	Q_7	
H	H	↑	↑	d_s	D_s	$o_0 - o_6$	$o_0 - o_7$*	Z	o_6	Store, then shift
L	H	↑	↑	d_s	D_s	$o_0 - o_6$	$o_0 - o_7$*	$o_0 - o$*	o_6	

H = High voltage level.
L = Low voltage level.
X = Don't care.
Z = High impedance.
$d_n(o_n)$ = Lower case letters indicate the state of the referenced input (or output) one set up time prior to the Low -to-High clock transition.
↑ = Low-to-High clock transition.
↕ = Not a Low-to-High clock transition.
*= When clocking both SHCP and STCP simultaneously the Shift Register state will always be one clock pulse ahead of the Storage Register.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Q_S	40	mA
		$Q_0 - Q_7$	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_S			-1	mA
		$Q_0 - Q_7$			-3	mA
I_{OL}	Low-level output current	Q_S			20	mA
		$Q_0 - Q_7$			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		Q_0- Q_7		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=20mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
		Q_0- Q_7		I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	mA
I_{OZH}	Off state output current, High-level voltage applied	Q_0- Q_7 only	V_{CC} =MAX, V_O=2.7V					50	µA
I_{OZL}	Off state output current, Low-level voltage applied	Q_0- Q_7 only	V_{CC} =MAX, V_O=0.5V					-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	80	mA
		I_{CCL}					70	100	mA
		I_{CCZ}					65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

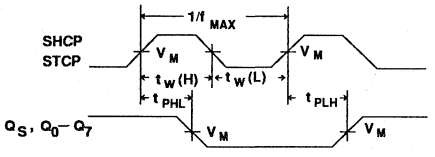
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	SHCP to Q_S	Waveform 1	115	135		90		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S		Waveform 1	6.0 2.5	8.0 4.5	10.5 7.5	5.0 2.5	12.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_0 - Q_7		Waveform 1	5.5 3.0	8.0 5.0	10.0 8.0	4.5 3.0	13.0 8.5	ns
t_{PHL}	Propagation delay $\overline{SHR}$ to Q_S		Waveform 2	3.5	5.5	8.0	3.0	8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_0 - Q_7		Waveform 5 Waveform 6	3.5 3.0	5.5 5.5	9.0 8.5	2.5 2.5	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ or Q_0 - Q_7		Waveform 5 Waveform 6	2.0 4.0	4.0 6.0	7.0 9.0	1.5 3.0	8.5 10.0	ns

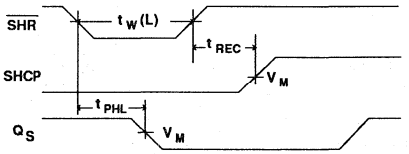
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_S to SHCP	Waveform 3	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_S to SHCP	Waveform 3	0 0			0 0		ns
$t_s(L)$	Setup time, Low $\overline{SHR}$ to STCP	Waveform 3	4.5			5.0		ns
$t_s(H)$	Setup time, High SHCP to STCP	Waveform 4	4.5			5.0		ns
$t_w(H)$ $t_w(L)$	SHCP Pulse width, High or Low	Waveform 1	3.5 4.0			4.0 4.0		ns
$t_w(H)$ $t_w(L)$	STCP Pulse width, High or Low	Waveform 1	4.0 3.0			4.0 3.5		ns
$t_w(L)$	$\overline{SHR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{REC}	Recovery time, $\overline{SHR}$ to SHCP	Waveform 2	3.0			3.0		ns

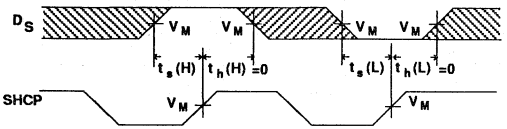
AC WAVEFORMS



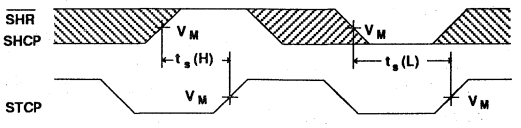
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



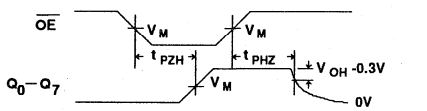
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



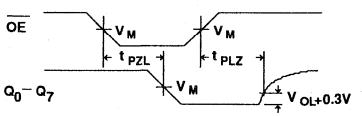
Waveform 3. Data Setup And Hold Times



Waveform 4. Setup And Hold Times



Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level

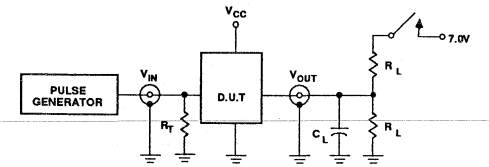


Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

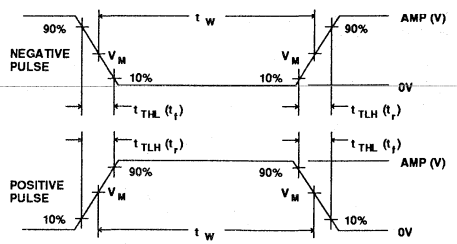
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

8-Bit shift register with input storage registers

74F597

FEATURES

- High impedance PNP base input for reduced loading (20μA in High and Low states)
- 8–bit parallel storage register
- 3–State output buffers
- Shift register has asynchronous direct overriding reset
- Shift load $\overline{SHLD}$ is functional when SHCP is Low and locked out when SHCP is High
- Guaranteed shift frequency DC to 105MHz

DESCRIPTION

The 74F597 consists of an 8–bit storage register feeding a parallel–in/serial–in, serial–out 8–bit shift register. The storage register and shift register have separate positive edge triggered clocks. The shift register has asynchronous reset and when SHCP is Low, it has asynchronous load.

The shift register load function has been modified to load when both $\overline{SHLD}$ and SHCP are Low. When SHCP is High the shift register load operation is not performed. Data will be properly shifted on the rising edge of SHCP when $\overline{SHLD}$ is High.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F597	135MHz	42mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16–pin plastic DIP	N74F597N
16–pin plastic SO	N74F597D

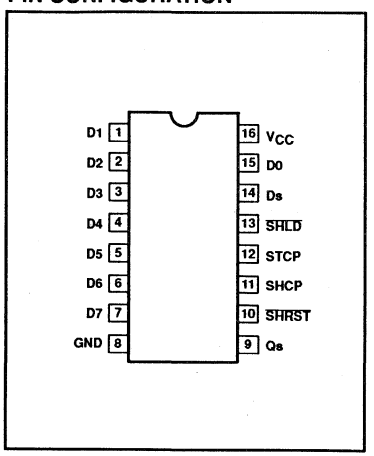
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) High/Low	LOAD VALUE High/Low
Ds	Serial data input	1.0/0.033	20μA/20μA
D0 – D7	Parallel data inputs	1.0/0.033	20μA/20μA
SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
STCP	Storage register clock pulse input	1.0/0.033	20μA/20μA
$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20μA/20μA
$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
Qs	Serial data output	50/33	1.0mA/20mA

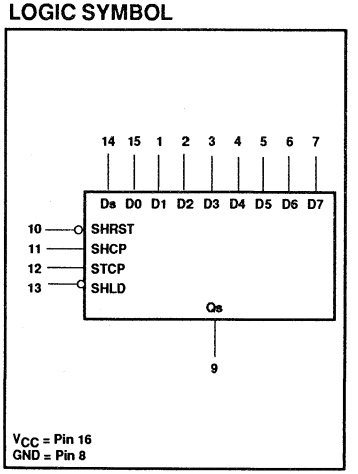
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

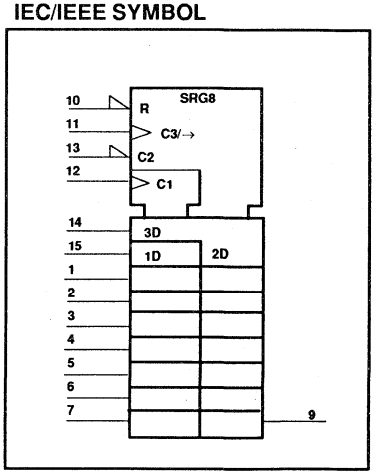
PIN CONFIGURATION



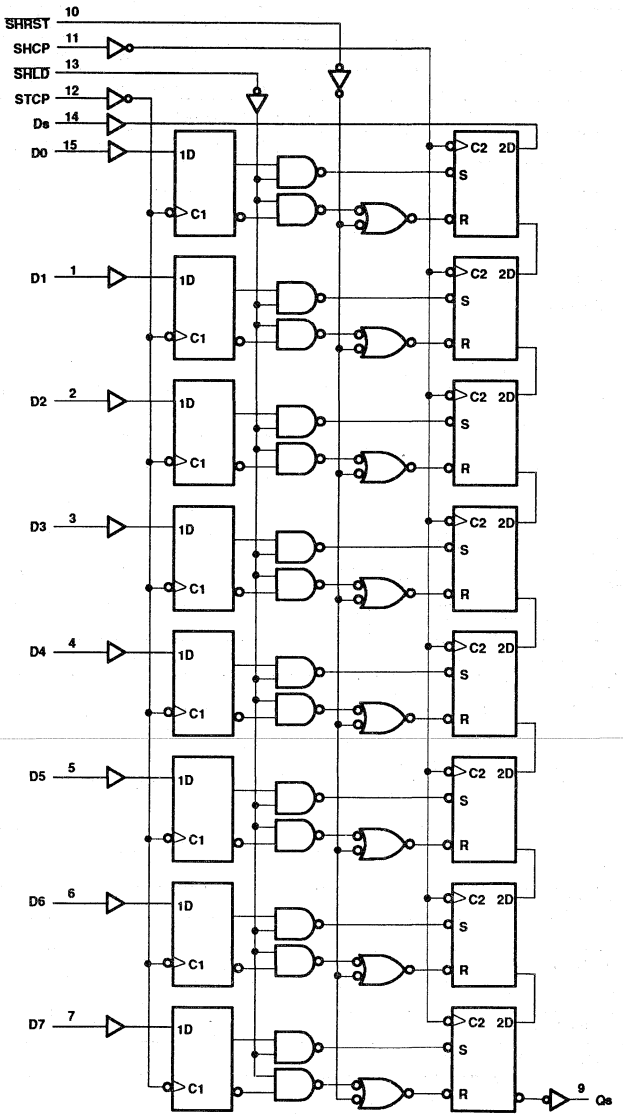
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS				OPERATING MODE
STCP	SHCP	$\overline{SHLD}$	$\overline{SHRST}$	
↑	X	X	X	Data loaded to storage registers
↑	L	L	H	Data loaded from inputs to shift register
↕	L	L	H	Data transferred from storage registers to shift registers
X	L	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	↑	H	H	Shift register clocked, Qn = Qn–1, Q0 = Ds
↕	H	X	H	Hold

Notes to function table
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. ↑ = Low–to–High clock transition
5. ↕ = Not Low–to–High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = –1mA	±10%V_{CC}	2.5			V
			V_{IL} = MAX		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,		±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				43	65	mA
		I_{CCL}					41	60	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

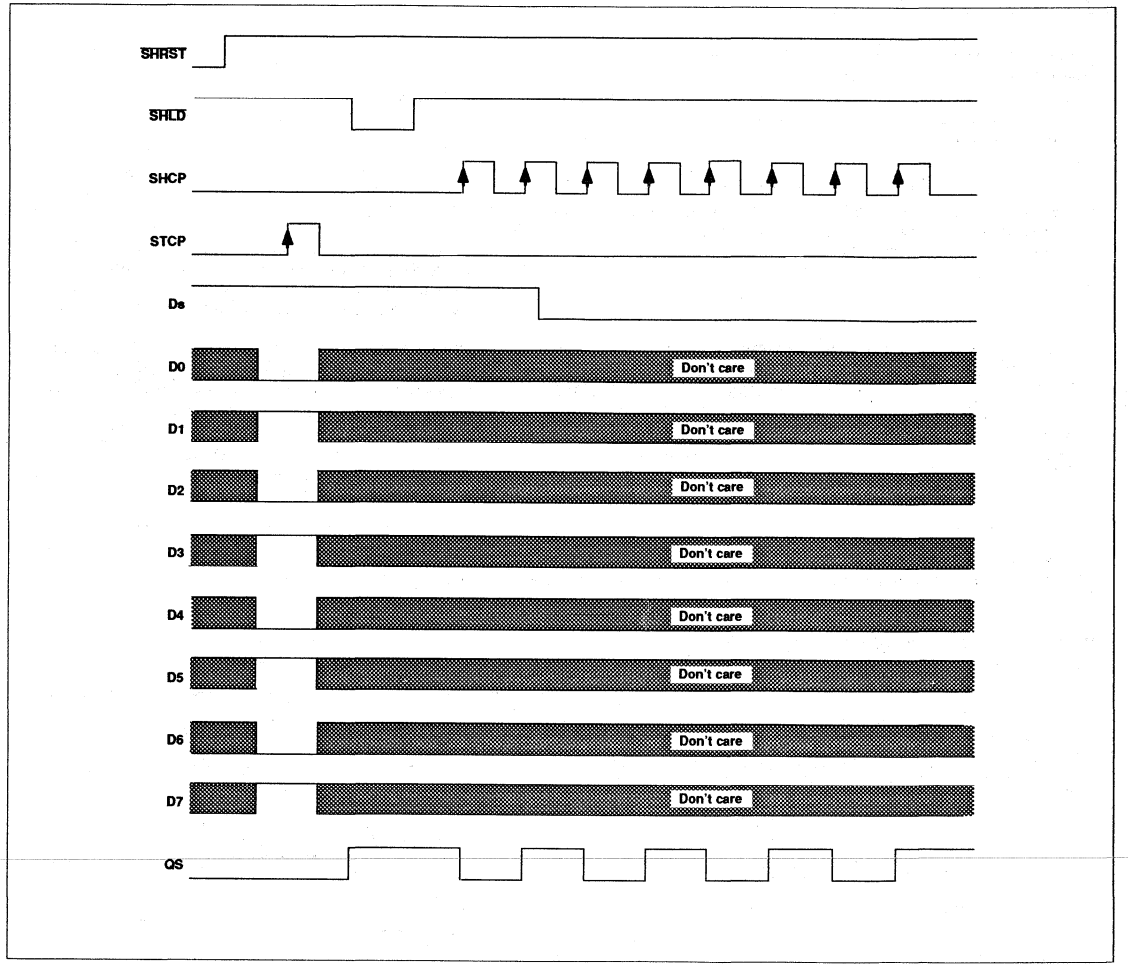
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
f_{max}	Maximum clock frequency	Waveform 1	120	135		105		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Qs	Waveform 1	7.0 6.0	8.5 7.5	11.0 10.0	6.0 5.5	12.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay SHLD to Qs	Waveform 1	8.0 6.0	9.5 7.5	12.0 10.0	7.0 5.5	13.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Qs	Waveform 1	7.5 8.0	9.5 9.5	11.5 12.0	6.5 7.5	13.0 13.0	ns
t_{PHL}	Propagation delay $\overline{SHRST}$ to Qs	Waveform 2	2.5	5.5	9.0	2.5	9.5	ns

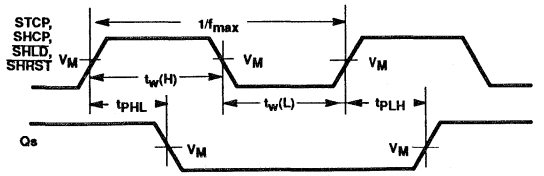
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s (H) t_s (L)	Setup time, High or Low Dn to STCP	Waveform 3	1.0 1.5			1.5 2.0		ns
t_h (H) t_h (L)	Hold time, High or Low Dn to STCP	Waveform 3	2.0 2.0			2.0 3.0		ns
t_s (H) t_s (L)	Setup time, High or Low Ds to SHCP	Waveform 3	1.0 1.5			1.0 2.0		ns
t_h (H) t_h (L)	Hold time, High or Low Ds to SHCP	Waveform 3	1.5 2.0			2.0 2.5		ns
t_s (H)	Setup time, High STCP to $\overline{SHLD}$↑	Waveform 4	8.5			9.0		ns
t_h (L)	Hold time, Low STCP to $\overline{SHLD}$↑ (hold mode)	Waveform 3	0.0			0.0		ns
t_s (H)	Setup time, High $\overline{SHLD}$ to SHCP↑	Waveform 3	6.0			6.5		ns
t_w (H) t_w (L)	SHCP Pulse width, High or Low	Waveform 1	4.5 4.5			5.5 4.5		ns
t_w (H) t_w (L)	STCP Pulse width, High or Low	Waveform 1	4.5 4.5			5.0 4.5		ns
t_w (L)	$\overline{SHRST}$ Pulse width, Low	Waveform 1	4.5			4.5		ns
t_w (L)	$\overline{SHLD}$ Pulse width, Low	Waveform 1	4.5			4.5		ns
t_{rec}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	2.0			2.5		ns

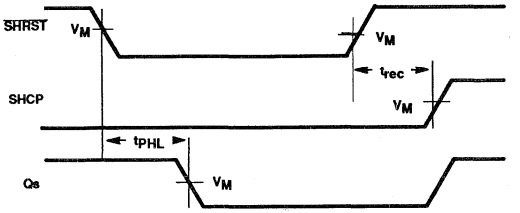
TYPICAL TIMING DIAGRAM



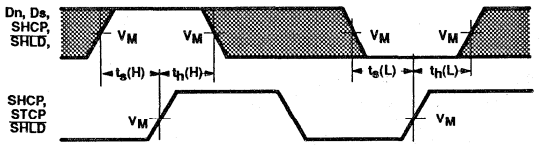
AC WAVEFORMS



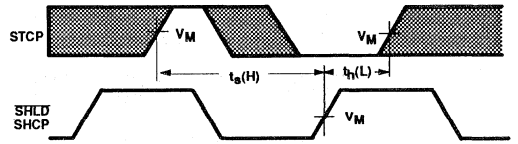
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency, shift register reset and load inputs to serial data output



Waveform 2. Propagatio0n delay for shift register reset and load inputs to serial data output, shift register reset ans load inputs to shift register clock pulse input recovery time



Waveform 3. Setup time and hold times

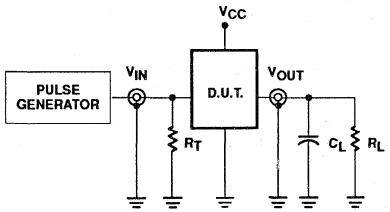


Waveform 4. Setup and hold time

Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



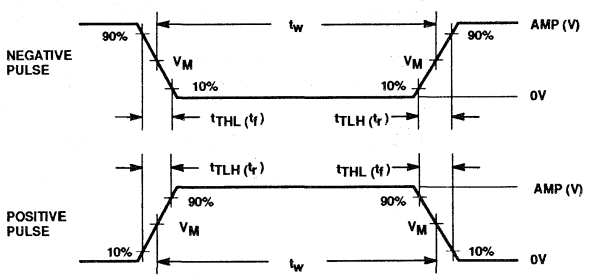
Test circuit for totem-pole outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

8-Bit shift register with input storage registers (3-State) 74F598

FEATURES

- High impedance PNP base input for reduced loading (20mA in High and Low states)
- 8–bit parallel storage register
- Shift register has asynchronous direct overriding reset
- Shift load $\overline{SHLD}$ is functional when SHCP is Low and locked out when SHCP is High.
- Guaranteed shift frequency DC to 105MHz
- Parallel 3–State I/O storage register inputs and shift register parallel outputs

DESCRIPTION

The 74F598 consists of an 8–bit storage register feeding a parallel–in/serial–in, parallel–out/serial–out 8–bit shift register. Both the storage register and shift register have positive edge–triggered clocks. The shift register has asynchronous reset and when SHCP is Low, it has asynchronous load.

The shift register load function has been modified to load when both $\overline{SHLD}$ and SHCP are Low. When SHCP is High the shift register load operation is not performed. Data will be properly shifted on the rising edge of SHCP when $\overline{SHLD}$ is High.

TYPE	TYPICAL SHCP f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F598	100MHz	75mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20–pin plastic DIP	N74F598N
20–pin plastic SOL	N74F598D

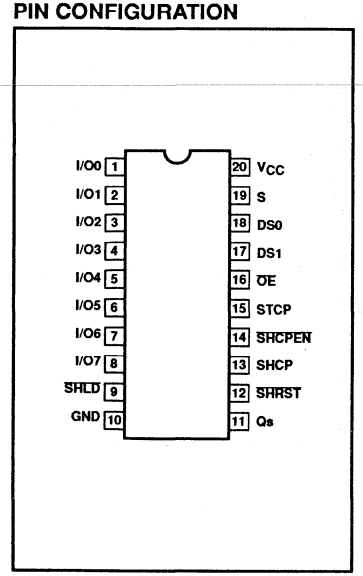
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) High/Low	LOAD VALUE High/Low
I/On	Parallel data input	1.0/0.033	20µA/20µA
Ds0, Ds1	Serial data inputs	1.0/0.033	20µA/20µA
SHCP	Shift register clock pulse input	1.0/0.033	20µA/20µA
STCP	Storage register clock pulse input	1.0/0.033	20µA/20µA
$\overline{SHCPEN}$	Shift register clock pulse enable input	1.0/0.033	20µA/20µA
$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20µA/20µA
$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20µA/20µA
S	Serial data select input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input	1.0/0.033	20µA/20µA
Qs	Serial data output	50/33	1.0mA/20mA
I/On	Parallel data outputs	150/40	3.0mA/24mA

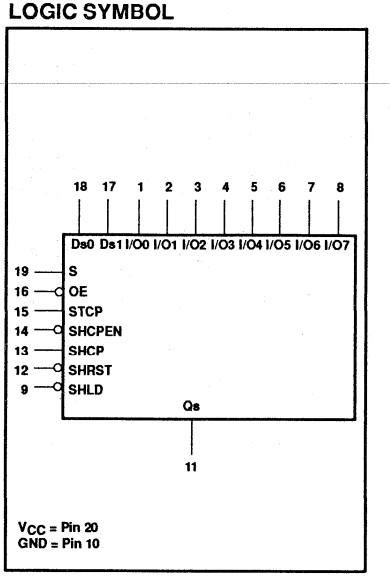
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

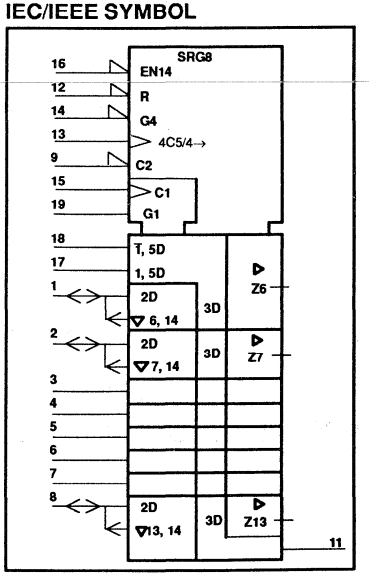
PIN CONFIGURATION



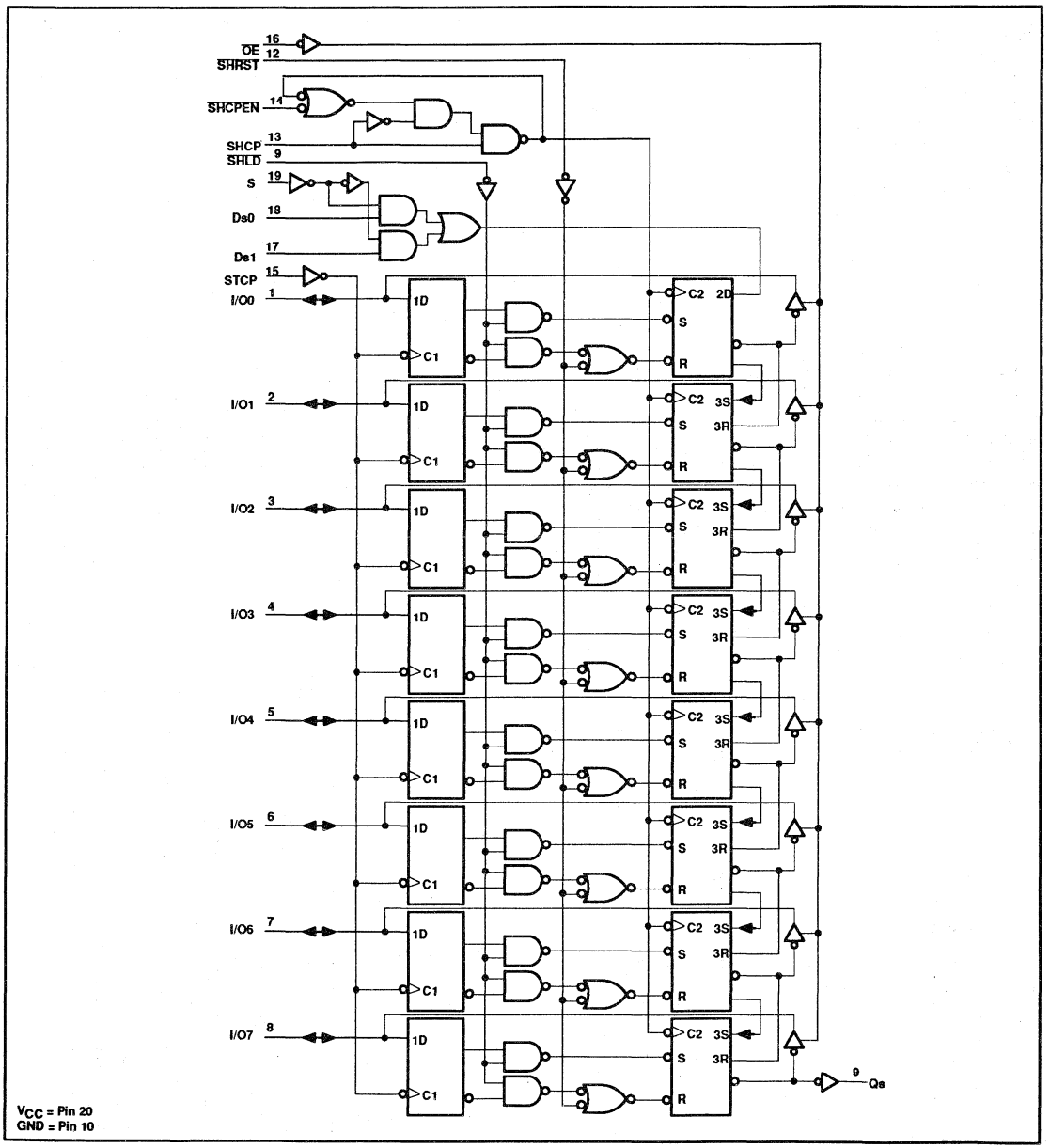
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



8-Bit shift register with input storage registers (3-State) 74F598

FUNCTION TABLE

INPUTS						INPUTS/OUTPUTS									OPERATING MODE
$\overline{SHRST}$	STCP	SHCP	$\overline{SHLD}$	S	$\overline{OE}$*	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	Q7	
L	X	L	H	X	L	L	L	L	L	L	L	L	L	L	Clear shift register
L	X	L	L	X	L										Invalid, state of shift register indeterminate when signal is removed
X	↑	X	X	X	H	I0	I1	I2	I3	I4	I5	I6	I7	O7	Load data to storage register
H	X	↑	H	L	L	Ds0	O0	O1	O2	O3	O4	O5	O6	O6	Shift right
H	X	↑	H	H	L	Ds1	O0	O1	O2	O3	O4	O5	O6	O6	
H	↑	L	L	X	H	I0	I1	I2	I3	I4	I5	I6	I7	O7	Load data directly to shift register
H	↕	L	L	X	X	O0	O1	O2	O3	O4	O5	O6	O7	O7	Data transferred from storage register to shift register
X	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	NC	3–State
H	↕	X	H	X	X	NC	NC	NC	NC	NC	NC	NC	NC	NC	Hold
H	↕	H	X	X	X	NC	NC	NC	NC	NC	NC	NC	NC	NC	Hold (no storage or shift register load

Notes to function table

D0 – D7 = The level of the steady state inputs to the serial multiplexer.
H = High voltage level
I0 – I7 = The level of the steady state input at the respective I/O terminal is loaded into the flip–flop while the flip–flop outputs (except Q7) are isolated from the I/O terminal.
L = Low voltage level
NC= No change
O0 – O7 = The level of the respective Qn flip–flop prior to the last clock Low–to–High transition
X = Don't care
Z = High impedance "off" state
* = When the $\overline{OE}$ input is High, all I/O terminals are at the High impedance state, sequential operation or cleaning of the register is not affected.
↑ = Low–to–High clock transition
↕ = Not Low–to–High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Qs	40	mA
		I/O0 – I/O7	48	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	Qs			–1	mA
		I/O0 – I/O7			–3	mA
I_{OL}	Low–level output current	Qs			20	mA
		I/O0 – I/O7			24	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	Qs	V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/On	V_{IH} = MIN,	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,		±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		I/On	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH} + I_{IH}	Off–state output current, High–level voltage applied	I/On only	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, Low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				68	100	mA
		I_{CCL}					80	110	mA
		I_{CCZ}					73	105	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

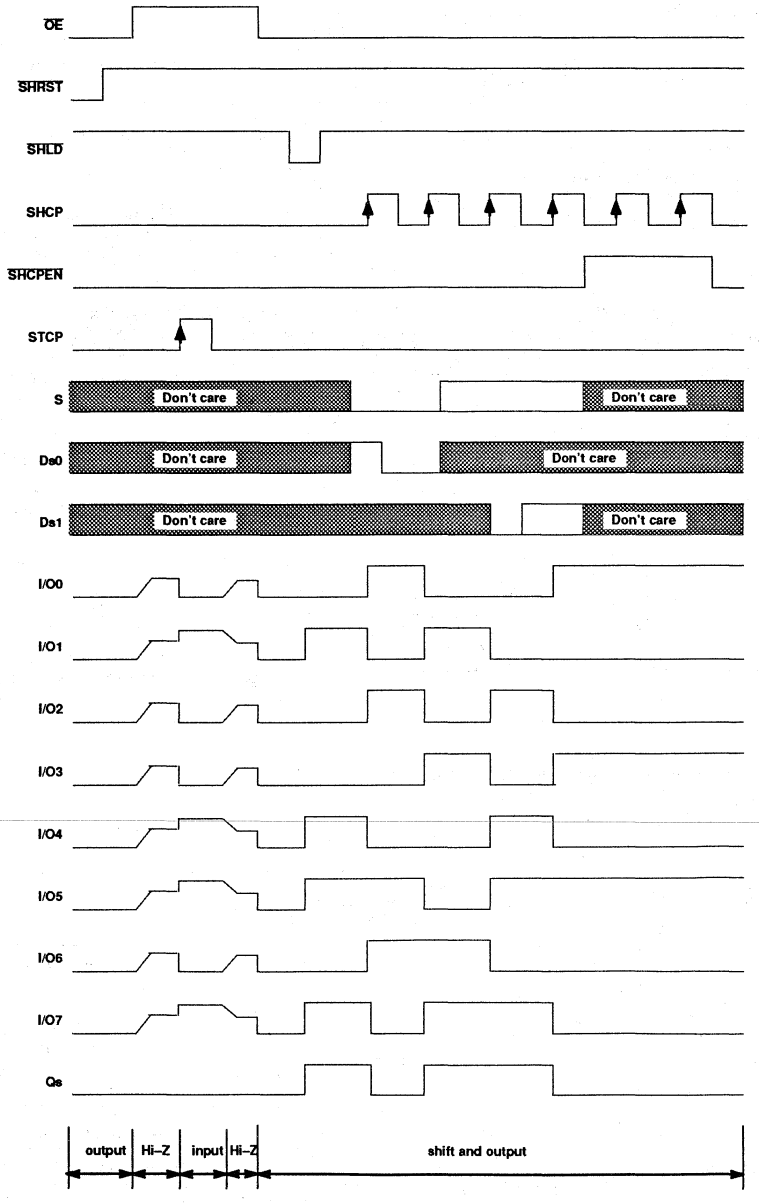
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	SHCP	Waveform 1	85	100		70		MHz
		STCP		140	160		130		
t_{PLH} t_{PHL}	Propagation delay SHCP to Qs		Waveform 1	9.5 6.5	11.5 8.5	14.0 11.5	8.5 6.0	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Qs ($\overline{SHLD}$ = Low)		Waveform 1	10.0 7.0	11.5 8.5	14.5 11.5	9.0 6.5	16.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Qs		Waveform 1	9.0 6.0	11.0 8.0	13.5 10.5	8.0 5.5	15.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SHCP to I/On		Waveform 1	8.5 5.0	10.5 7.0	13.5 9.5	7.0 4.5	15.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to I/On		Waveform 1	7.5 6.0	9.5 8.0	12.5 11.0	6.5 6.0	14.5 11.5	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to I/On		Waveform 2	6.5	9.0	12.0	6.0	12.5	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to Qs		Waveform 2	6.0	7.5	10.5	5.0	11.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low		Waveform 5 Waveform 6	3.5 3.0	5.5 5.0	8.5 7.5	3.0 2.5	9.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low		Waveform 5 Waveform 6	1.5 4.0	3.5 6.0	6.5 9.0	1.5 4.0	7.5 9.5	ns

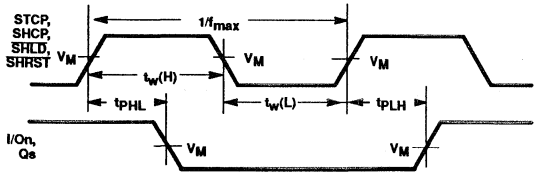
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s (H) t_s (L)	Setup time, High or Low Dsn to SHCP	Waveform 3	0.0 3.5			1.5 4.5		ns
t_h (H) t_h (L)	Hold time, High or Low DSn to SHCP	Waveform 3	0.0 2.5			0.0 3.0		ns
t_s (H) t_s (L)	Setup time, High or Low I/On to STCP	Waveform 3	2.5 2.5			2.5 3.0		ns
t_h (H) t_h (L)	Hold time, High or Low I/On to STCP	Waveform 3	0.0 0.0			1.5 2.0		ns
t_s (H) t_s (L)	Setup time, High or Low S to SHCP	Waveform 3	3.5 3.0			4.0 3.5		ns
t_h (H) t_h (L)	Hold time, High or Low S to SHCP	Waveform 3	2.5 3.0			3.0 3.0		ns
t_s (H)	Setup time, High, STCP to $\overline{SHLD}$	Waveform 4	7.0			8.0		ns
t_h (L)	Hold time, Low, STCP to $\overline{SHLD}$ (hold mode)	Waveform 4	0.0			0.0		ns
t_s (H) t_s (L)	Setup time, High or Low, $\overline{SHCPEN}$ to SHCP	Waveform 3	0.0 2.0			0.0 2.0		ns
t_h (H) t_h (L)	Hold time, High or Low, $\overline{SHCPEN}$ to SHCP	Waveform 3	0.0 4.5			0.0 5.5		ns
t_s (H)	Setup time, High, $\overline{SHLD}$ to SHCP↑	Waveform 3	7.5			8.5		ns
t_w (H) t_w (L)	SHCP Pulse width, High or Low	Waveform 1	5.5 4.0			6.5 4.0		ns
t_w (H) t_w (L)	STCP Pulse width, High or Low	Waveform 1	4.5 4.0			5.5 4.0		ns
t_w (L)	$\overline{SHRST}$ Pulse width, Low	Waveform 1	4.0			4.0		ns
t_w (L)	$\overline{SHLD}$ Pulse width, Low	Waveform 1	4.0			5.0		ns
t_{rec}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	0.0			0.0		ns

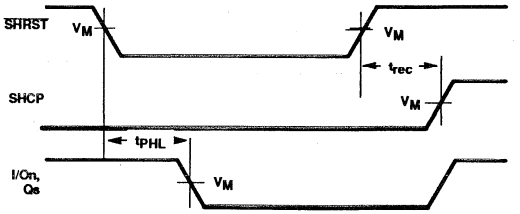
TYPICAL TIMING DIAGRAM



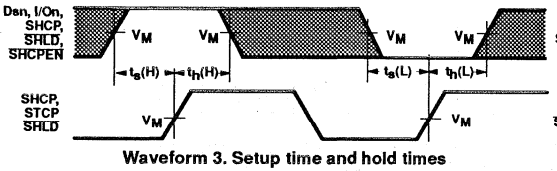
AC WAVEFORMS



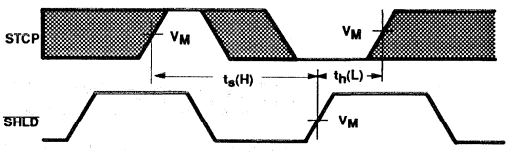
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency, shift register reset and load inputs to serial data output



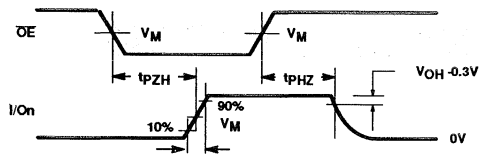
Waveform 2. Propagation delay for shift register reset to serial data output, shift register reset to shift register, shift register input recovery time



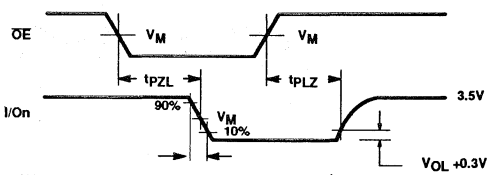
Waveform 3. Setup time and hold times



Waveform 4. Setup time and hold time



Waveform 5. 3-State output enable time to High level, output disable time from High level and transition time to High level



Waveform 6. 3-State output enable time to Low level, output disable time from Low level and transition time to Low level

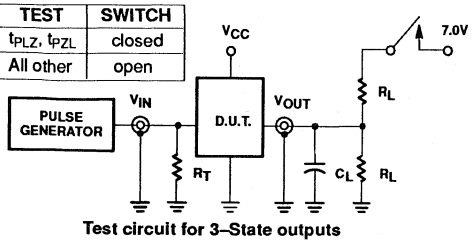
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



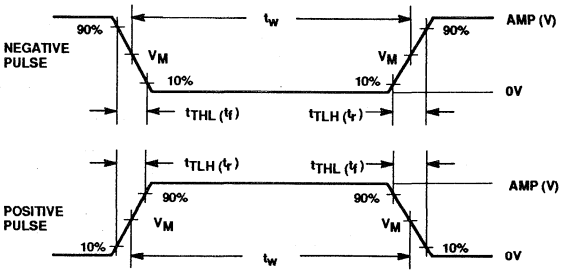
Test circuit for 3–State outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0029
ECN No.	98991
Date of issue	March 1, 1990
Status	Product Specification
FAST Products	

FAST 74F604
Latch

Dual Octal Latch (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F604	7.5ns	75mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in HIgh and Low states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **3-State outputs**
- **Power supply current 75mA typical**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F604N
28-Pin Plastic SOL	N74F604D

DESCRIPTION

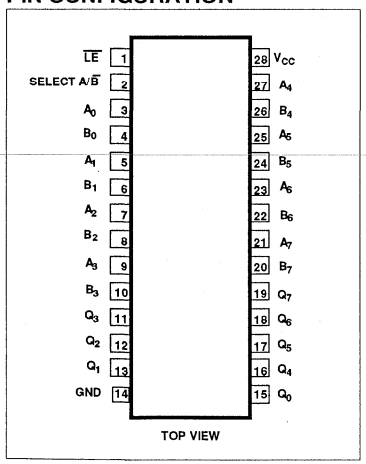
The 74F604 multiplexed latch is ideal for storing data from two input buses, A or B, and providing data from either the A or B latches to the output bus. Organized as 8-bit A and B latches, the latch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT A/$\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight 3-State outputs. Data entered from the B inputs are selected when SELECT A/$\overline{B}$ is Low; data from the A inputs are selected when SELECT A/$\overline{B}$ is High. Data enters the latches when the Latch Enable ($\overline{LE}$) input is Low and is latched on the $\overline{LE}$ rising edge. The outputs are enabled when $\overline{LE}$ is High and disabled when $\overline{LE}$ is Low.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

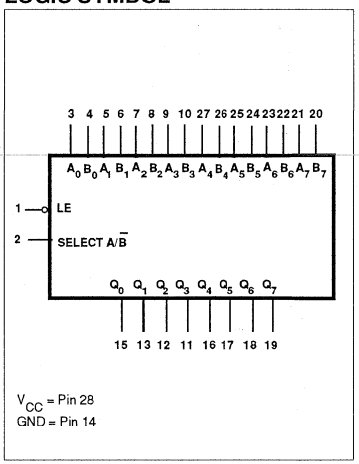
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	1.0/0.033	20μA/20μA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20μA/20μA
$\overline{LE}$	Latch Enable Input (active Low)	1.0/0.033	20μA/20μA
Q_0-Q_7	Data outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

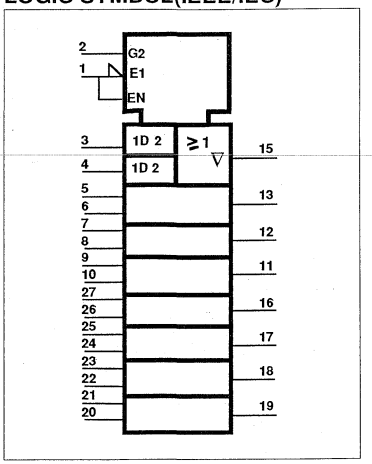
PIN CONFIGURATION



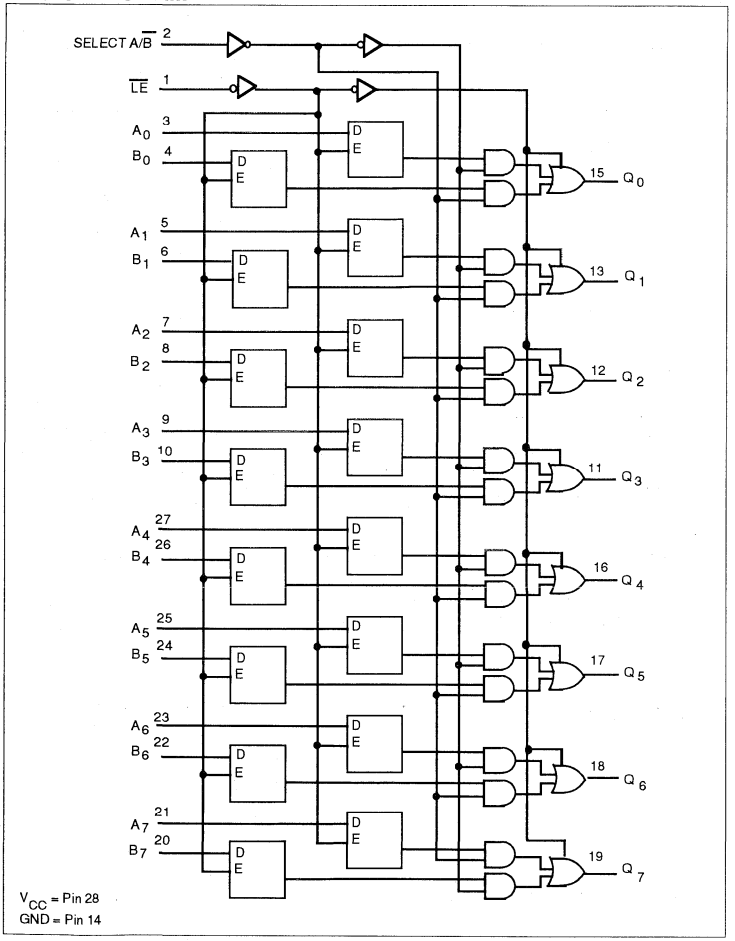
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
A_0-A_7	B_0-B_7	SELECT A/B	LE	Q_0-Q_7
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z
X	X	L	H	B latched data
X	X	H	H	A latched data

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OZH}	Off state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	A_n, B_n, SELECT A/$\overline{B}$=4.5V, $\overline{LE}$= ↑		60	82	mA
	Supply current (total) I_{CCL}	V_{CC} = MAX	A_n, B_n, SELECT A/$\overline{B}$=GND, $\overline{LE}$= ↑		75	100	mA
	Supply current (total) I_{CCZ}	V_{CC} = MAX	A_n, B_n, SELECT A/$\overline{B}$=GND, $\overline{LE}$= GND		75	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed lasty.

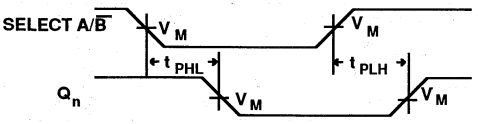
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay SELECT A/B to Q_n (B latch)	Waveform 1	5.0 6.0	7.0 8.5	9.0 10.5	4.5 5.5	10.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/B to Q_n (A latch)	Waveform 2	6.0 4.0	8.0 6.5	10.0 8.5	5.5 3.5	11.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	5.0 5.0	7.5 7.5	9.5 9.5	4.5 4.5	10.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low leve	Waveform 4 Waveform 5	5.0 5.0	7.0 7.0	9.5 9.5	4.5 4.5	11.0 11.0	ns

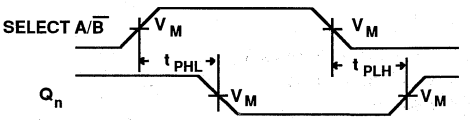
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n, B_n to LE	Waveform 3	1.0 2.0			2.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n, B_n to LE	Waveform 3	0 1.0			0 1.5		ns
t_w(L)	LE Pulse width, Low	Waveform 3	5.0			6.0		ns

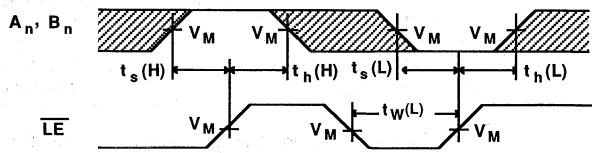
AC WAVEFORMS



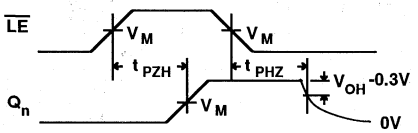
Waveform 1. Propagation Delay, SELECT A/B To Output (B latched data=Low. LE=H)



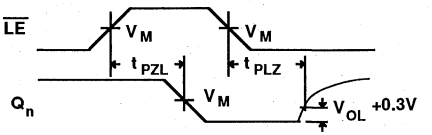
Waveform 2. Propagation Delay, SELECT A/B To Output (A latched data=Low. LE=H)



Waveform 3. Data Setup And Hold Times ,Latch Enable pulse width



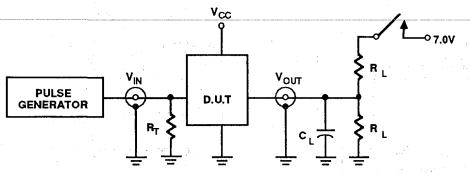
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

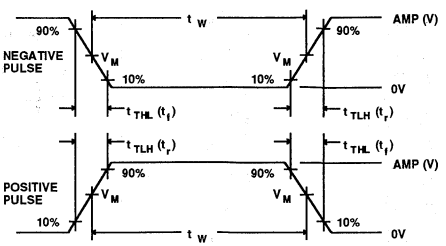
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0379
ECN No.	96249
Date of issue	April 6, 1990
Status	Product Specification
FAST Products	

FAST 74F620, 74F623 Transceivers

74F620 Octal Bus Transceiver, Inverting (3-State)
74F623 Octal Bus Transceiver, Non-Inverting (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F620	3.5ns	80mA
74F623	4.5ns	105mA

FEATURES

- **High impedance NPN base inputs for reduced loading (70µA in High and Low states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 64mA and source 15mA**
- **-'F620 Inverting**
  -'F623 Non-Inverting

DESCRIPTION

The 74F620 is an octal bus transceiver featuring inverting 3-state bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 74F623 is a non-inverting version of the 74F620.These octal bus transceivers are designed for asynchro-

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F620N, N74F623N
20-Pin Plastic SOL[1]	N74F620D, N74F623D

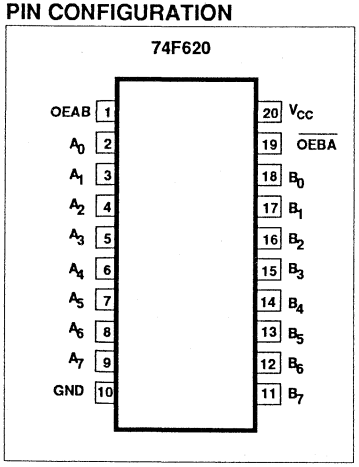
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal considerations for suface mounted device.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

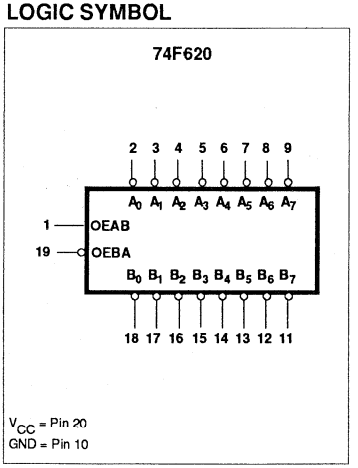
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	3.5/1.16	70µA/70µA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/0.033	20µA/20µA
A_0-A_7	Data outputs	150/40	3mA/24mA
B_0-B_7	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

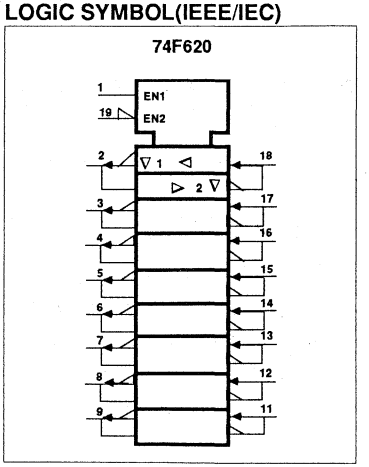
PIN CONFIGURATION



LOGIC SYMBOL

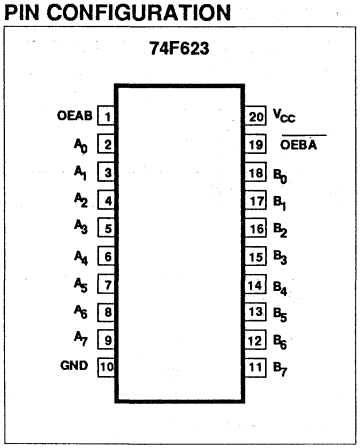


LOGIC SYMBOL(IEEE/IEC)

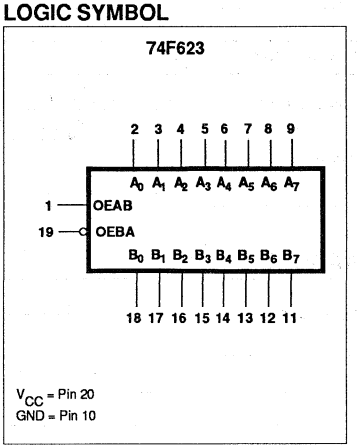


nous two-way communication between data busses. The control function implementation allows for maximum flexibilty in timing. These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the 'F620 and 'F623 the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance,both sets of bus lines (16 in all) will remain at their last states.

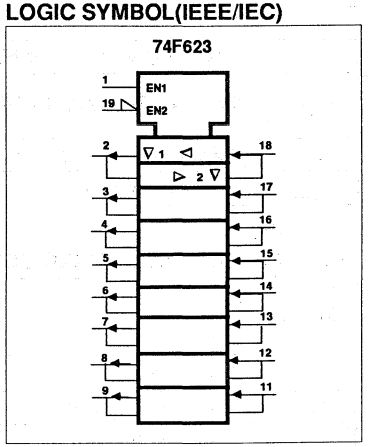
PIN CONFIGURATION



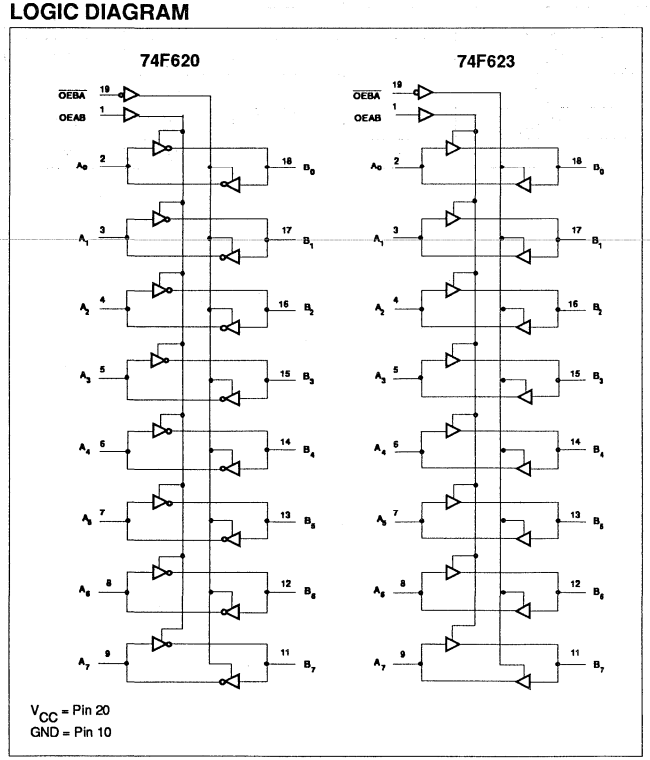
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OPERATING MODES	
$\overline{OEBA}$	OEAB	'F620	'F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus	B data to A bus
		$\overline{A}$ data to B bus	A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEBA}$, OEAB	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		Others	V_{CC} = 5.5V, V_I =5.5V					1	mA
I_{IH}	High-level input current	$\overline{OEBA}$, OEAB only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH} +I_{IH}	Off state output current, High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL}+I_{IL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-70	µA
I_{OS}	Short circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	'F620 I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=GND			70	92	mA
		'F620 I_{CCL}		$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=4.5V			84	110	mA
		'F620 I_{CCZ}		OEAB=GND; $\overline{OEBA}$= A_0-A_7=4.5V			84	110	mA
		'F623 I_{CCH}		$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=4.5V			110	140	mA
		'F623 I_{CCL}		$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=GND			110	140	mA
		'F623 I_{CCZ}		OEAB=GND; $\overline{OEBA}$= A_0-A_7=4.5V			99	130	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

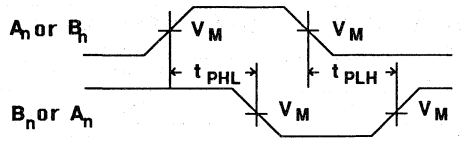
AC CHARACTERISTICS for 'F620

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	3.0 4.0	7.5 7.5	10.5 10.5	2.5 3.5	11.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	2.5 2.0	4.5 4.5	7.5 7.0	2.0 1.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	4.5 4.5	7.5 7.5	10.5 10.0	4.0 4.0	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.5 6.5	9.5 9.5	2.5 3.5	10.5 10.5	ns

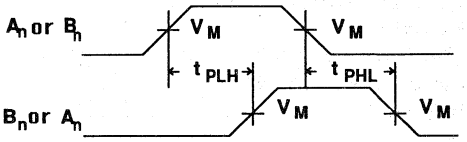
AC CHARACTERISTICS for 'F623

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	2.0 3.0	4.0 5.0	5.5 7.0	2.0 2.5	6.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	2.0 2.5	4.0 4.5	5.5 6.5	2.0 2.5	6.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	5.0 5.0	8.5 7.5	10.5 9.5	5.0 5.0	12.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.5 6.5	2.5 2.5	7.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	5.0 4.5	8.0 7.0	10.0 9.0	5.0 4.5	11.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.0 7.0	8.5 9.0	3.0 4.0	10.0 10.0	ns

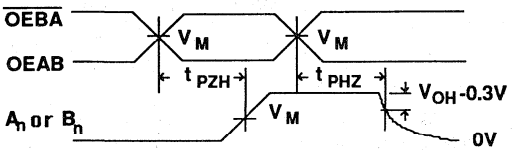
AC WAVEFORMS



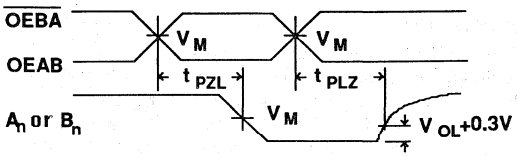
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



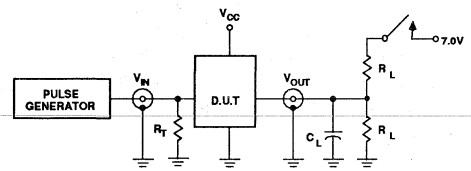
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

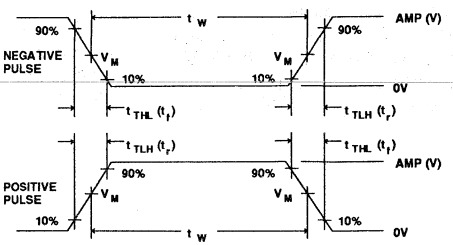
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

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Status	Product Specification
FAST Products	

FAST 74F621, 74F622 Transceivers

74F621 Octal Bus Transceiver, Non-Inverting (Open Collector)
74F622 Octal Bus Transceiver, Inverting (Open Collector)

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Octal bidirectional bus interface**
- **Open collector outputs sink 64mA**
- **-'F621 Non-Inverting**
  -'F622 Inverting

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F621	8.0ns	105mA
74F622	8.5ns	53mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F621N, N74F622N
20-Pin Plastic SOL[1]	N74F621D, N74F622D

NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal considerations for suface mounted device.

DESCRIPTION

The 74F621 is an octal bus transceiver featuring non-inverting open collector bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA, providing very good capacitive drive characteristics. The 74F622 is a inverting version of the 74F621. These octal bus transceivers are designed for asynchronous two-way communication between data busses. The control function implementation allows for maximum flexibilty in timing. These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the 'F621 and 'F622 the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB.

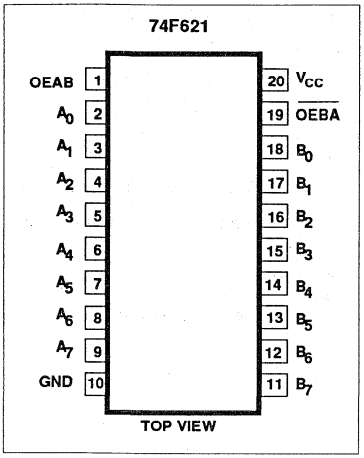
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/0.033	20μA/20μA
A_0- A_7	Data outputs	OC/40	OC/24mA
B_0- B_7	Data outputs	OC/106.7	OC/64mA

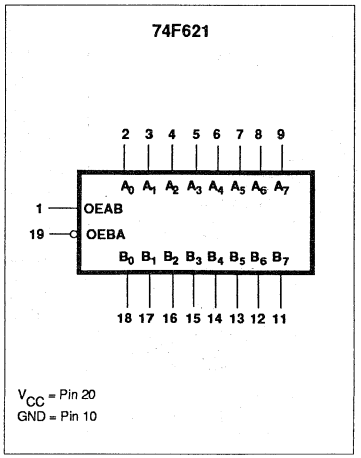
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC=Open Collector

Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

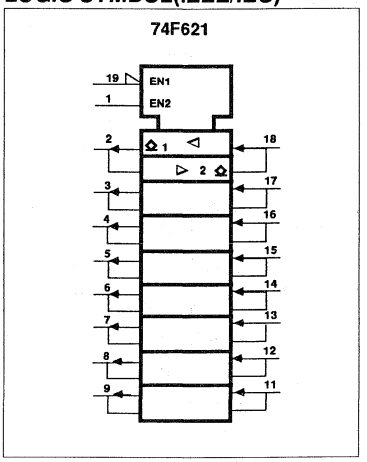
PIN CONFIGURATION



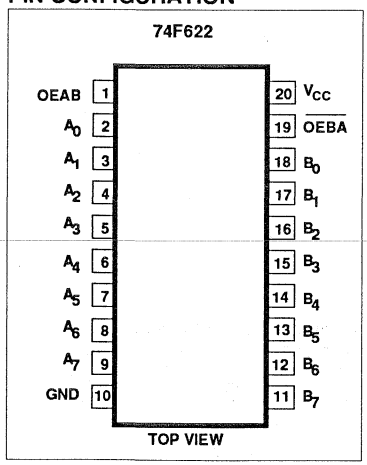
LOGIC SYMBOL



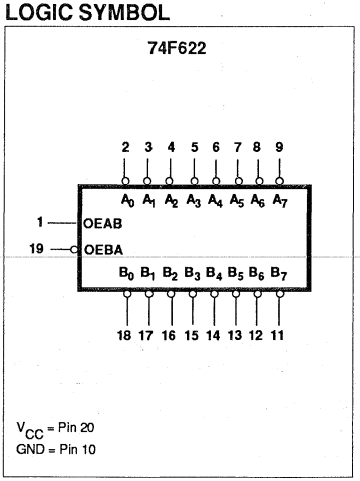
LOGIC SYMBOL(IEEE/IEC)



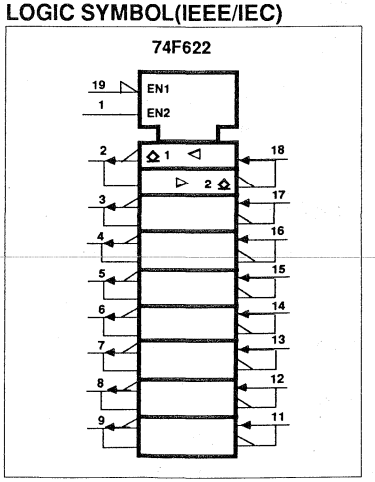
PIN CONFIGURATION



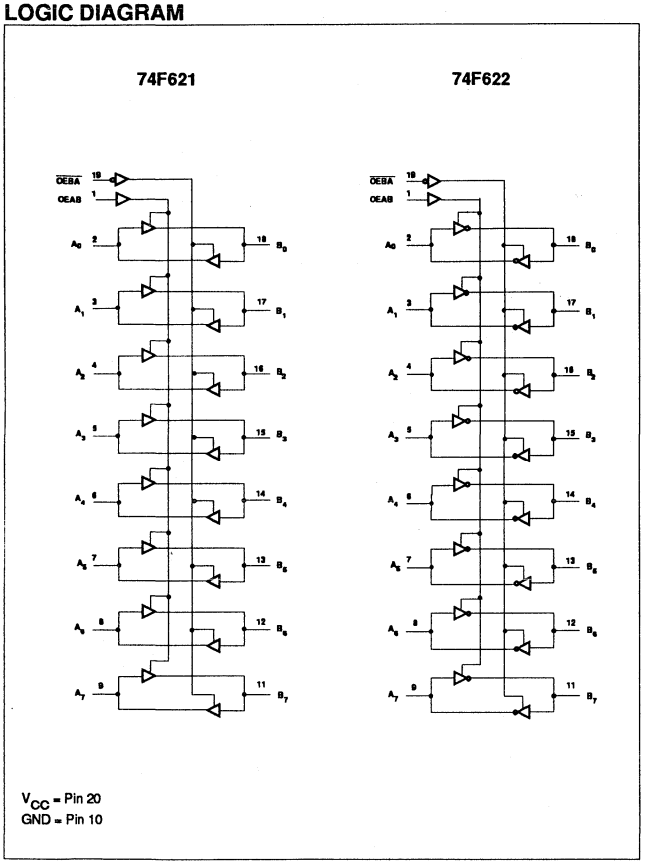
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OPERATING MODES	
$\overline{OEBA}$	OEAB	74F621	74F622
L	L	B data to A bus	$\overline{B}$ data to A bus
H	H	A data to B bus	$\overline{A}$ data to B bus
H	L	OFF	OFF
L	H	B data to A bus A data to B bus	$\overline{B}$ data to A bus $\overline{A}$ data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
OFF= High if pull-up resistor is connected to open collector output

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_7	48	mA
		B_0 - B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage				4.5	V
I_{OL}	Low-level output current	A_0 - A_7			24	mA
		B_0 - B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output voltage	A_0-A_7		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
		B_0-B_7			I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$		V_{CC} = 0.0V, V_I = 7.0V					100	µA
		others		V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{CC}	Supply current (total)	'F621	I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$=OEAB=A_0-A_7=4.5V			105	140	mA
			I_{CCL}		$\overline{OEBA}$=OEAB=4.5V, A_0-A_7=GND			105	140	mA
		'F622	I_{CCH}		$\overline{OEBA}$=OEAB=4.5V, A_0-A_7=GND			37	48	mA
			I_{CCL}		$\overline{OEBA}$=OEAB=A_0-A_7=4.5V			68	90	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

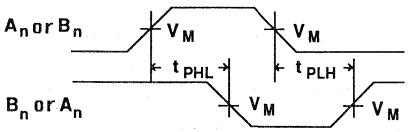
AC ELECTRICAL CHARACTERISTICS for 74F621

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	6.0 4.0	9.5 6.0	12.0 8.0	5.5 3.5	13.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	6.0 3.5	9.0 5.5	12.0 7.5	5.5 3.0	12.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEBA}$ to A_n	Waveform 3	6.0 3.5	10.0 6.5	13.5 10.5	5.5 3.0	14.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay OEAB to B_n	Waveform 4	7.0 3.5	12.0 6.5	15.0 9.5	6.0 3.0	17.0 10.0	ns

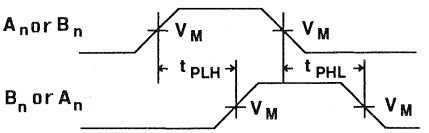
AC ELECTRICAL CHARACTERISTICS for 74F622

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	8.0 1.5	11.0 4.0	12.5 5.5	8.0 1.5	13.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	7.5 1.5	10.0 3.5	12.0 5.0	7.5 1.5	12.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEBA}$ to A_n	Waveform 3	8.0 6.0	10.5 8.0	12.0 10.0	8.0 6.0	12.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay OEAB to B_n	Waveform 4	10.0 5.0	12.5 7.5	14.5 9.0	10.0 5.0	15.5 9.5	ns

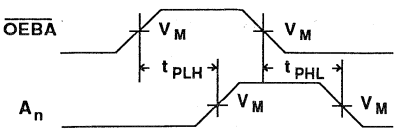
AC WAVEFORMS



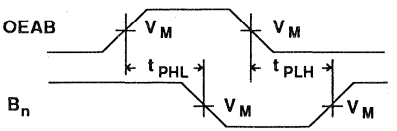
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



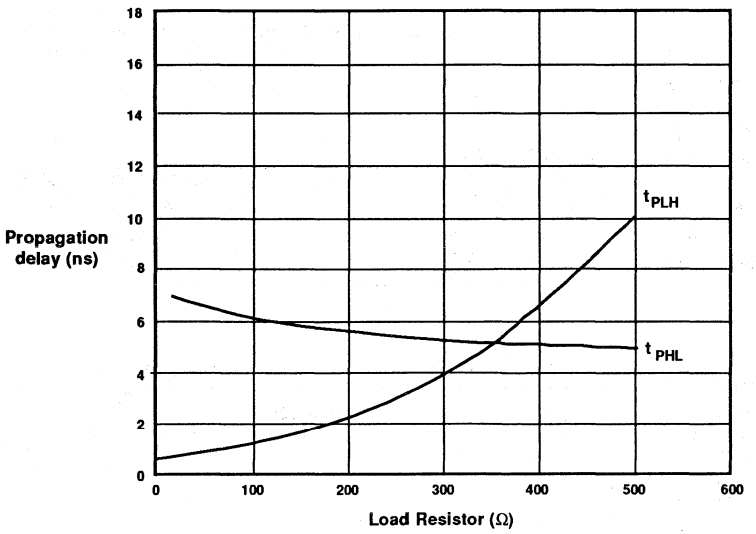
Waveform 3. Propagation delay, $\overline{OEBA}$ to An



Waveform 4. Propagation delay, OEAB to Bn

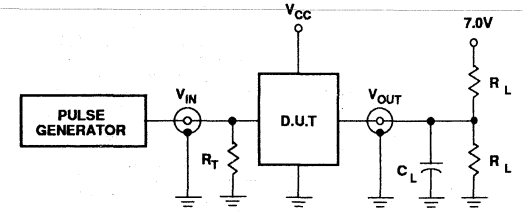
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

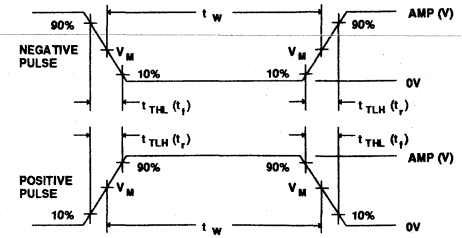


NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500 Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0381
ECN No.	98171
Date of issue	November 27, 1989
Status	Product Specification
FAST Products	

FAST 74F640
Transceiver

Octal Bus Transceiver , Inverting (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F640	3.5ns	78mA

FEATURES

- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Ideal for applications which require high-output drive and minimal bus loading**
- **Inverting version of 'F245**
- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 64mA and source 15mA**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F640N
20-Pin Plastic SOL	N74F640D

DESCRIPTION

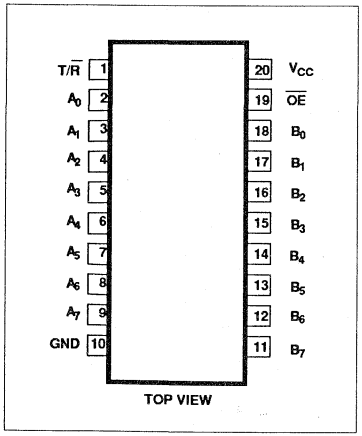
The 74F640 is an octal transceiver featuring inverting 3-state bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing 15mA, providing very good capacitive drive characteristics.The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive($T/\overline{R}$) input for direction control. The 3-state outputs, B_0-B_7, have been designed to prevent output bus loading if the power is removed from the device.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	3.5/0.115	70μA/70μA
$\overline{OE}$	Output enable input (active Low)	2.0/0.067	40μA/40μA
$T/\overline{R}$	Transmit/Receive input	2.0/0.067	40μA/40μA
A_0- A_7	A port outputs	150/40	3.0mA/24mA
B_0- B_7	B Port outputs	750/106.7	15mA/64mA

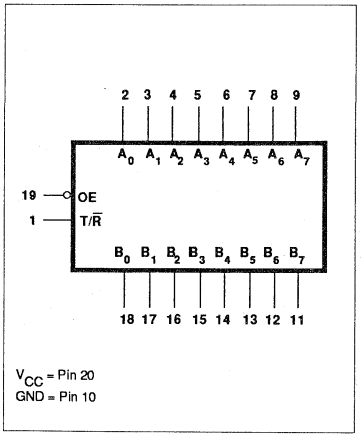
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



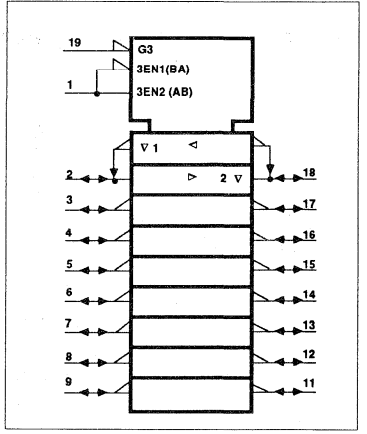
TOP VIEW

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

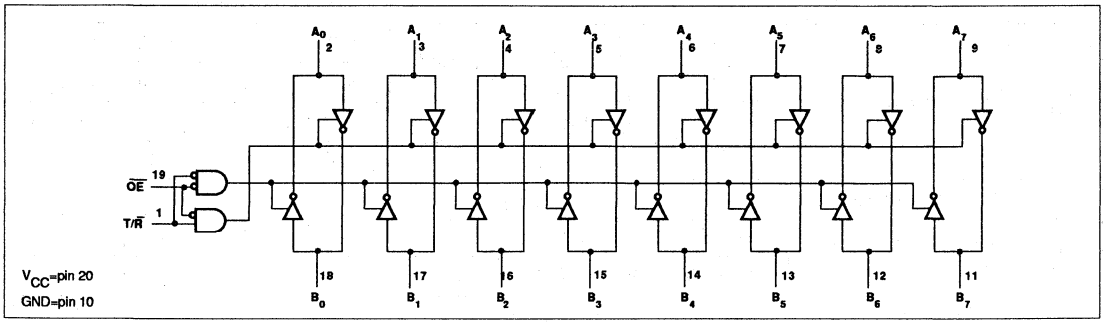


FUNCTION TABLE

INTPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus $\overline{A}$
L	H	Bus A data to Bus $\overline{B}$
H	X	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I =5.5V					1.0	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-40	µA
I_{OZH} +I_{IH}	Off state output current, High-level voltage applied		V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL}+I_{IL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-70	µA
I_{OS}	Short circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	T/$\overline{R}$=A_n=4.5V, $\overline{OE}$=GND			66	85	mA
		I_{CCL}		T/$\overline{R}$=B_n=$\overline{OE}$=GND			91	120	mA
		I_{CCZ}		T/$\overline{R}$=B_n=GND, $\overline{OE}$=4.5V			78	102	mA

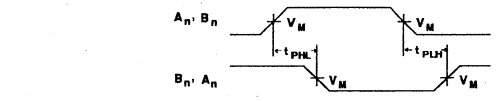
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

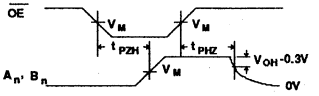
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.0 1.0	4.5 2.5	7.0 5.0	2.0 1.0	8.0 5.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	5.5 5.5	6.5 7.0	10.5 10.5	5.0 5.0	12.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	3.5 4.5	6.5 7.0	1.5 2.0	8.0 7.5	ns

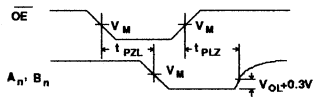
AC WAVEFORMS



Waveform 1. Propagation Delay For Inverting Outputs



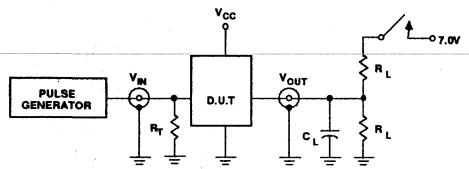
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

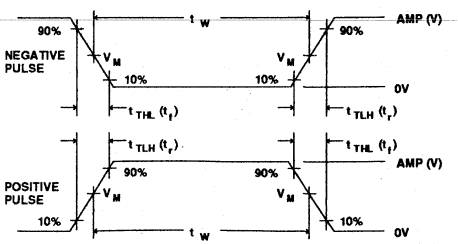
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0382
ECN No.	98172
Date of issue	November 27, 1989
Status	Product Specification
FAST Products	

FAST 74F641, 74F642 Transceivers

74F641 Octal Bus Transceiver With Common Output Enable, Non-Inverting (Open Collector)
74F642 Octal Bus Transceiver With Common Output Enable, Inverting (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F641	8.0ns	69mA
74F642	8.5ns	52mA

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Octal bidirectional bus interface
- Common Output Enable for both Transmit and Receive modes
- Open collector outputs sink 64mA
- -'F641 Non-Inverting
  -'F642 Inverting

ORDERING INFORMATION

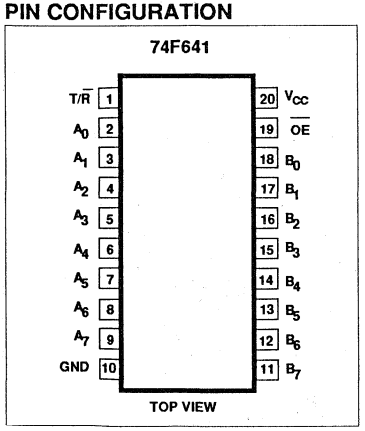
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F641N, N74F642N
20-Pin Plastic SOL	N74F641D, N74F642D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

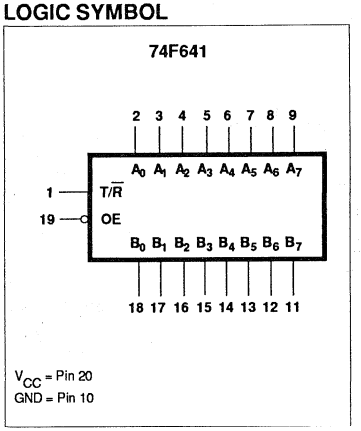
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	1.0/0.033	20μA/20μA
$T/\overline{R}$	Transmit / Receive input	2.0/0.067	40μA/40μA
$\overline{OE}$	Output Enable inputs	2.0/0.067	40μA/40μA
A_0- A_7	Data outputs	OC/40	OC /24mA
B_0- B_7	Data outputs	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC=Open Collector

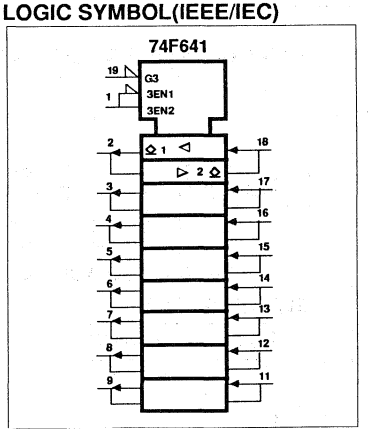
PIN CONFIGURATION



LOGIC SYMBOL

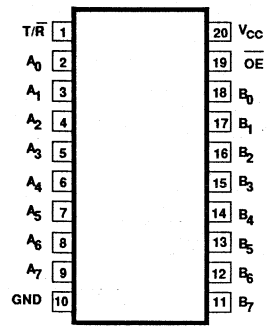


LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION

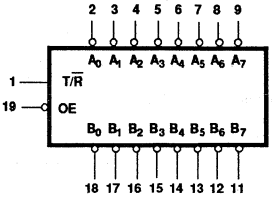
74F642



TOP VIEW

LOGIC SYMBOL

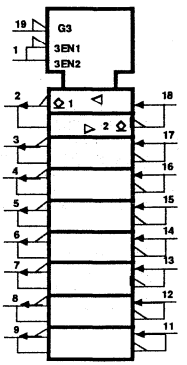
74F642



V_{CC} = Pin 20
GND = Pin 10

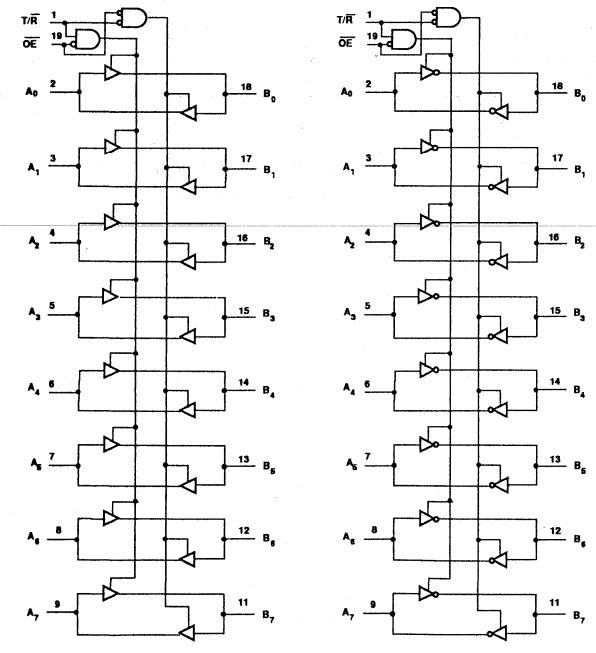
LOGIC SYMBOL(IEEE/IEC)

74F642



LOGIC DIAGRAM

74F641 74F642



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE 'F641

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A=B	INPUTS
L	H	INPUTS	B=A
H	X	OFF	OFF

H = High voltage level
L = Low voltage level
X = Don't care
OFF= High if pull-up resistor is connected to open collector output

FUNCTION TABLE 'F642

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A=$\overline{B}$	INPUTS
L	H	INPUTS	B=$\overline{A}$
H	X	OFF	OFF

H = High voltage level
L = Low voltage level
X = Don't care
OFF= High if pull-up resistor is connected to open collector output

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_7	48	mA
		B_0 - B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage				4.5	V
I_{OL}	Low-level output current	A_0 - A_7			24	mA
		B_0 - B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltag	T/$\overline{R}$, $\overline{OE}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	T/$\overline{R}$, $\overline{OE}$	V_{CC} = MAX, V_I = 2.7V					40	µA
		A_n, B_n						20	µA
I_{IL}	Low-level input current	T/$\overline{R}$, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V					-40	µA
		A_n, B_n						-20	µA
I_{CC}	Supply current (total)	'F641 I_{CCH}	V_{CC} = MAX	A_n=T/$\overline{R}$=4.5V, $\overline{OE}$=GND			60	90	mA
		'F641 I_{CCL}		T/$\overline{R}$=4.5V, A_n=$\overline{OE}$=GND			78	120	mA
		'F642 I_{CCH}		A_n=T/$\overline{R}$=$\overline{OE}$=4.5V			37	55	mA
		'F642 I_{CCL}		A_n=T/$\overline{R}$=4.5V, $\overline{OE}$=GND			67	98	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

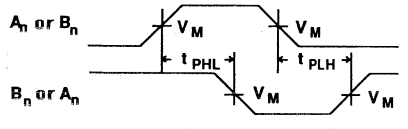
AC ELECTRICAL CHARACTERISTICS for 74F641

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	6.5 4.0	8.5 6.0	11.5 9.5	6.5 4.0	12.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	6.0 3.5	8.0 5.5	11.5 7.5	6.0 3.5	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n	Waveform 4	7.0 5.0	10.5 7.0	12.5 9.0	7.0 5.0	13.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	Waveform 4	8.0 5.5	9.0 7.5	12.5 9.5	8.0 5.5	13.5 10.5	ns

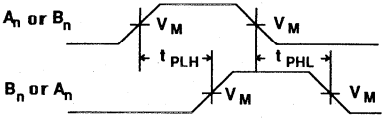
AC ELECTRICAL CHARACTERISTICS for 74F642

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	8.0 2.0	9.0 4.5	12.5 6.5	8.0 2.0	13.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	7.5 1.5	8.0 4.0	12.0 6.0	7.5 1.5	12.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n	Waveform 4	7.5 6.0	9.0 8.0	12.0 10.5	7.5 6.0	12.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	Waveform 4	8.0 6.0	9.0 7.0	12.5 10.5	8.0 6.0	13.0 11.0	ns

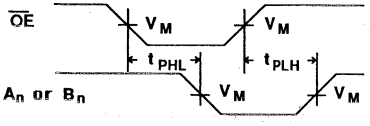
AC WAVEFORMS



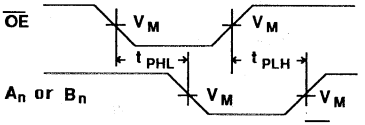
Waveform 1. Propagation delay for An to Bn or Bn to An ('F642)



Waveform 2. Propagation delay for An to Bn or Bn to An ('F641)



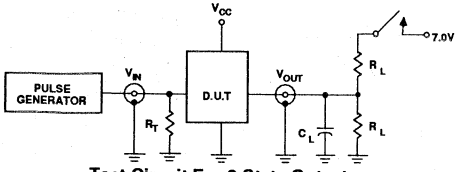
Waveform 3. Propagation delay for $\overline{OE}$ to An or Bn Outputs ('F642) (Bn or An inputs in High state)



Waveform 4. Propagation delay for $\overline{OE}$ to An or Bn Outputs ('F641) (Bn or An inputs in Low state)

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

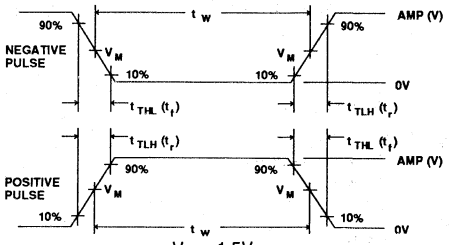
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Transceivers/registers — 74F646/A/74F648/A

74F646/646A Octal transceiver/register, non-inverting (3-State)
74F648/648A Octal transceiver/register, inverting (3-State)

FEATURES

- Combines 74F245 and two 74F374 type functions in one chip
- High impedance base inputs for reduced loading (70µA in high and low states)
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- Controlled ramp outputs for 74F646A/74F648A
- 3-state outputs
- 300 mil wide 24-pin slim dip package

DESCRIPTION

The 74F646/74F646A and 74F648/74F648A transceivers/registers consist of bus transceiver circuits with 3–state outputs, D–type flip–flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes high. Output enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) pins determine whether data is stored or transferred through the device in real–time. The DIR determines which bus will receive data when the $\overline{OE}$ is active low. In the isolation mode ($\overline{OE}$ = high), data from bus A may be stored in the B register and/or data from bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F646/74F648	115MHz	140mA
74F646A/74F648A	185MHz	105mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
24–pin plastic slim DIP (300mil)	N74F646N, N74F646AN, N74F648N, N74F648AN
24–pin plastic SOL[1]	N74F646D, N74F646AD, N74F648D, N74F648AD

NOTE: Thermal mounting techniques are recommended except for N74F646A/N648A. See SMD Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

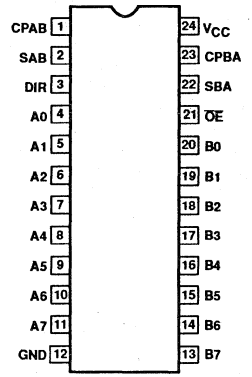
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
A0 – A7, B0 – B7	A and B inputs	3.5/0.116	70µA/70µA
CPAB	A–to–B clock input	1.0/0.033	20µA/20µA
CPBA	B–to–A clock input	1.0/0.033	20µA/20µA
SAB	A–to–B select input	1.0/0.033	20µA/20µA
SBA	B–to–A select input	1.0/0.033	20µA/20µA
DIR	Data flow directional control enable input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input	1.0/0.033	20µA/20µA
A0 – A7, B0 – B7	A, B outputs for N74F646A/N74F648A	750/80	15mA/48mA
A0 – A7, B0 – B7	A, B outputs for N74F646/N74F648	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

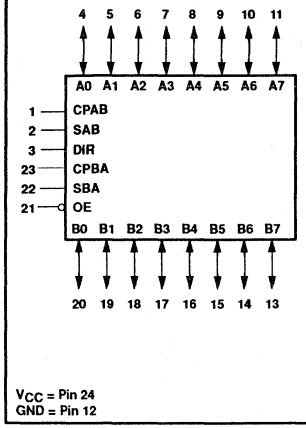
PIN CONFIGURATION

74F646/646A



LOGIC SYMBOL

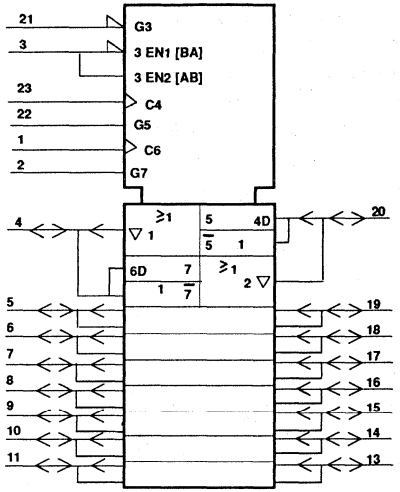
74F646/646A



VCC = Pin 24
GND = Pin 12

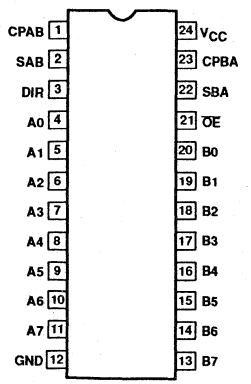
IEC/IEEE SYMBOL

74F646/646A



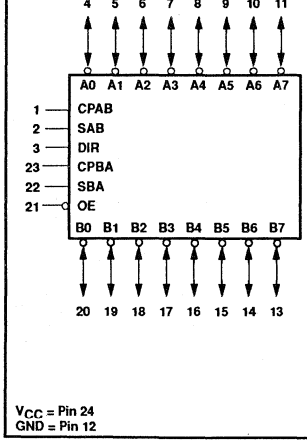
PIN CONFIGURATION

74F648/648A



LOGIC SYMBOL

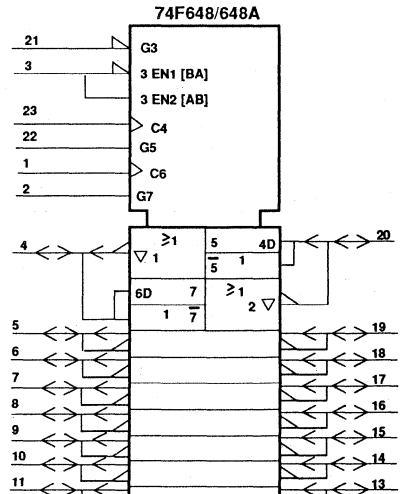
74F648/648A



VCC = Pin 24
GND = Pin 12

IEC/IEEE SYMBOL

74F648/648A



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	74F646/74F646A	74F648/74F648A
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real tme B data to A bus	Real tme $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real tme A data to B bus	Real tme $\overline{A}$ data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus	Stored $\overline{A}$ data to B bus

NOTES:
1. H = High–voltage level
2. L = Low–voltage level
3. X = Don't care
4. ↑ = Low–to–high clock transition
5. * = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low–to–high transition of the clock.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

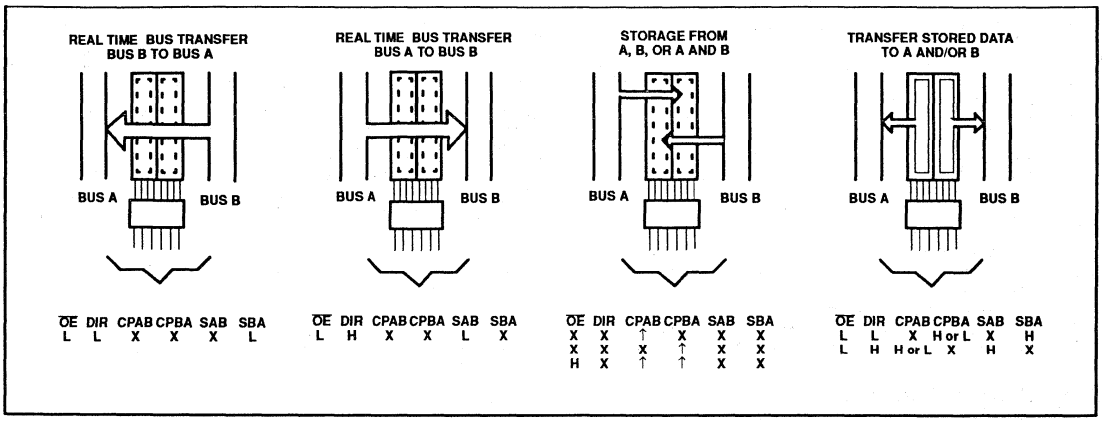
SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	74F646A, 74F648A	72	mA
		74F646, 74F648	128	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

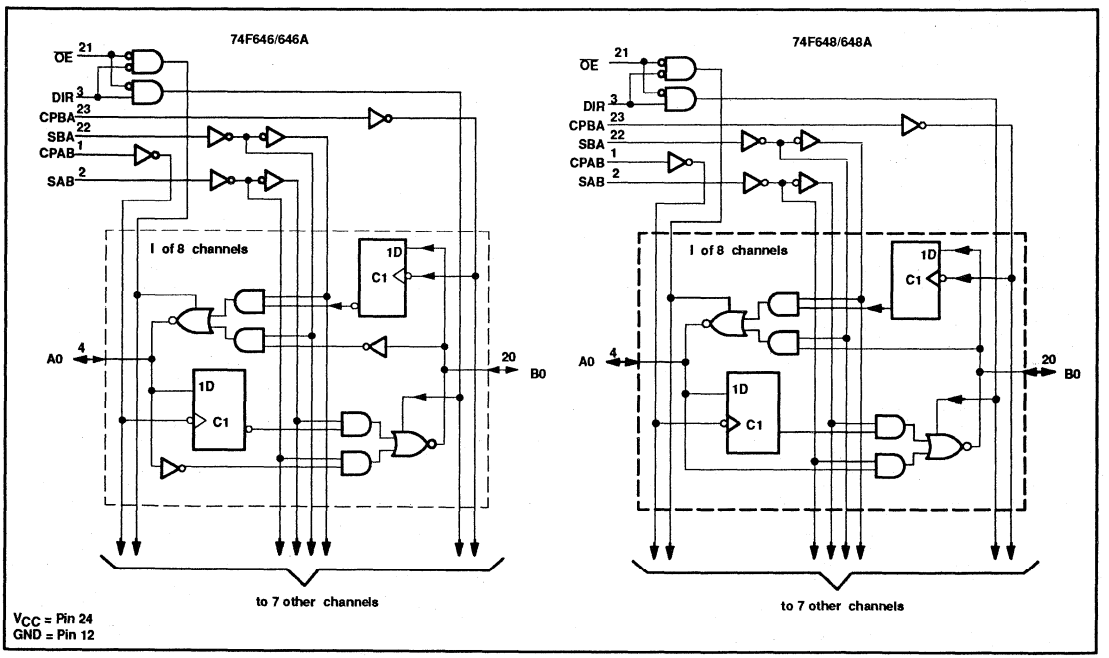
SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–15	mA
I_{OL}	Low–level output current	74F646A, 74F648A			48	mA
		74F646, 74F648			64	mA
T_{amb}	Operating free air temperature range		0		+70	°C

The following examples demonstrate the four fundamental bus–management functions that can be performed with the 74F646/646A and 74F648/648A. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

BUS MANAGEMENT FUNCTIONS



LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	All	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.38	0.55	V
		74F646/74F648 only		I_{OL} = 64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High–level input current	$\overline{OE}$, DIR, CPAB, CPBA, SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH} + I_{IH}	Off–state output current, high–level voltage applied	A0 – A7, B0 –B7	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OS}	Short–circuit output current[3]	74F646, 74F648	V_{CC} = MAX			-100		-225	mA
I_O	Output current[4]	74F646A, 74F648A	V_{CC} = MAX, V_O = 2.25V			-60		-150	mA
I_{CC}	Supply current (total)	74F646, 74F648	I_{CCH}	V_{CC} = MAX			125	165	mA
			I_{CCL}				160	210	mA
			I_{CCZ}				135	160	mA
		74F646A, 74F648A	I_{CCH}	V_{CC} = MAX			100	145	mA
			I_{CCL}				110	155	mA
			I_{CCZ}				105	155	mA

NOTES:

6. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
7. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
8. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
9. I_O is tested under conditions that produce current approximately one half of the true short–circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS FOR 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.5 5.5	7.5 8.0	10.0 10.0	5.0 5.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	4.0 4.0	6.0 6.5	9.0 8.0	4.0 4.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	5.0 5.0	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	5.0 6.5	7.0 8.5	10.0 11.0	4.5 6.0	11.0 12.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	4.5 6.0	6.5 8.5	9.0 11.0	4.0 5.5	10.0 12.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	6.5 6.5	9.0 9.0	11.5 11.5	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	5.5 5.5	8.5 8.5	11.0 11.0	4.5 5.0	13.0 12.5	ns

AC SETUP REQUIREMENTS FOR 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.0	7.0 7.5	9.5 9.5	4.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 3	3.0 4.0	6.0 6.0	8.5 8.5	2.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2,3	4.5 4.5	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.5 5.5	11.0 12.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.0 5.5	11.0 12.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	6.0 6.0	9.0 8.5	11.5 12.0	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	5.0 5.0	9.0 9.0	12.5 12.5	4.5 5.0	14.0 14.0	ns

AC SETUP REQUIREMENTS FOR 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	3.5 6.5			4.0 7.0		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	165	185		150		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.5 4.5	7.0 7.0	10.5 9.5	4.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	4.0 2.0	6.0 5.0	9.0 8.0	3.5 2.0	10.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.5 3.5	6.5 8.0	9.5 10.0	4.0 3.0	10.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	3.0 3.0	5.5 5.5	9.0 10.0	2.5 2.5	10.0 10.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	3.0 3.5	5.0 6.0	8.0 8.5	3.0 3.0	8.5 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	1.5 2.5	4.0 5.5	6.5 8.0	1.0 2.0	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	2.0 3.0	4.5 5.0	7.5 8.0	1.5 2.0	8.5 8.5	ns

AC SETUP REQUIREMENTS FOR 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	3.5 3.5			4.5 4.0		ns

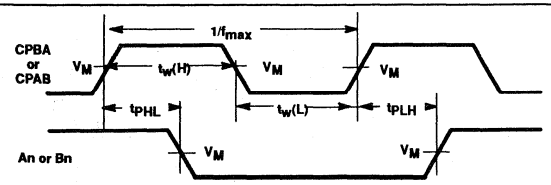
AC ELECTRICAL CHARACTERISTICS FOR 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	160	185		135		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.5	7.0 7.5	9.5 10.0	4.5 4.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 3	2.5 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.0 4.5	7.0 7.0	9.5 9.5	3.5 4.5	11.5 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	3.5 4.5	6.5 6.5	10.0 10.0	3.5 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	3.5 4.0	5.5 6.5	8.5 9.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	2.5 4.0	4.0 6.5	6.5 9.0	2.0 3.5	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	2.5 2.5	5.0 5.0	8.5 8.0	2.0 3.5	9.0 9.0	ns

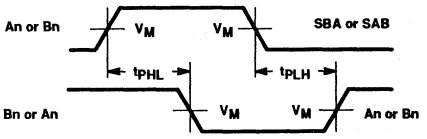
AC SETUP REQUIREMENTS FOR 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.0 4.0			4.5 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	3.5 3.5			4.0 3.5		ns

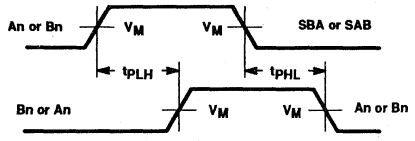
AC WAVEFORMS



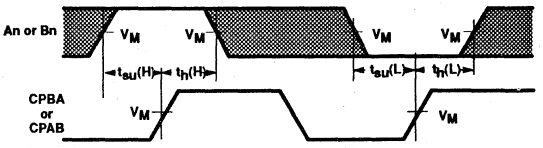
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



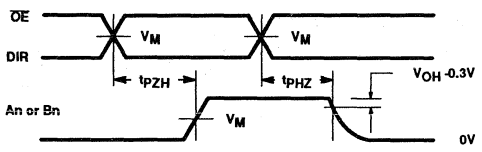
Waveform 2. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



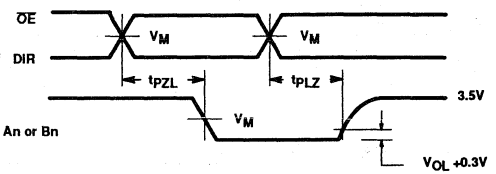
Waveform 3. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



Waveform 4. Data setup time and hold times



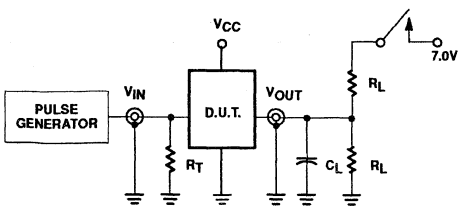
Waveform 5. 3-state output enable time to high level and output disable time from high level



Waveform 6. 3-state output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test circuit for 3–state outputs

SWITCH POSITION

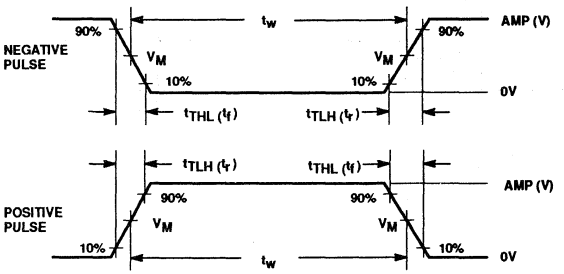
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0876
ECN No.	05853
Date of issue	February 28, 1992
Status	Product Specification
FAST Products	

FAST 74F647, 74F649 Transceivers/Registers

74F647 Octal Transceiver/Register, Non-Inverting (Open Collector)
74F649 Octal Transceivers/Register, Inverting (Open Collector)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F647	65MHz	125mA
74F649	65MHz	125mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **Open Collector outputs**
- **300 mil wide 24-pin Slim Dip package**

DESCRIPTION

The 74F647 and 74F649 Transceivers/Registers consist of bus transceiver circuits with open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both. The select (SAB,SBA) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive data when the Output Enable, $\overline{OE}$ is active Low. In the isolation mode (Output Enable, $\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses, A or B, may be driven at a time. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F647 and 'F649.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F647N, N74F649N
24-Pin Plastic SOL[1]	N74F647D, N74F649D

NOTE : 1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

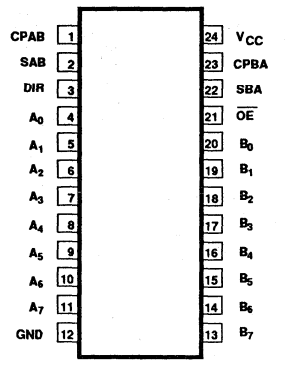
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	1.0/0.033	20μA/20μA
B_0 - B_7	B inputs	1.0/0.033	20μA/20μA
CPAB	A-to-B clock inputs	1.0/0.033	20μA/20μA
CPBA	B-to-A clock inputs	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
DIR	Data flow Directional control enable input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output Enable input	1.0/0.033	20μA/20μA
A_0 - A_7	A outputs	OC/106.7	OC/64mA
B_0 - B_7	B outputs	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC=Open-Collector

PIN CONFIGURATION

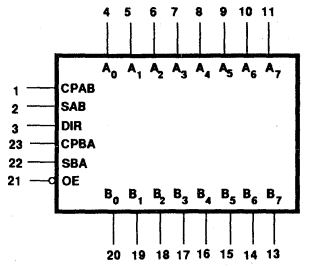
'F647



TOP VIEW

LOGIC SYMBOL

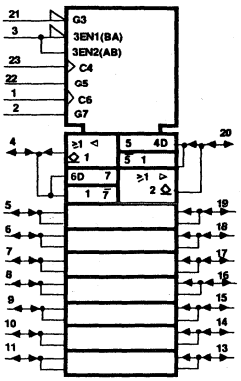
'F647



V_{CC} = Pin 24
GND = Pin 12

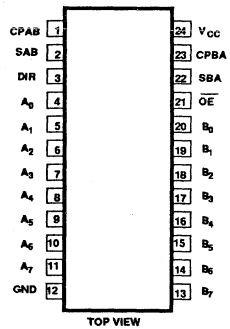
LOGIC SYMBOL(IEEE/IEC)

'F647



PIN CONFIGURATION

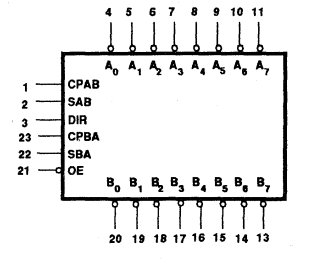
'F649



TOP VIEW

LOGIC SYMBOL

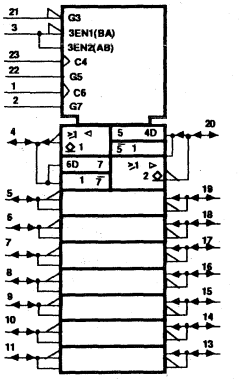
'F649



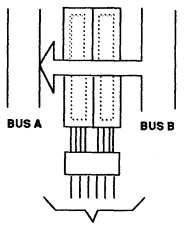
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F649

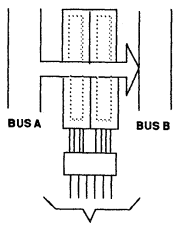


REAL TIME BUS TRANSFER BUS B TO BUS A



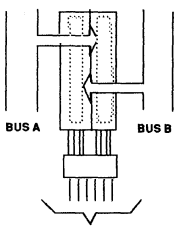
OE	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



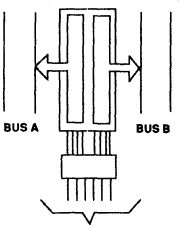
OE	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



OE	DIR	CPAB	CPBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



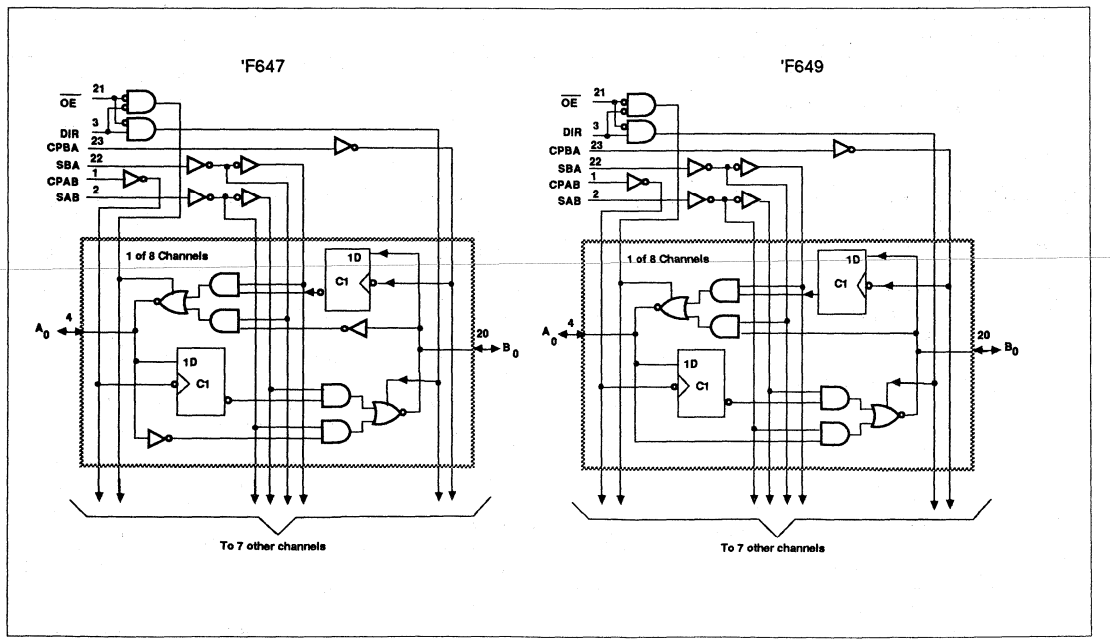
OE	DIR	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	'F647	'F649
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store A, B unspecified*	Store A, B unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus	Real time B data to A bus Stored B data to A bus
L L	H H	H or L X	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus	Real time A data to B bus Stored A data to B bus

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High clock transition
*= The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} =0.0V, V_I = 7.0V					100	µA
		A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				105	145	mA
		I_{CCL}					145	200	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

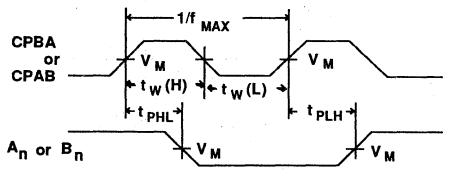
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	50	65		40		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to B_n or CPBA to A_n	Waveform 1	7.0 5.5	12.0 8.5	15.0 11.0	7.0 5.5	16.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2 Waveform 3	7.5 4.0	10.5 7.0	13.5 9.5	7.5 4.0	16.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n	Waveform 2 Waveform 3	7.5 4.0	11.5 7.0	14.5 9.5	7.5 4.0	17.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n or B_n	Waveform 2 Waveform 3	9.0 6.5	13.0 10.0	16.0 12.5	9.0 6.5	18.5 13.5	ns
t_{PLH} t_{PHL}	Propagation delay DIR to A_n or B_n	Waveform 2 Waveform 3	9.0 7.0	13.0 15.0	16.0 18.0	9.0 7.0	18.5 20.0	ns

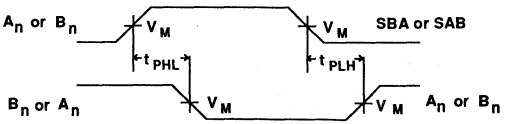
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n to CPBA or B_n to CPAB	Waveform 4	4.0 4.0			5.0 5.0		ns
t_s(H) t_s(L)	Hold time, High or Low A_n to CPBA or B_n to CPAB	Waveform 4	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.0			4.5 6.5		ns

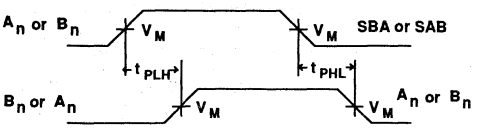
AC WAVEFORMS



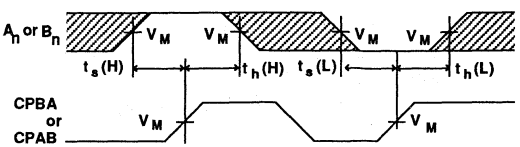
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



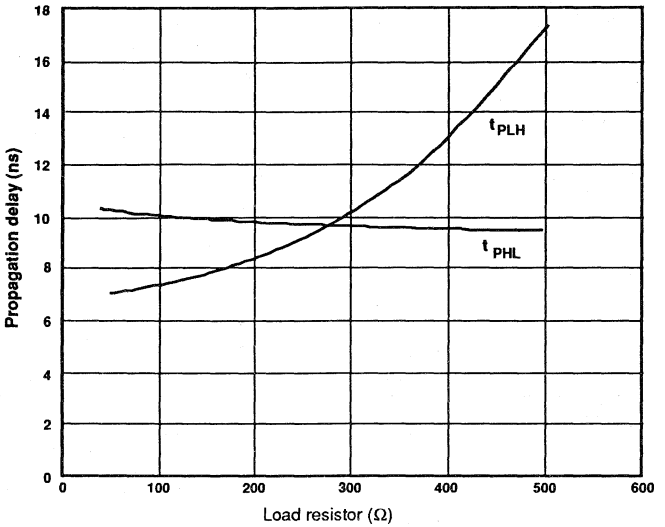
Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



Waveform 4. Data Setup And Hold Times

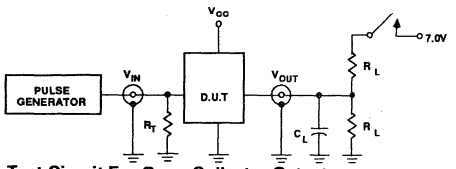
NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs

SWITCH POSITION

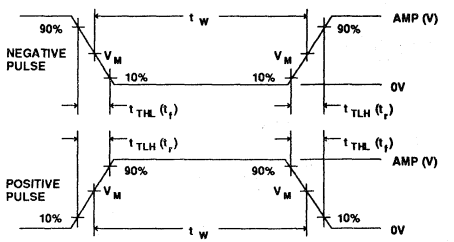
TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Transceivers/registers

74F651/74F652
74F651A/74F652A

74F651/74F651A octal transceiver/register, inverting (3–state)
74F652/74F652A octal transceiver/register, non–inverting (3–state)

FEATURES

- Combines 74F245 and two 74F374 type functions in one chip
- High impedance base inputs for reduced loading (70μA in high and low states)
- Independent registers for A and B buses
- Multiplexed real–time and stored data
- Choice of non–inverting and inverting data paths
- 3–state outputs
- Industrial temperature range available (–40°C to +85°C) for 74F652A

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F651/74F652	110MHz	140mA
74F651A/74F652A	175MHz	110mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
24–pin plastic slim DIP (300mil)[1]	N74F651N, N74F652N	
24–pin plastic slim DIP (300mil)	N74F651AN, N74F652AN	I74F652AN
24–pin plastic SOL[1]	N74F651AD, N74F652AD	I74F652AD

Note to ordering information
1.Thermal mounting techniques are recommended. See SMD Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

DESCRIPTION

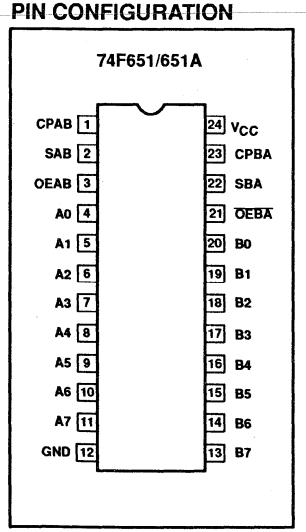
The 74F651/74F651A and 74F652/74F652A transceivers/registers consist of bus transceiver circuits with 3–state outputs, D–type flip–flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes high. Output enable (OEAB, $\overline{OEBA}$) and select (SAB, SBA) pins are provided for bus management.

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

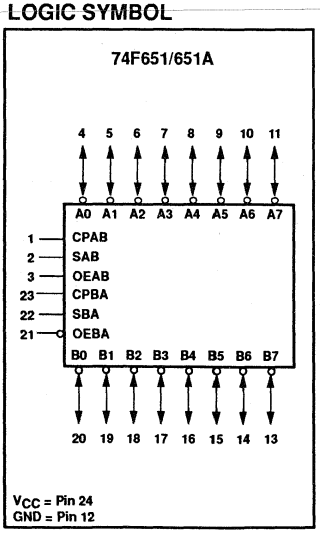
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7, B0 – B7	A, B inputs	3.5/0.116	70μA/70μA
CPAB, CPBA	A–to–B, B–to–A clock inputs	1.0/0.033	20μA/20μA
SAB, SBA	A–to–B, B–to–A select inputs	1.0/0.033	20μA/20μA
OEAB, $\overline{OEBA}$	A–to–B, B–to–A output enable inputs	1.0/0.033	20μA/20μA
A0 – A7, B0 – B7	A, B outputs for N74F651, N74F652	750/106.7	15mA/64mA
A0 – A7, B0 – B7	A, B outputs for N74F651A, N74F652A	750/80	15mA/48mA
A0 – A7, B0 – B7	A, B outputs for I74F652A	750/60	15mA/36mA

Note to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

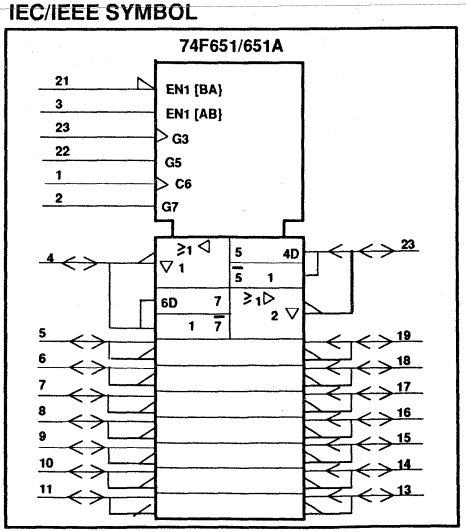
PIN CONFIGURATION



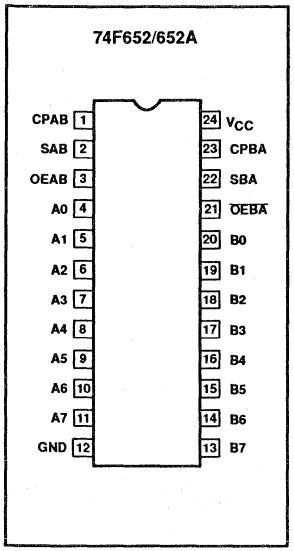
LOGIC SYMBOL



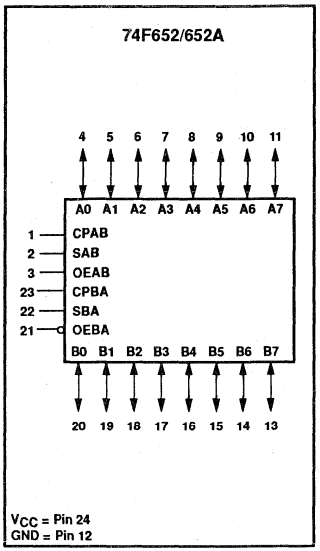
IEC/IEEE SYMBOL



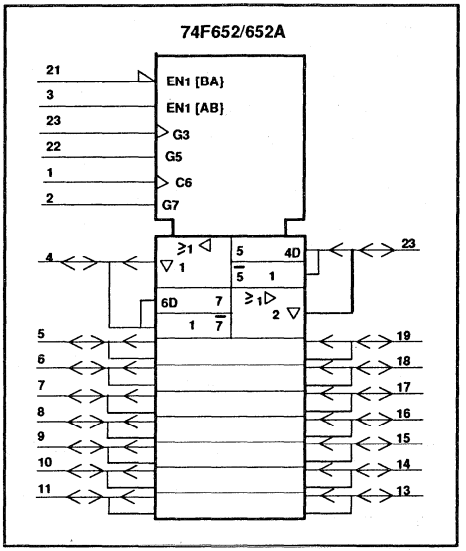
PIN CONFIGURATION



LOGIC SYMBOL

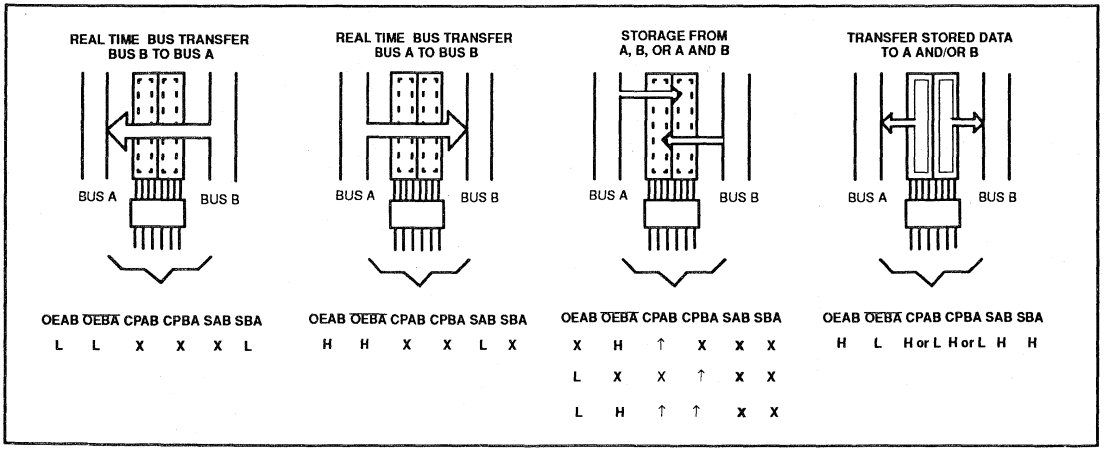


IEC/IEEE SYMBOL

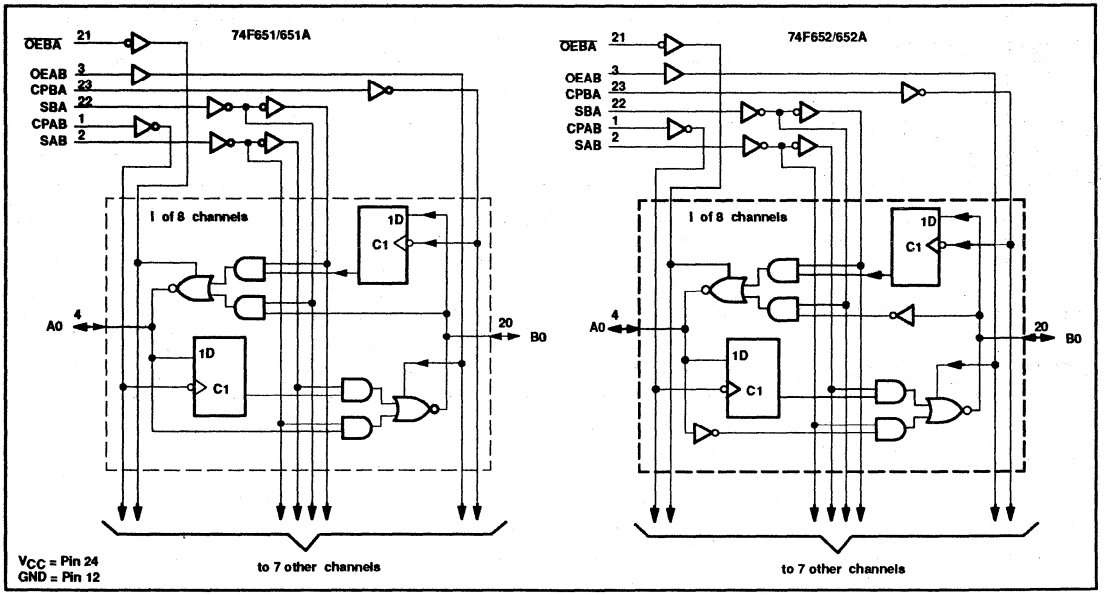


The following examples demonstrate the four fundamental bus–management functions that can be performed with the 74F651/651A and 74F652/652A. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

BUS MANAGEMENT FUNCTIONS



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	74F651/74F651A	74F652/74F652A
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, hold B	Store A hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, store B	Hold A, store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{B}$ data to A bus	Stored B data to A bus

Notes to function table

1. H = High–voltage level
2. L = Low–voltage level
3. * = The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low–to–high transition of the clock.
4. ↑ = Low–to–high clock transition
5. X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	74F651, 74F652	128	mA
		74F651A, 74F652A	72	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER			LIMITS			UNIT
				MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5.0	5.5	V
V_{IH}	High–level input voltage			2.0			V
V_{IL}	Low–level input voltage					0.8	V
I_{Ik}	Input clamp current					–18	mA
I_{OH}	High–level output current					–15	mA
I_{OL}	Low–level output current	Commercial range	74F651, 74F652			64	mA
			74F651A, 74F652A			48	mA
		Industrial range (74F652A only)				36	mA
T_{amb}	Operating free air temperature range	Commercial range		0		+70	°C
		Industrial range (74F652A only)		–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}			0.55	V
			V_{IH} = MIN		±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High–level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA, SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH} + I_{IH}	Off–state output current, high–level voltage applied	A0 – A7, B0 –B7	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OS}	Short–circuit output current[3]	74F651, 74F652	V_{CC} = MAX			-100		-225	mA
I_O	Output current[4]	74F651A, 74F652A	V_{CC} = MAX, V_O = 2.25V			-60		-160	mA
I_{CC}	Supply current (total)	74F651, 74F652	I_{CCH}	V_{CC} = MAX			110	155	mA
			I_{CCH}				140[5]	185[5]	mA
			I_{CCL}				155	200	mA
			I_{CCL}				165[5]	240[5]	mA
			I_{CCZ}				130	175	mA
		74F651A, 74F652A	I_{CCH}	V_{CC} = MAX			105	145	mA
			I_{CCL}				115	165	mA
			I_{CCZ}				115	160	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short–circuit output current (I_{OS}).
5. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. When using worst case conditions thermal mounting is required.

AC ELECTRICAL CHARACTERISTICS FOR 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	90	110		80		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.5	7.0 7.5	10.5 11.0	4.5 5.0	12.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Bn or An	Waveform 2, 3	3.0 3.0	6.0 6.0	10.0 9.0	2.5 3.0	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.0 4.0	7.0 6.5	10.0 9.5	4.0 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	4.0 6.0	7.0 10.5	10.0 12.0	3.5 5.5	11.0 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	4.5 4.5	9.5 9.0	13.0 13.0	4.0 4.0	14.5 15.5	ns

AC SETUP REQUIREMENTS FOR 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

Note to AC setup requirements for 74F651/652

1. Setup time is to protect against surge current caused by enabling 16 outputs (64mA per output) simultaneously.

AC ELECTRICAL CHARACTERISTICS FOR 74F651A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	155	175		140		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	4.5 5.5	7.0 7.5	10.0 10.5	4.0 5.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Bn or An	Waveform 2, 3	2.5 4.0	4.5 6.5	7.5 9.0	2.0 4.0	8.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.0 5.0	7.0 7.0	10.0 10.0	3.5 4.5	12.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	3.0 3.5	5.0 6.0	8.0 8.5	2.5 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	1.5 2.5	4.0 6.0	7.0 8.5	1.0 2.0	7.5 9.0	ns

AC SETUP REQUIREMENTS FOR 74F651A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.5 3.5			4.5 4.0		ns

Note to AC setup requirements for 74F651A

1. Setup time is to protect against surge current caused by enabling 16 outputs (48mA per output) simultaneously.

AC ELECTRICAL CHARACTERISTICS FOR 74F652A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	155	175		140		140		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.0	7.5 7.0	10.0 10.0	4.5 4.5	11.5 10.5	4.5 4.5	11.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Bn or An	Waveform 1	4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 8.5	3.5 2.5	10.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.5 4.0	7.0 8.0	10.0 10.0	4.0 4.0	11.0 11.5	4.0 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time[1] OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	3.0 3.5	5.0 6.0	8.0 8.5	2.5 3.0	8.5 9.0	2.5 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	1.5 2.5	4.0 6.0	7.0 8.5	1.0 2.0	7.5 9.0	1.0 2.0	7.5 9.0	ns

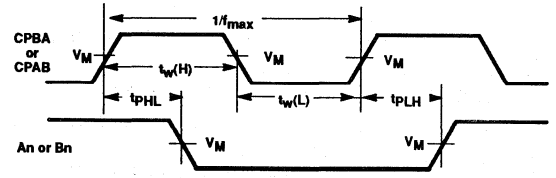
AC SETUP REQUIREMENTS FOR 74F652A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		4.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.0 3.5			4.5 4.0		4.5 4.0		ns

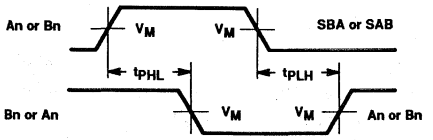
Note to AC setup requirements for 74F652A

1. Setup time is to protect against surge current caused by enabling 16 outputs (48mA per output) simultaneously.

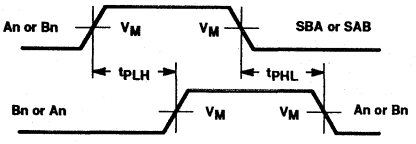
AC WAVEFORMS



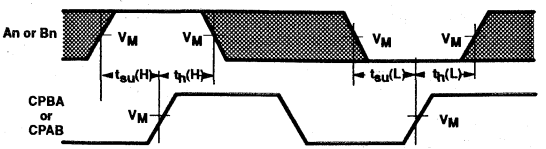
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



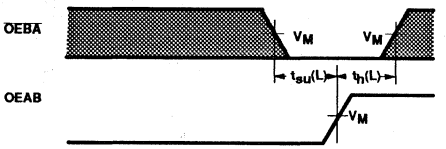
Waveform 2. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



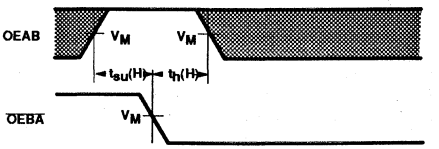
Waveform 3. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



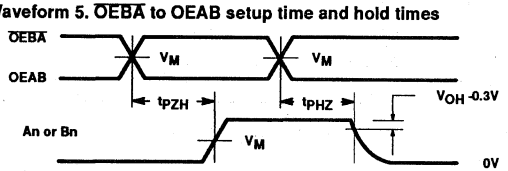
Waveform 4. Data setup time and hold times



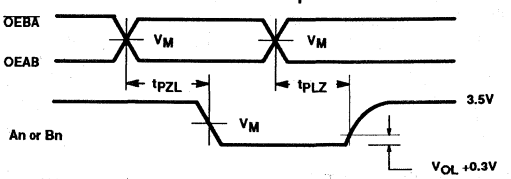
Waveform 5. $\overline{OEBA}$ to OEAB setup time and hold times



Waveform 6. OEAB to $\overline{OEBA}$ setup time and hold times



Waveform 7. 3-state output enable time to high level and output disable time from high level



Waveform 8. 3-state output enable time to low level and output disable time from low level

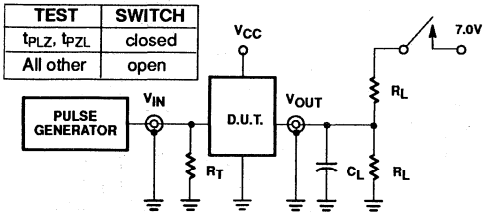
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



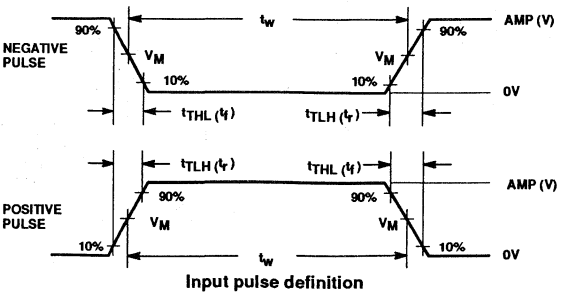
Test circuit for 3–state outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0085
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Date of issue	February 4, 1989
Status	Product Specification
FAST Products	

FAST 74F653, 74F654 Transceivers/Registers

'F653 Octal Transceiver/Register, Inverting (3-state +Open Collector)
'F654 Octal Transceiver/Register, Non-Inverting (3-state +Open Collector)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F653	90MHz	140mA
74F654	90MHz	140mA

FEATURES

- **High impedance NPN base inputs for redued loading (70µA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-state outputs (B_0-B_7) or Open-Collector outputs (A_0-A_7)**

DESCRIPTION

The 74F653 and 74F654 Transceivers/Registers consist of bus transceiver circuits with 3-state (B_0-B_7) or open collector (A_0-A_7)outputs , D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

ORDERING INFORMATION

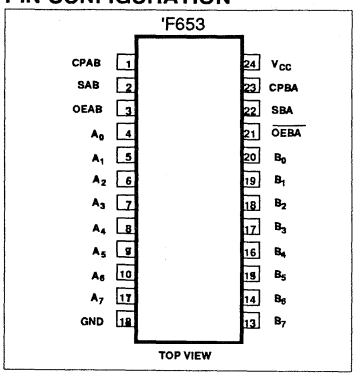
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Cerdip (300mil)	N74F653F, N74F654F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

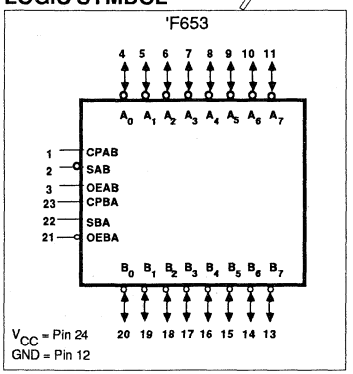
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	1.0/0.033	20µA/20µA
B_0 - B_7	B inputs	3.5/0.116	70µA/70µA
CPAB	A-to-B clock input	1.0/0.033	20µA/20µA
CPBA	B-to-A clock input	1.0/0.033	20µA/20µA
SAB	A-to-B select input	1.0/0.033	20µA/20µA
SBA	B-to-A select input	1.0/0.033	20µA/20µA
OEAB	A-to-B output enable input	1.0/0.033	20µA/20µA
$\overline{OEBA}$	B-to-A output enable input	1.0/0.033	20µA/20µA
A_0 - A_7	A outputs	OC /106.7	OC /64mA
B_0 - B_7	B outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

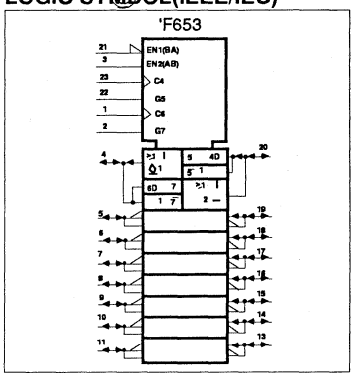
PIN CONFIGURATION



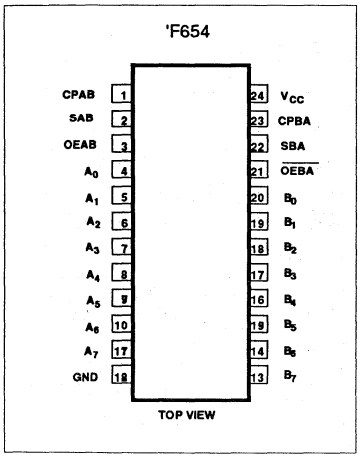
LOGIC SYMBOL



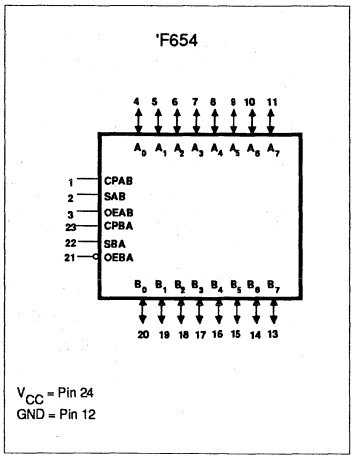
LOGIC SYMBOL(IEEE/IEC)



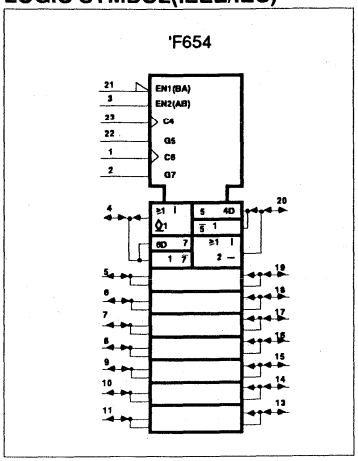
PIN CONFIGURATION



LOGIC SYMBOL

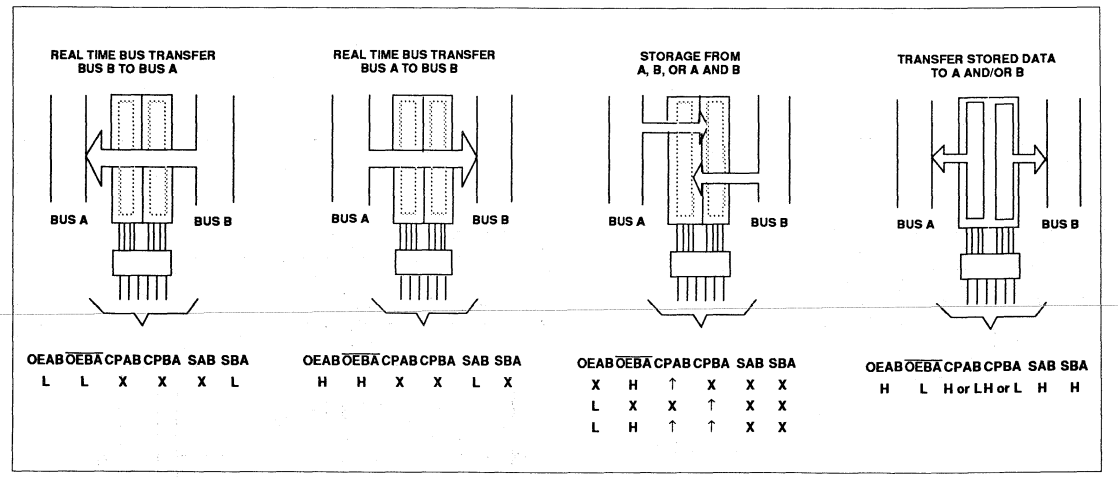


LOGIC SYMBOL(IEEE/IEC)



The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F653 and 'F654. The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.

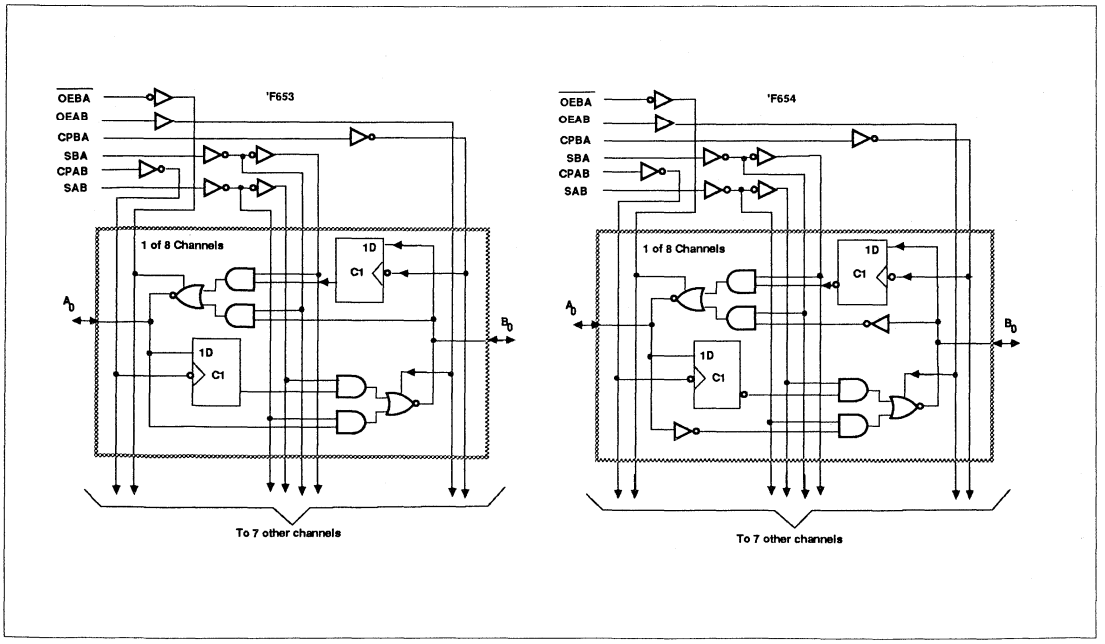


FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_n	B_n	'F653	'F654
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, Hold B	Store A, Hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
								Stored $\overline{B}$ data to A bus	Stored B data to A bus

H= High voltage level
L= Low voltage level
*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ =Low-to-High clock transition
X=Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage	A_0 - A_7			4.5	V
I_{OH}	High-level output current	A_0 - A_7			-3	mA
		B_0 - B_7			-15	mA
I_{OL}	Low-level output current				64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA SAB, SBA A_0-A_7	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{IH}+I_{OZH}	Off-state current High-level voltage applied	B_0-B_7	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]	B_0-B_7	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				110 140[4]	160 185[4]	mA
		I_{CCL}					140 160[4]	210 240[4]	mA
		I_{CCZ}					130	175	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. When using worst case conditions thermal mounting is required.

AC ELECTRICAL CHARACTERISTICS

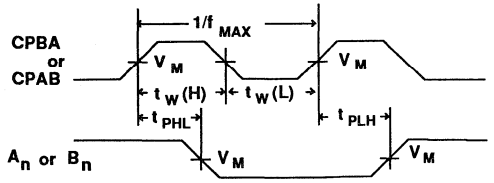
SYMBOL	PARAMETER		TEST CONDITION	74F653, 74F654					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	A_0-A_7	Waveform 1	55	70		45		MHz
		B_0-B_7		100	115		85		
t_{PLH} t_{PHL}	Propagation delay CPBA to A_n		Waveform 1	6.0 6.0	14.5 8.0	19.0 11.0	5.5 5.5	21.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to B_n		Waveform 1	5.5 5.5	7.5 8.0	10.5 10.5	5.0 5.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 3, 4	4.5 4.5	14.0 7.0	18.5 10.0	4.0 4.0	20.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n		Waveform 3, 4	4.0 4.0	6.0 6.5	9.5 9.5	3.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n		Waveform 3, 4	5.0 5.0	15.0 7.5	18.5 10.5	4.5 4.5	21.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB to B_n		Waveform 3, 4	5.0 5.0	7.0 7.0	10.0 10.0	4.5 4.5	12.0 10.5	ns
t_{PLH} t_{PHL}	Output Enable and Disable time $\overline{OEBA}$ to A_n		Waveform 2	6.5 6.5	16.0 10.0	20.0 12.5	6.0 6.0	23.0 14.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB to B_n		Waveform 8 Waveform 9	4.5 6.0	6.5 8.0	9.5 11.0	4.0 5.5	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB to B_n		Waveform 8 Waveform 9	6.5 6.0	9.5 9.0	13.0 12.0	6.0 5.5	14.5 14.5	ns

AC SETUP REQUIREMENTS

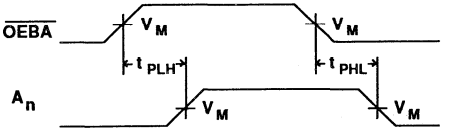
SYMBOL	PARAMETER	TEST CONDITION	74F653, 74F654					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 5	4.5 4.5			5.5 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 5	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low [1] $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 6, 7	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 6, 7	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	W aveform 1	4.5 6.5			4.5 6.5		ns

Note : 1. Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

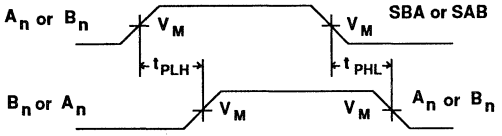
AC WAVEFORMS



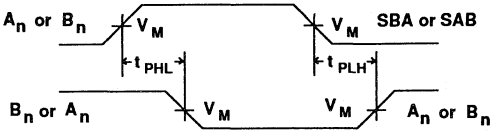
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



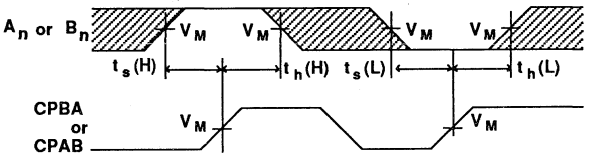
Waveform 2. Enable and Disable Times for Open Collector Outputs



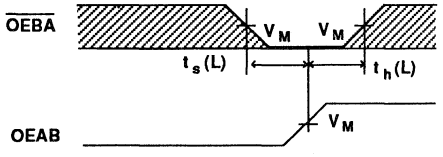
Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



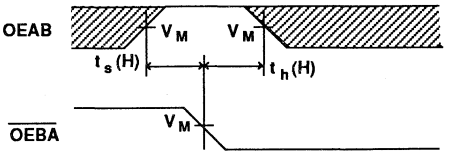
Waveform 4. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



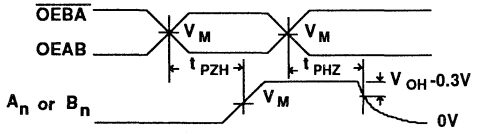
Waveform 5. Data Setup And Hold Times



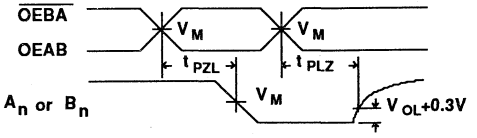
Waveform 6. $\overline{OEBA}$ to OEAB Setup And Hold Times



Waveform 7. OEAB to $\overline{OEBA}$ Setup And Hold Times



Waveform 8. 3-State Output Enable Time To High Level And Output Disable Time From High Level

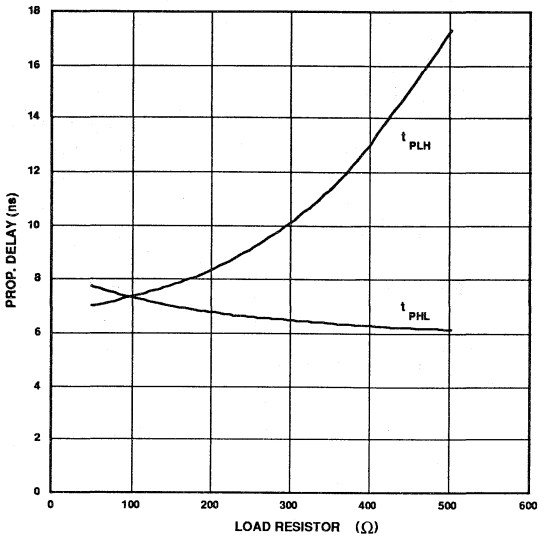


Waveform 9. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

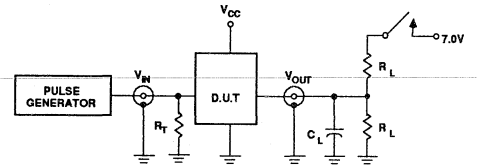
The shaded areas indicate when the input is permitted to change for predictable output performance.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

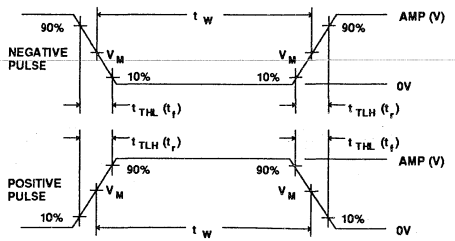


NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State and Open Collector Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Buffers/drivers

FAST 74F655A, 74F656A

74F655A Octal buffer/driver with parity, inverting (3-State); 74F656A Octal buffer/driver with parity, non-inverting (3-State)

FEATURES

- Significantly improved AC performance over 'F655 and 'F656
- High impedance NPN base inputs for reduced loading (40µA in High and Low states)
- Ideal in applications where high output drive and light bus loading are required (I_{IL} is 40µA vs FAST std of 600µA)
- 'F655A combines 'F240 and 'F280A functions in one package
- 'F656A combines 'F244 and 'F280A functions in one package
- 'F655A Inverting
- 'F656A Non-Inverting
- 3-state outputs sink 64mA and source 15mA
- 24-pin plastic Slim DIP (300mil) package
- Inputs on one side and outputs on the other side simplifies PC board layout
- Combined functions reduce part count and enhance system performance
- Industrial temperature range available (-40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F655A	6.5ns	64mA
74F656A	6.5ns	64mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10%, T_{amb} = -40°C to +85°C
24-Pin Plastic Slim DIP (300mil)	N74F655AN, N74F656AN	I74F655AN, I74F656AN
24-Pin Plastic SOL	N74F655AD, N74F656AD	I74F655AD, I74F656AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

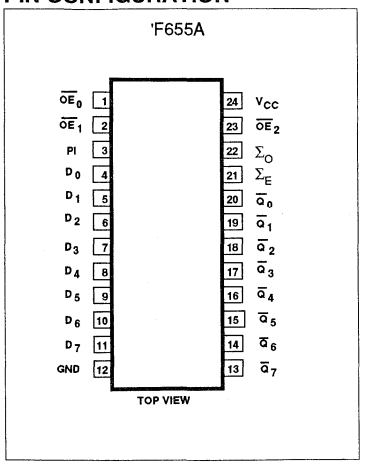
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0- D7	Data inputs	2.0/0.066	40µA/40µA
PI	Parity input	1.0/0.033	20µA/20µA
$\overline{OE}$0, $\overline{OE}$1, $\overline{OE}$2	Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
ΣE, ΣO	Parity outputs	750/106.7	15mA/64mA
$\overline{Q}$0- $\overline{Q}$7	Data outputs ('F655A)	750/106.7	15mA/64mA
Q0- Q7	Data outputs ('F656A)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

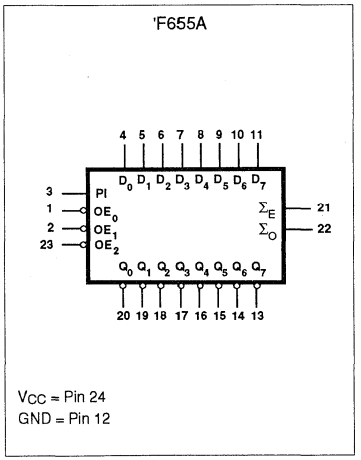
DESCRIPTION

The 74F655A and 74F656A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

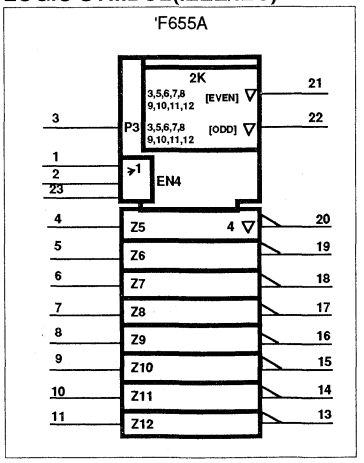
PIN CONFIGURATION



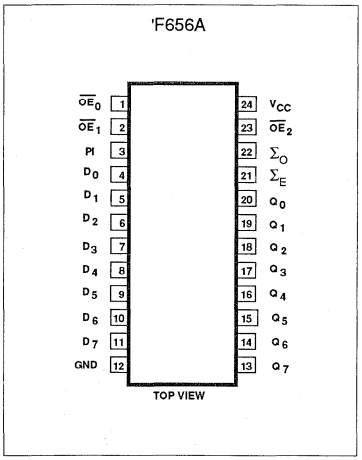
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION



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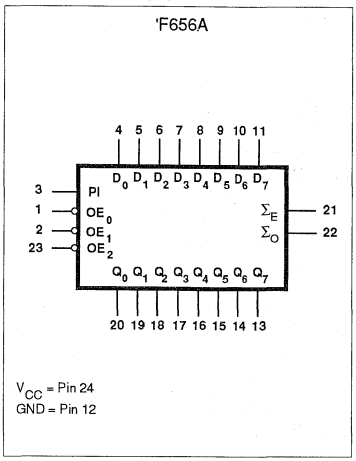
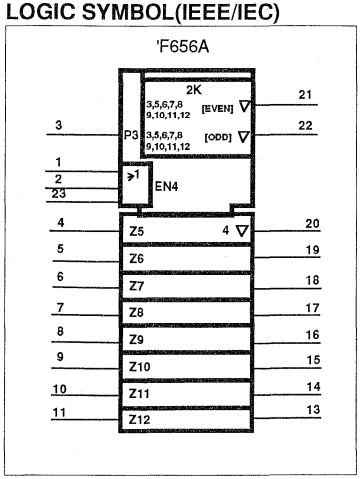


LOGIC SYMBOL(IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS	
				'F655A	'F656A
$\overline{OE}0$	$\overline{OE}1$	$\overline{OE}2$	Dn	$\overline{Q}n$	Qn
L	L	L	L	H	L
L	L	L	H	L	H
H	X	X	X	Z	Z
X	H	X	X	Z	Z
X	X	H	X	Z	Z

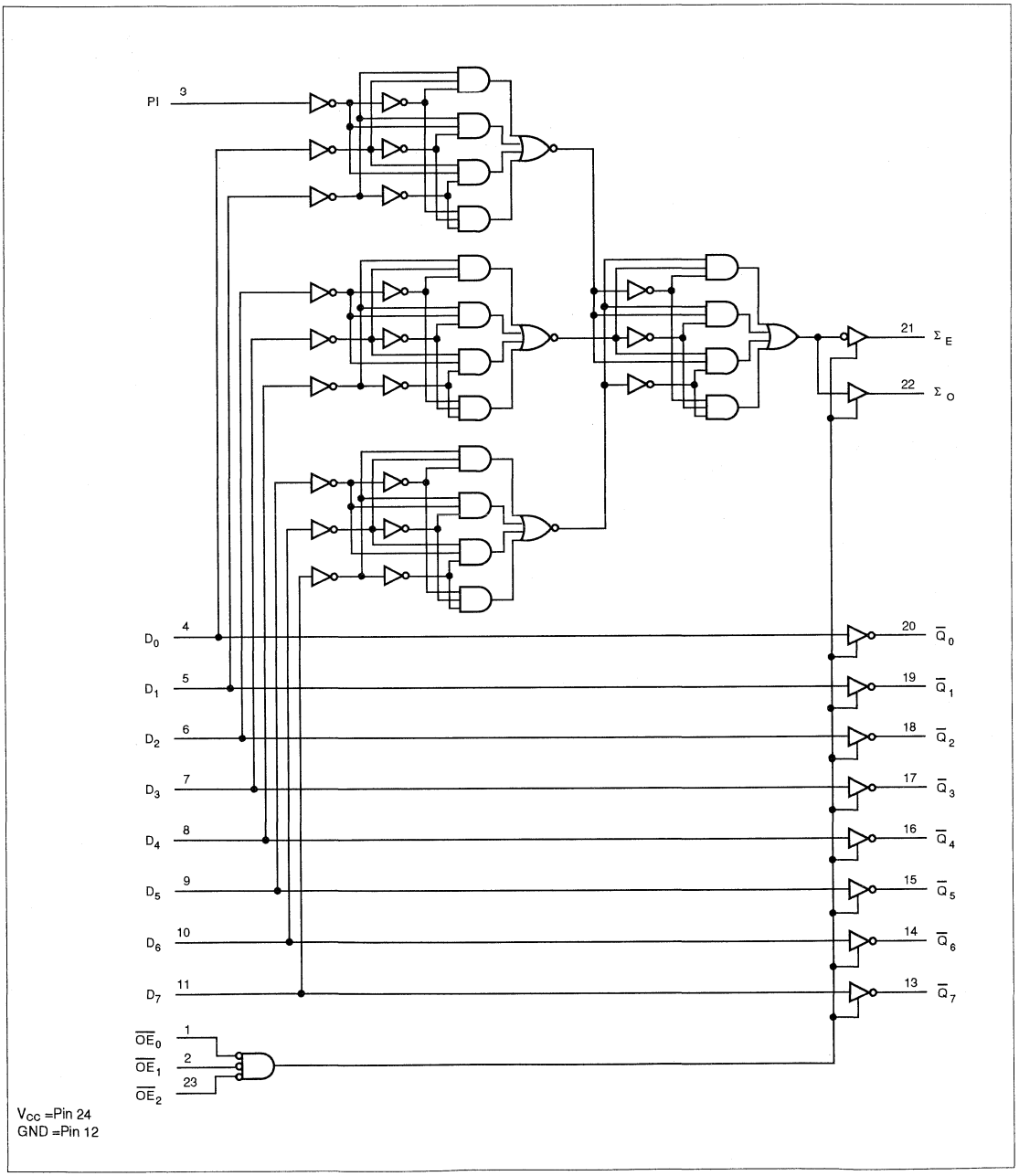
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

FUNCTION TABLE for PARITY OUTPUTS

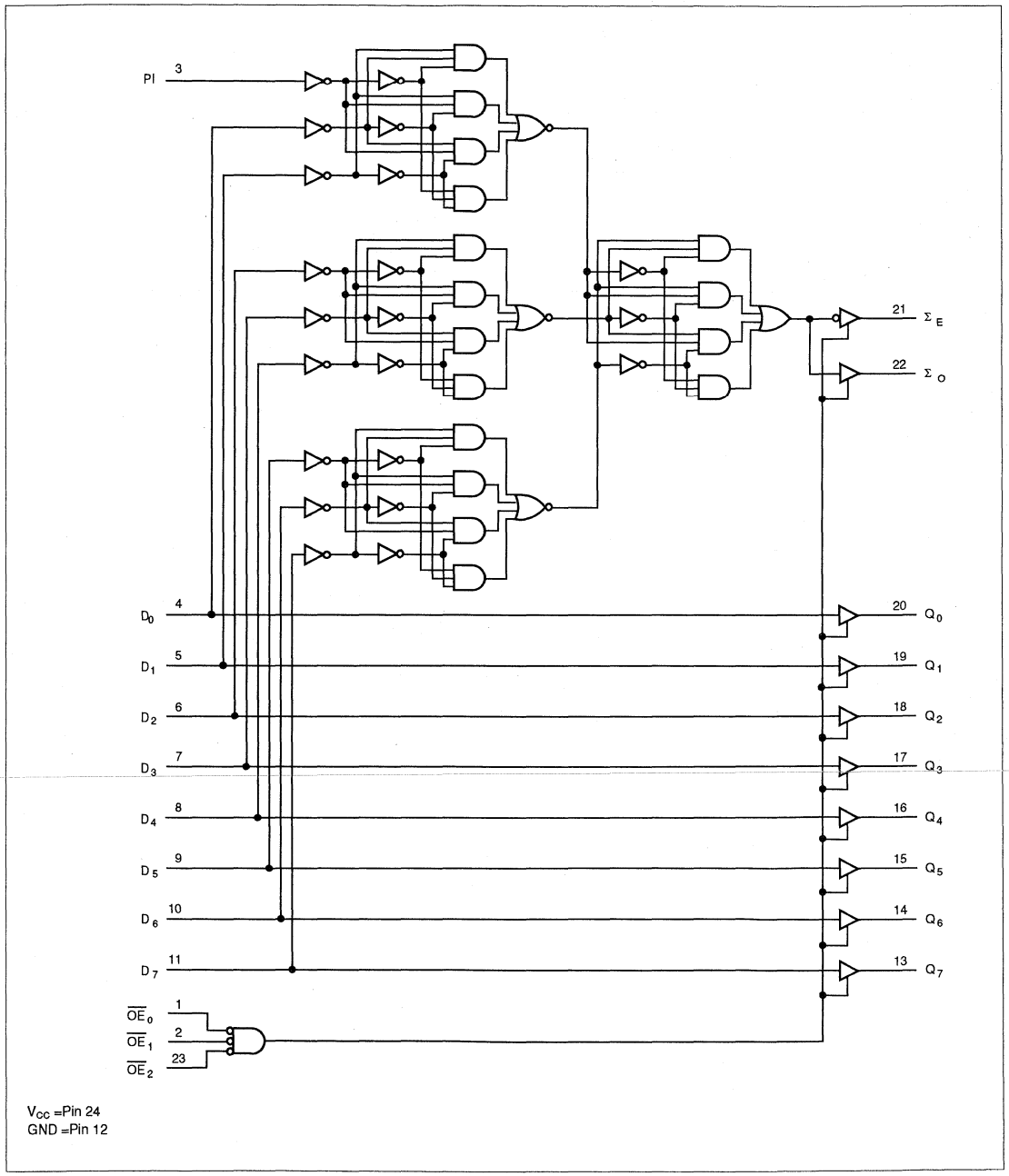
INPUTS	OUTPUTS	
Number of inputs High (PI, D0-D7)	ΣE	ΣO
Even ------ 0, 2, 4, 6, 8	H	L
Odd ------1, 3, 5, 7, 9	L	H
Any $\overline{OE}$n=High	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

LOGIC DIAGRAM for 'F655A



LOGIC DIAGRAM for 'F656A



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state		128	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current				64	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	-40		85	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
					I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=64mA	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level Input current	Commercial range	Dn	V_{CC} = MAX, V_I = 2.7V					40	µA
			PI, $\overline{OE}$n						20	µA
		Industrial range	Dn						80	µA
			PI, $\overline{OE}$n						40	µA
I_{IL}	Low-level input current		Dn	V_{CC} = MAX, V_I = 0.5V					-40	µA
			PI, $\overline{OE}$n						-20	µA
I_{OZH}	Off-state output current High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)		I_{CCH}	V_{CC} = MAX				50	80	mA
			I_{CCL}					78	110	mA
			I_{CCZ}					83	90	mA

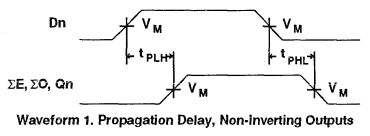
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

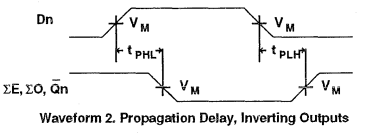
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS							UNIT
				T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_{amb} = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	'F655A	Waveform 2	2.0 1.0	4.5 2.5	6.5 4.0	2.0 1.0	7.5 4.5	2.0 1.0	8.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	'F656A	Waveform 1	2.0 2.5	4.0 5.5	6.5 7.0	2.0 2.5	7.0 7.5	2.0 2.5	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay Dn to ΣE , ΣO		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	4.5 5.5	16.5 18.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.5 4.0	7.0 8.0	10.5 11.0	3.5 4.0	11.5 12.0	3.0 4.0	13.0 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.5 5.0	8.0 8.0	1.5 2.0	9.0 9.0	1.5 1.5	10.0 10.0	ns

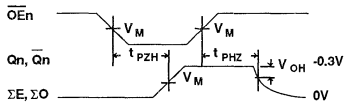
AC WAVEFORMS



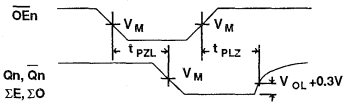
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs



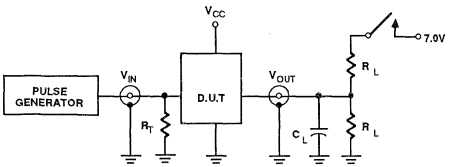
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

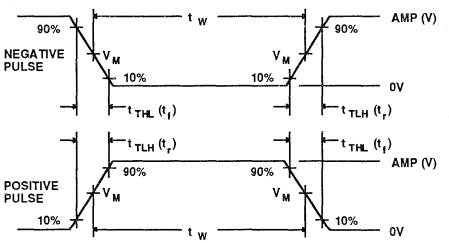
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal transceiver with 8-bit parity generator/checker — 74F657

Octal transceivers with 8–bit parity generator/checker

FEATURES

- Combines 74F245 and 74F280A functions in one package
- High impedance base input for reduced loading (70µA in high and low states)
- Ideal in applications where high output drive and light bus loading are required (I_{IL} is 70µA vs FAST std of 600µA)
- 3–state buffer outputs sink 64mA and source 15mA
- Input diodes for termination effects
- 24–pin plastic slim DIP (300mil) package
- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F657	8.0ns	100mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
24–pin plastic slim DIP (300mil)	N74F657N	I74F657N
24–pin plastic SOL[1]	N74F657D	I74F657D

Note to ordering information

1. Thermal mounting techniques are recommended. See SMD Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	A ports 3–state inputs	3.5/0.117	70µA/70µA
B0 – B7	B ports 3–state inputs	3.5/0.117	70µA/70µA
PARITY	Parity input	3.5/0.117	70µA/70µA
T/$\overline{R}$	Transmit/receive input	2.0/0.066	40µA/40µA
ODD/$\overline{EVEN}$	Parity select input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input (active low)	2.0/0.066	40µA/40µA
A0 – A7	A ports 3–state outputs	150/40	3.0mA/24mA
B0 – B7	B ports 3–state outputs	750/106.7	15mA/64mA
PARITY	Parity output	750/106.7	15mA/64mA
$\overline{ERROR}$	Error output	750/106.7	15mA/64mA

Note to input and output loading and fan out table

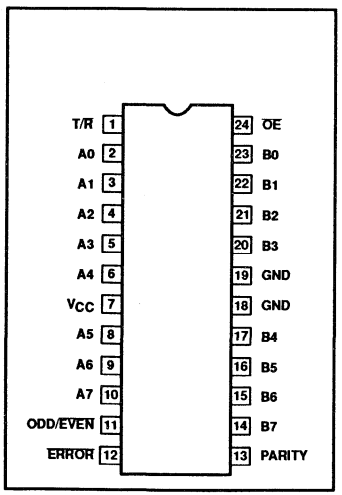
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

DESCRIPTION

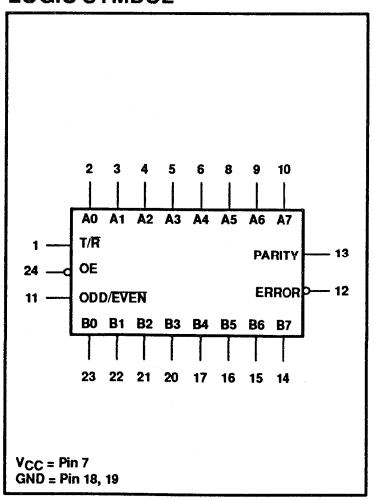
The 74F657 is an octal transceiver featuring non–inverting buffers with 3–state outputs and an 8–bit parity generator/checker, and is intended for bus–oriented applications. The buffers have a guaranteed current sinking capability of 24mA at the A ports and 64mA at the B ports. The transmit/receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers.

Transmit (active high) enables data from A ports to B ports; receive (active low) enables data from B ports to A ports. (continues)

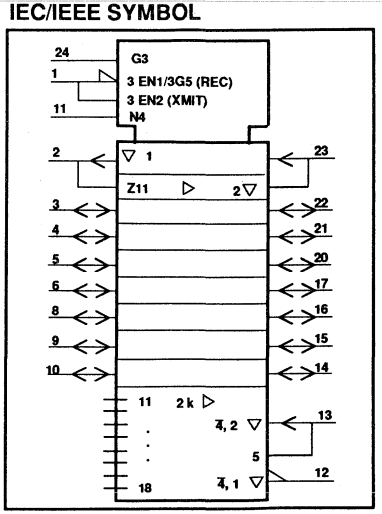
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



DESCRIPTION (CONTINUED)

The output enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is high.

The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems.

The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B (T/$\overline{R}$ = high) and an input when receiving from port B to A port (T/$\overline{R}$ = low).

When transmitting (T/$\overline{R}$ = high) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determined the number of high bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of high bits on port A.

For example, if the parity select (ODD/$\overline{EVEN}$) is set low (even parity), and the number of high bits on port A is odd, then the parity (PARITY) output will be high, transmitting even parity. If the number of high bits on port A is even, then the parity (PARITY) output will be low, keeping even parity.

When in receive mode (T/$\overline{R}$ = low) the B port is polled to determine the number of high bits. If parity select (ODD/$\overline{EVEN}$) is low (even parity) and the number of highs on port B is:

(1) odd and the parity (PARITY) input is high, then $\overline{ERROR}$ will be high, significantly no error.

(2) even and the parity (PARITY) input is high, then $\overline{ERROR}$ will be asserted low, indicating an error.

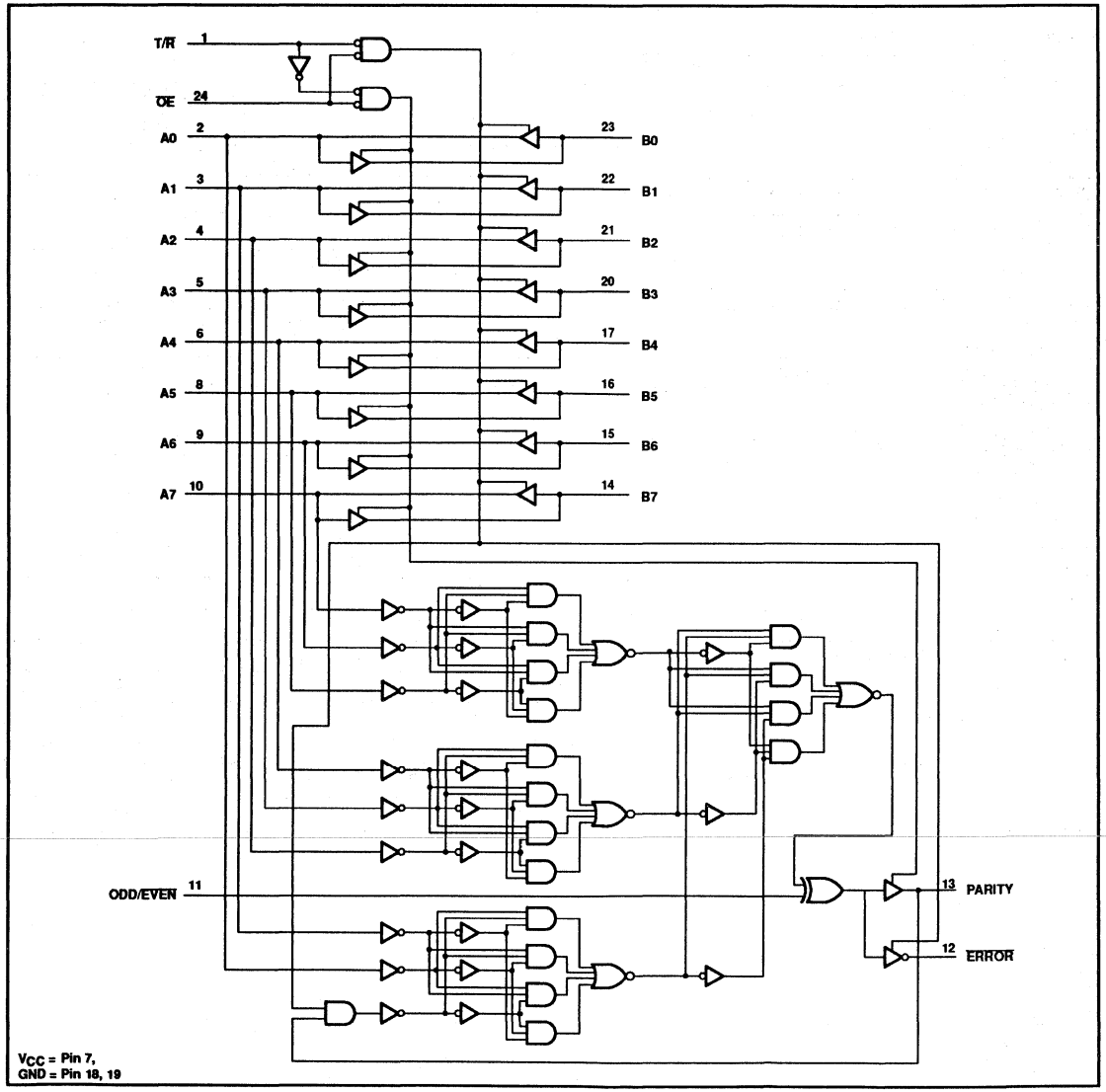
FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

Notes to function table

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "'off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	A0 – A7	48	mA
		B0 – B7, PARITY, $\overline{ERROR}$	128	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	A0 – A7			–3	mA
		B0 – B7, PARITY, $\overline{ERROR}$			–15	mA
I_{OL}	Low–level output current	A0 – A7			24	mA
		B0 – B7, PARITY, $\overline{ERROR}$			64	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	All outputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA[4,5]	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7			V
		B0 – B7, PARITY, $\overline{ERROR}$		I_{OH} = –12mA[5]	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
				I_{OH} = –15mA[4]	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0 – A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA[4,5]	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B0 – B7, PARITY, $\overline{ERROR}$		I_{OL} = 48mA[4]	±10%V_{CC}		0.38	0.55	V
				I_{OL} = 48mA[5]	±5%V_{CC}		0.42	0.55	V
				I_{OL} = 64mA[4]	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$, ODD/$\overline{EVEN}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0 – A7	V_{CC} = 5.5V, V_I = 5.5V					2	mA
		B0 – B7						1	mA
I_{IH}	High–level input current	OOD/$\overline{EVEN}$	V_{CC} = MAX, V_I = 2.7V					20[4]	µA
								40[5]	µA
		$\overline{OE}$, T/$\overline{R}$						40[4]	µA
								80[5]	µA
I_{IL}	Low–level input current	OOD/$\overline{EVEN}$	V_{CC} = MAX, V_I = 0.5V					–20	µA
		$\overline{OE}$, T/$\overline{R}$						–40	µA
I_{OZH} + I_{IH}	Off–state output current, high–level voltage applied	A0 – A7, B0 – B7, PARITY	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OZH}	Off–state output current, High–level voltage applied	$\overline{ERROR}$	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short circuit output current[3]	A0 – A7	V_{CC} = MAX			-60		-150	mA
		B0 – B7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	125[4]	mA
							90	135[5]	mA
		I_{CCL}					106	150[4]	mA
							106	160[5]	mA
		I_{CCZ}					98	145	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. For commercial range.
5. For industrial range.

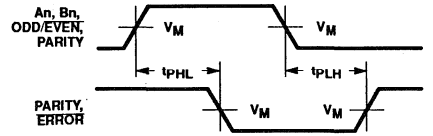
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.0 8.0	2.0 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	Waveform 1, 2	7.0 7.0	10.0 10.0	14.0 15.0	7.0 7.0	16.0 16.0	5.5 6.5	16.5 19.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/EVEN to PARITY, $\overline{\text{ERROR}}$	Waveform 1, 2	4.5 4.5	7.5 8.0	11.0 11.5	4.5 4.5	12.0 12.5	3.5 4.0	13.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay Bn to $\overline{\text{ERROR}}$	Waveform 1, 2	8.0 8.0	14.0 14.0	20.5 20.5	7.5 7.5	22.5 22.5	7.5 7.5	24.5 25.0	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{\text{ERROR}}$	Waveform 1, 2	8.0 8.0	11.5 12.0	15.5 15.5	7.5 8.0	16.5 17.0	6.5 6.5	18.5 20.0	ns
t_{PZH} t_{PZL}	Output enable time[1] to high or low level	Waveform 3, 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	2.0 4.0	9.0 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 3, 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	1.0 1.0	8.0 7.5	ns

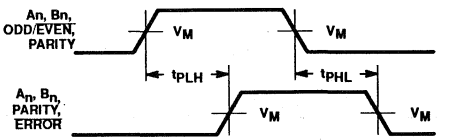
Note to AC electrical characteristics

1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$ output. VALID data at the $\overline{\text{ERROR}}$ pin ≥ (B to A) + (A to PARITY).

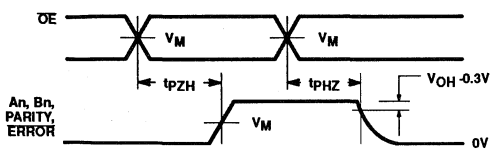
AC WAVEFORMS



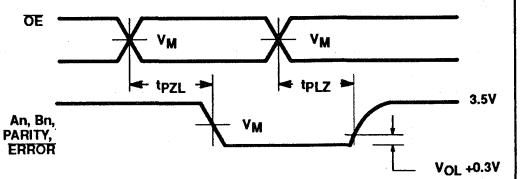
Waveform 1. Propagation delay for inverting outputs



Waveform 2. Propagation delay for non-Inverting outputs



Waveform 3. 3-state output enable time to high level and output disable time from high level



Waveform 4. 3-state output enable time to low level and output disable time from low level

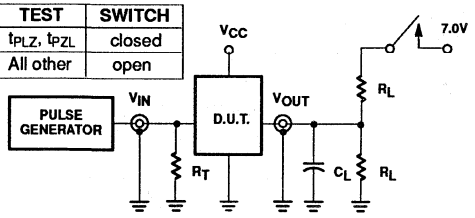
Note to AC waveforms

1. For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



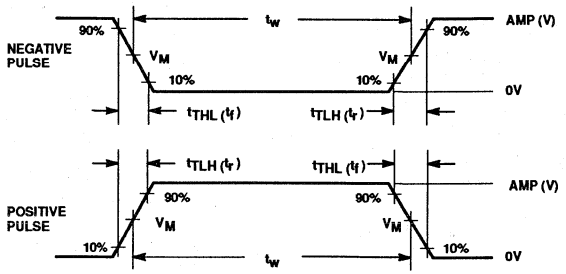
Test circuit for 3–state outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0014
ECN No.	99965
Date of issue	July 12, 1990
Status	Product Specification
FAST Products	

FAST 74F670
Register File

4 x 4 Register File (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F670	6.5ns	50mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F670N
16-Pin Plastic SOL	N74F670D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
W_A, W_B	Write address inputs	1.0/1.0	20µA/0.6mA
R_A, R_B	Read address inputs	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{RE}$	Read Enable inputs	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Data output	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

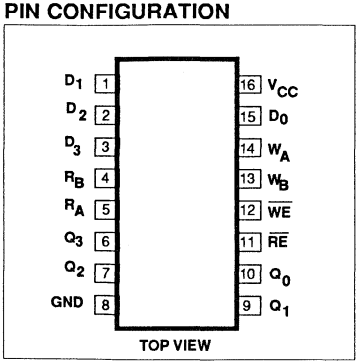
FEATURES

- **Simultaneous and independent Read and Write operations**
- **Expandable to almost any word size and bit length**
- **3-state outputs**

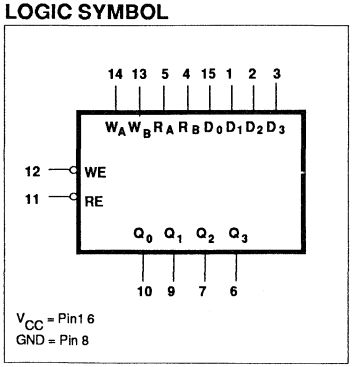
DESCRIPTION

The 74F670 is a 16 bit 3-state Register File organized as a 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs. The Write address inputs (W_A and W_B) determine the locatoion of the stored word. The Write Address inputs should only be changed when the Write Enable input ($\overline{WE}$) is High for conventional operation. When the $\overline{WE}$ is Low, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is Low. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs. Data and address inputs are inhibited when the $\overline{WE}$ is High. Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A, R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is Low. Data outputs are in the high impedance "off" state when the $\overline{RE}$ is High. This permits outputs to be tied together to increase the word capacity to very large numbers.

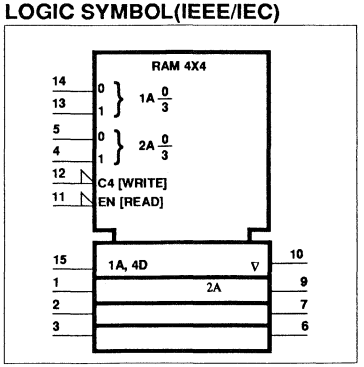
PIN CONFIGURATION



LOGIC SYMBOL

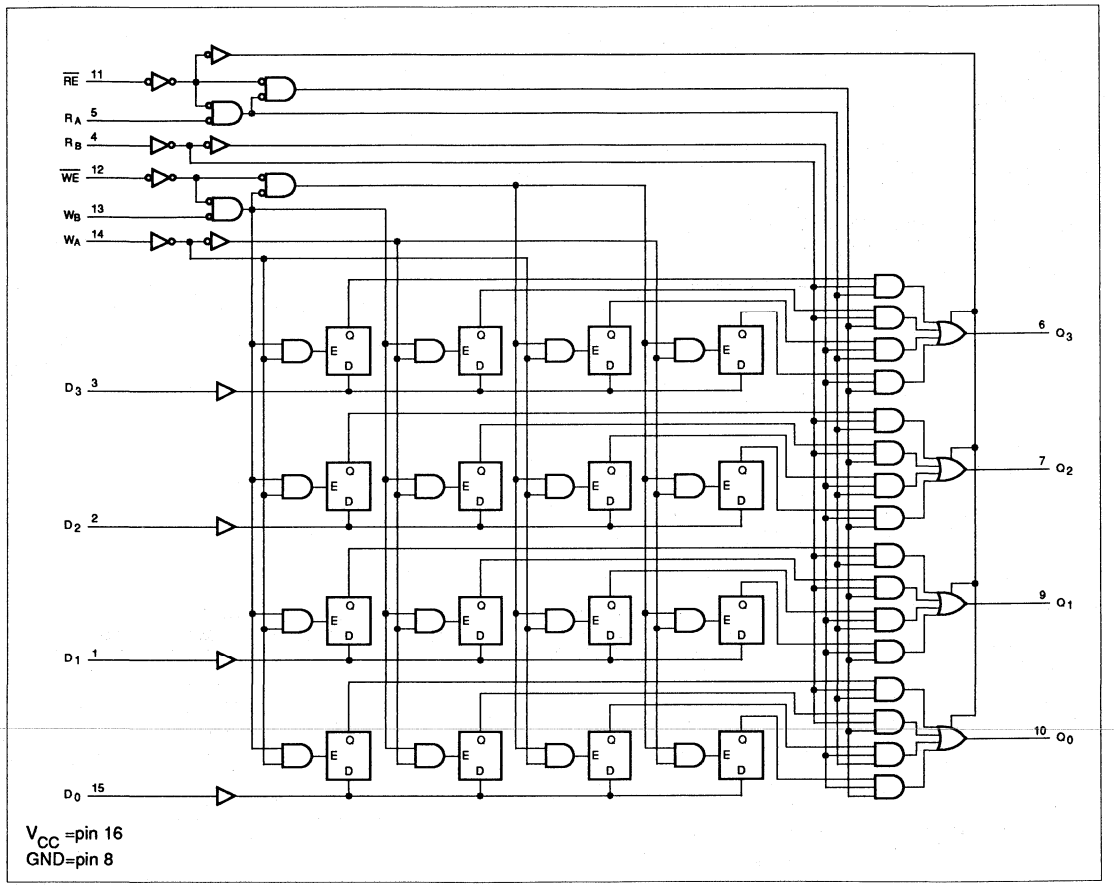


LOGIC SYMBOL(IEEE/IEC)



Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-state outputs together. Since the limiting factor for expansion is the output High current, further stacking is possible by tying pullup resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the Low levels which cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and address inputs of each device in parallel.

LOGIC DIAGRAM



WORD SELECT FUNCTION TABLE

WRITE MODE		READ MODE		OPERATING MODE
W_B	W_A	R_B	R_A	Word Selected
L	L	L	L	Word 0
L	H	L	H	Word 1
H	L	H	L	Word 2
H	H	H	H	Word 3

H = High voltage level
L = Low voltage level

WRITE MODE FUNCTION TABLE

INPUTS		INTERNAL LATCHES*	OPERATING MODE
$\overline{WE}$	D_n		
L	L	L	Write data
L	H	H	
H	X	NC	Data latched

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care

* = The write address (W_A and W_B) to the "internal latches" must be stabled while $\overline{WE}$ is Low for conventional operation.

READ MODE FUNCTION TABLE

INPUT	INTERNAL LATCHES*	OUTPUT	OPERATING MODE
$\overline{RE}$		Q_n	
L	L	L	Read
L	H	H	
H	X	Z	Disabled

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off " state

* = The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			50	70	mA
		I_{CCL}				50	70	mA
		I_{CCZ}				55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed lasty.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay R_A, R_B to Q_n	Waveform 2	3.5 4.0	5.5 5.5	9.0 8.5	3.0 3.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{WE}$ to Q_n	Waveform 1	5.0 6.5	7.0 8.5	10.0 11.5	4.5 6.0	11.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	3.5 6.0	6.0 8.0	8.5 11.0	3.0 5.5	9.5 12.5	ns
t_{PZH} t_{PZL}	$\overline{RE}$ Enable time Q_n to High or Low Level	Waveform 3 Waveform 4	3.0 4.5	7.0 6.5	12.0 9.0	2.5 4.0	13.0 10.0	ns
t_{PHZ} t_{PLZ}	$\overline{RE}$ Disable time Q_n to High or Low Level	Waveform 3 Waveform 4	2.0 3.0	3.0 5.0	6.5 8.5	1.5 3.0	7.5 8.5	ns

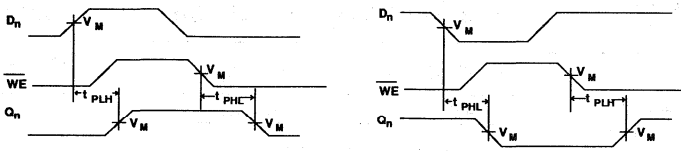
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to positive going $\overline{WE}$	Waveform 2	1.5 6.0			1.5 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to positive going $\overline{WE}$	Waveform 2	0 1.0			0 1.0		ns
t_s(H) t_s(L)	Setup time, High or Low W_A, W_B to negative going $\overline{WE}$[1]	Waveform 2	0 0			0 0		ns
t_h(H) t_h(L)	Hold time, High or Low W_A, W_B to negative going $\overline{WE}$[1]	Waveform 2	0 0			0 0		ns
t_w(L)	$\overline{WE}$ Pulse width, Low	Waveform 2	6.5			8.5		ns

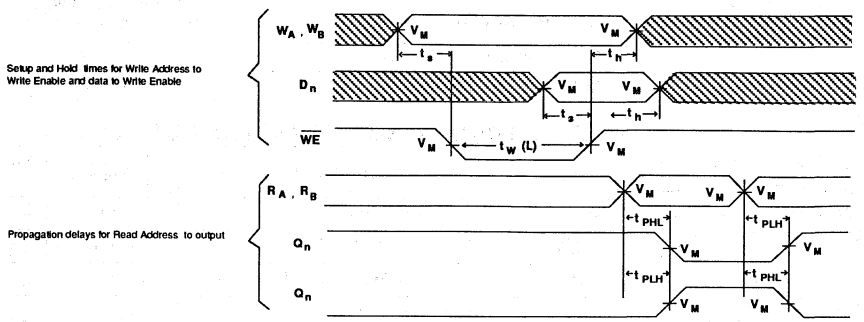
NOTES:

1. Write Address (W_A, W_B) setup time will protect the data written into the previous address. If protection of data in the previous address is not required, setup time for Write Address to $\overline{WE}$ can be ignored. Any address selection sustained for the final 7ns of the $\overline{WE}$ pulse during hold time for Write Address to $\overline{WE}$ will result in data being written into that location.

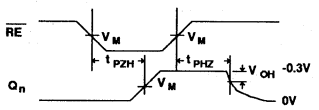
AC WAVEFORMS



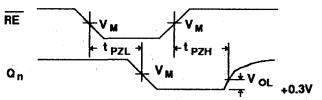
Waveform1. Propagation delay, Write Enable And Data To Outputs



Waveform 2. Setup and Hold Times, Write Address To Write Enable and Data To Write Enable And Propagation Delay Read Address To Output



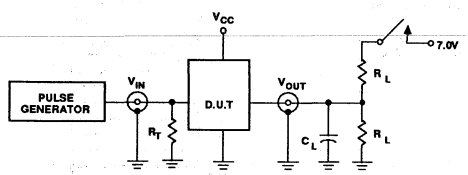
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

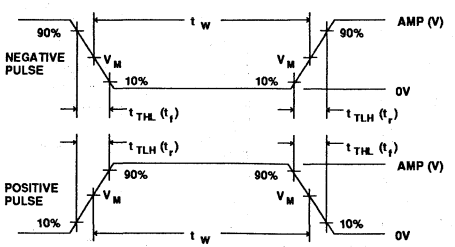
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-1248
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Date of issue	February 5, 1989
Status	Product Specification
FAST Products	

FAST 74F674
Shift Register

16-Bit Serial/Parallel-In, Serial-Out Shift Register (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F674	95MHz	55mA

FEATURES

- **16-bit serial I/O shift register**
- **16-bit parallel-in/serial-out converter**
- **Recirculating serial shifting**
- **Common serial data I/O pin (3-state)**

DESCRIPTION

The 74F674 is a 16 bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as 3-state serial output. In the serial out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility. The 'F674 operates in one of four modes, as indicated in the Function Table.

Hold : a High signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high impedance state.

ORDERING INFORMATION

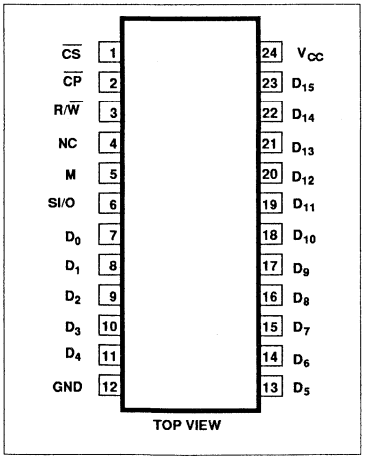
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F674N
24-Pin Plastic SOL	N74F674D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

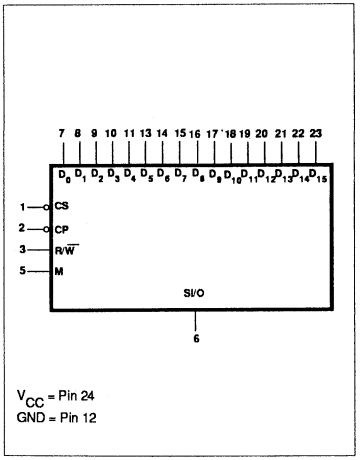
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 -D_{15}	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
M	Mode select input	1.0/1.0	20µA/0.6mA
R/$\overline{W}$	Read/Write input	1.0/1.0	20µA/0.6mA
SI/O	Serial data input or	3.5/1.0	70µA/0.6mA
	Serial 3-state output	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

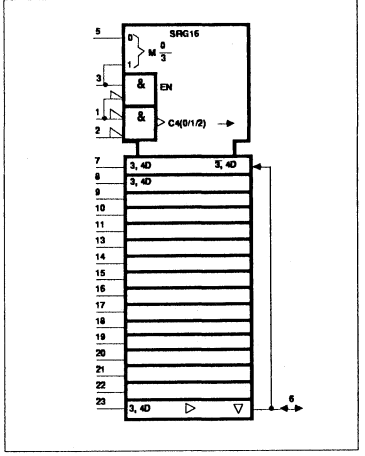
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Shift Register

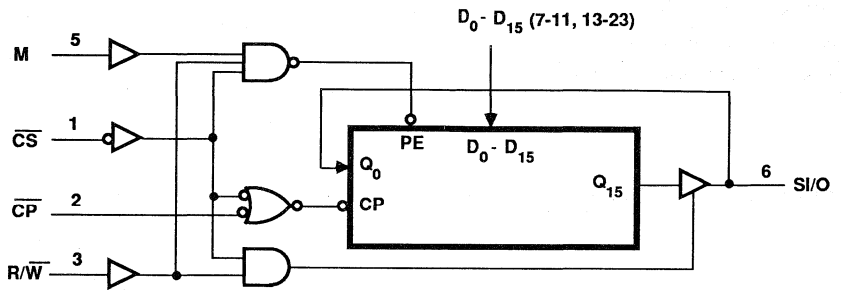
FAST 74F674

Serial load : data present on the SI/O pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks.

Serial output : the SI/O 3-state buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0.

Parallel load : data present on D_0- D_{15} is entered into the register on the falling edge of $\overline{CP}$. The SI/O 3-state buffer is active and represents the Q_{15} output. To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

LOGIC DIAGRAM



V_{CC} =pin 24
GND=pin 12

FUNCTION TABLE

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	M	$\overline{CP}$		
H	X	X	X	High Z	Hold
L	L	X	↓	Data in	Serial load
L	H	L	↓	Data out	Serial output with recirculation
L	H	H	↓	Active	Parallel load ; no shifting

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low transition of designated input

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	SI/O only	V_{CC} = MAX, V_I = 5.5V				100	µA
		others	V_{CC} = MAX, V_I = 7.0V					
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH} + I_{IH}	Off state output current, High-level voltage applied	SI/O only	V_{CC} =MAX, V_O=2.7V				70	µA
I_{OZL}+I_{IL}	Off state output current, Low-level voltage applied		V_{CC} =MAX, V_O=0.5V				-600	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

V_{OL} Low-level output voltage

V_{IK} Input clamp voltage V_{CC} = MIN, I_I = I_{IK}

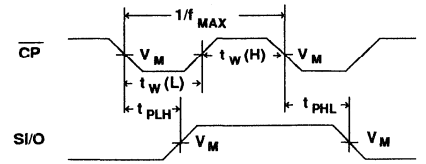
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frquency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SI/O	Waveform 1	7.0 6.0	9.5 8.5	12.5 11.5	6.5 5.5	14.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{CS}$ to SI/O	Waveform 3 Waveform 4	5.5 7.0	8.5 9.5	11.0 12.5	5.0 6.5	12.5 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{CS}$ to SI/O	Waveform 3 Waveform 4	3.0 4.5	6.0 7.5	8.5 10.0	3.0 4.5	10.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	6.0 7.5	8.5 10.0	11.5 13.0	5.5 7.0	13.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time	Waveform 3 Waveform 4	5.0 5.5	7.5 8.0	10.5 11.0	4.5 5.0	12.0 13.5	ns

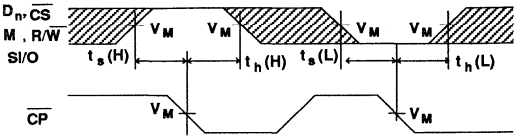
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low SI/O to $\overline{CP}$	Waveform 2	2.0 2.0			2.5 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low SI/O to $\overline{CP}$	Waveform 2	1.5 1.5			2.0 2.0		ns
t_s(H) t_s(L)	Setup time, High or Low D_n to $\overline{CP}$	Waveform 2	1.5 1.0			2.0 1.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to $\overline{CP}$	Waveform 2	3.0 4.0			3.0 4.0		ns
t_s(H) t_s(L)	Setup time, High or Low M to $\overline{CP}$	Waveform 2	2.0 5.5			2.5 6.0		ns
t_h(H) t_h(L)	Hold time, High or Low M to $\overline{CP}$	Waveform 2	0.0 0.0			1.0 1.0		ns
t_s(L)	Setup time, Low $\overline{CS}$ to $\overline{CP}$	Waveform 2	8.0			9.0		ns
t_h(H)	Hold time, High $\overline{CS}$ to $\overline{CP}$	Waveform 2	0.0			0.0		ns
t_w(H) t_w(L)	$\overline{CP}$ pulse width, High or Low	Waveform 1	3.5 4.5			4.0 5.0		ns

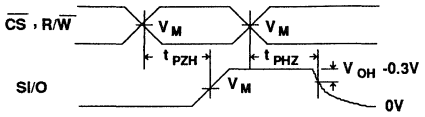
AC WAVEFORMS



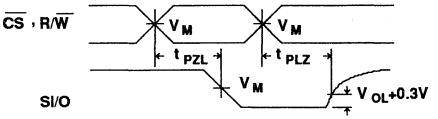
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Setup And Hold Times



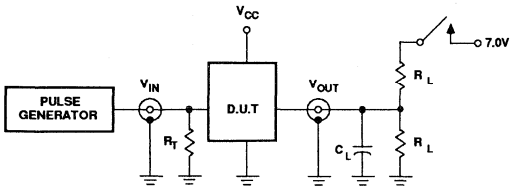
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

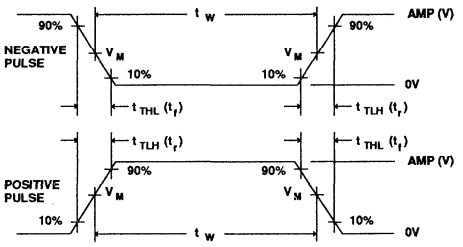
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors--Signetics

Document No.	853-0284
ECN No.	99394
Date of issue	April 18, 1990
Status	Product Specification
FAST Products	

FAST 74F676
Shift Register

16-Bit Serial/Parallel-In, Serial-Out Shift Register (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F676	110MHz	48mA

FEATURES

- **16-bit parallel-to-serial conversion**
- **16-bit serial-in, serial-out**
- **Chip select control**
- **Power supply current 48mA typical**
- **Shift frequency 110 MHz typical**
- **Available in 300mil-wide 24-pin Slim DIP package**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F676N
24-Pin Plastic SOL	N74F676D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_{15}	Parallel data inputs	1.0/1.0	20µA/0.6mA
SI	Serial data input	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
M	Mode select input	1.0/1.0	20µA/0.6mA
SO	Serial data output	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the mode (M) input is High, information present on the parallel data (D_0 - D_{15}) inputs is entered on the falling edge of the clock pulse ($\overline{CP}$) input signal. When M is Low, data is shifted out of the most significant bit position while information present on the serial (SI) input shifts into the least significant bit position. A High signal on the chip select ($\overline{CS}$) input prevents both parallel and serial operations. The 16 bit shift register operates in one of three modes, as indicated in the shift register Function Table.

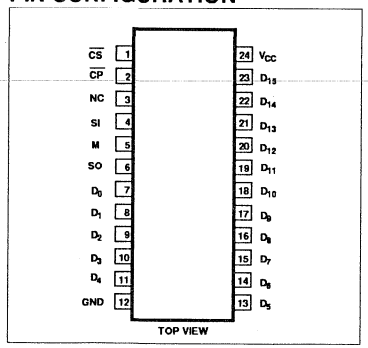
Hold : a High signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the 16 registers.

Shift/Serial load : data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks finally appearing on the SO pin.

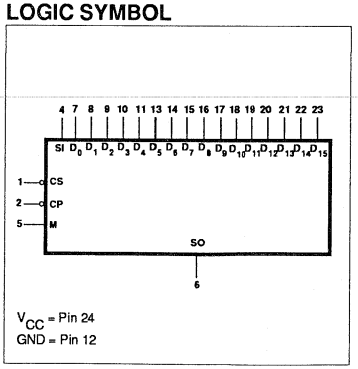
Parallel load : data present on D_0 - D_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

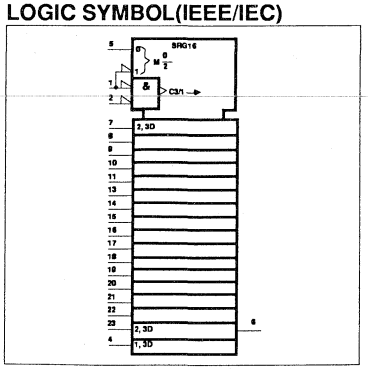
PIN CONFIGURATION



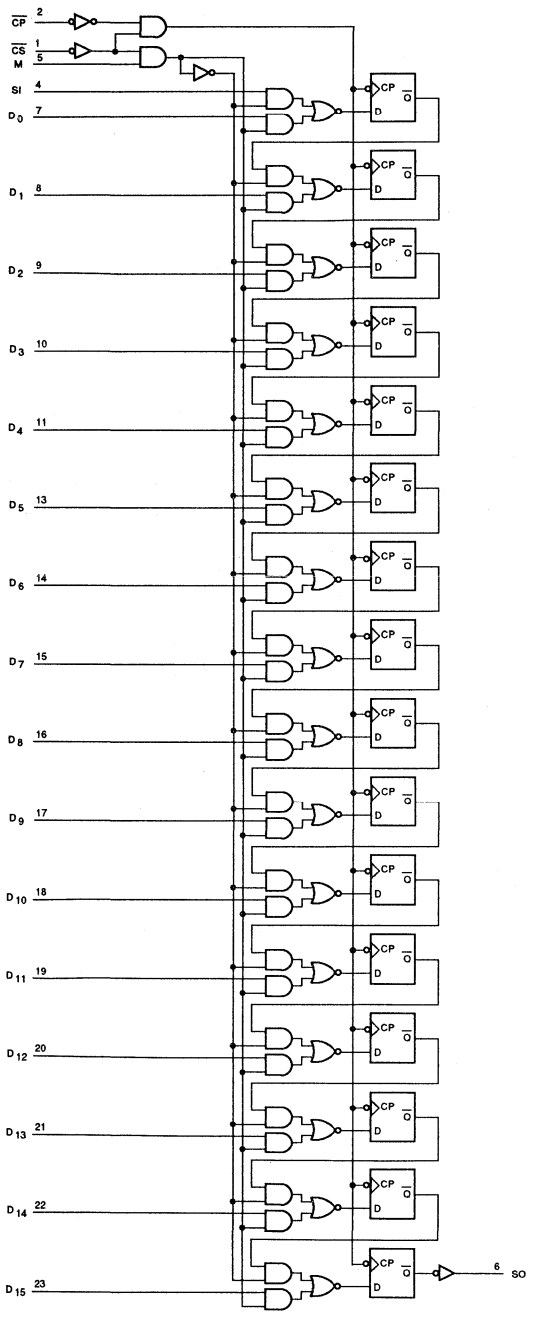
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} =pin 24
GND=pin 12

FUNCTION TABLE

CONTROL INPUTS			OPERATING MODE
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/Serial load
L	H	↓	Parallel load

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low transition of clock input

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			48	72	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

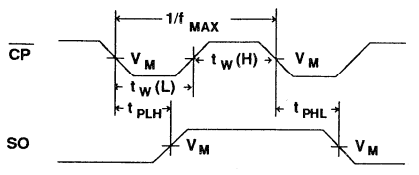
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	110		90		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SO	Waveform 1	4.5 5.0	8.0 7.0	11.0 12.5	4.5 5.0	12.0 13.5	ns

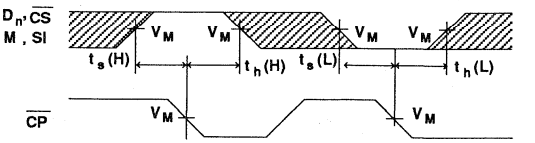
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{CP}$	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low M to $\overline{CP}$	Waveform 2	8.0 8.0			8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low M to $\overline{CP}$	Waveform 2	2.0 2.0			2.0 2.0		ns
$t_s(L)$	Setup time, Low $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		ns
$t_h(H)$	Hold time, High $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS



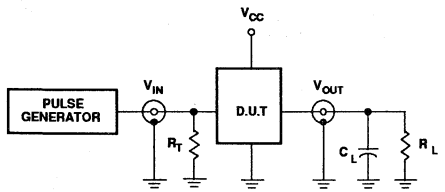
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



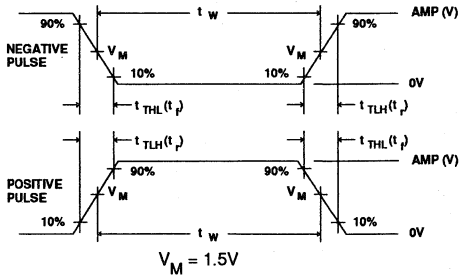
Waveform 2. Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1368
ECN No.	01258
Date of issue	December 13, 1990
Status	Product Specification
FAST Products	

FAST 74F711A/711-1, 74F712A/712-1 Multiplexers

74F711A Quint 2-to-1 Data Selector Multiplexer (3-State)
74F711-1Quint 2-to-1 Data Selector Multiplexer With 30 ohm Equivalent Output Termination Impedance (3-State)
74F712A Quint 3-to-1 Data Selector Multiplexer
74F712-1 Quint 3-to-1 Data Selector Multiplexer With 30 ohm Equivalent Output Termination Impedance

FEATURES for 74F711A/711-1

- **Consists of five 2-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **Output inverting/non-inverting option**
- **30 ohm termination impedance on each output-'F711-1**
- **Outputs sink 64mA ('F711A only)**

FEATURES for 74F712A/712-1

- **Consists of five 3-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **30 ohm termination impedance on each output-'F712-1**
- **Outputs sink 64mA ('F712A only)**

DESCRIPTION

The 74F711A/711-1 consist of five 2-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 'F711A has a common select (S) input, an Output Enable ($\overline{OE}$) input and an Output Inverting ($\overline{INV}$) input to control the 3-state outputs. The outputs source 15mA and sink 64mA. The 'F711-1 is the same as the 'F711A except that it has a 30 ohm termination impedance on each output to reduce line noise and the 3-state outputs sink 5mA.

When the inverting input ($\overline{INV}$) is Low, the input data path is inverted.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F711A	6.0ns	30mA
74F711-1	6.5ns	29mA
74F712A	5.5ns	25mA
74F712-1	6.5ns	25mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F711AN, N74F711-1N
24-Pin Plastic Slim DIP (300 mil)	N74F712AN, N74F712-1N
20-Pin Plastic SOL	N74F711AD, N74F711-1D
24-Pin Plastic SOL	N74F712AD, N74F712-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F711A/ 'F711-1	D_{na}, D_{nb}	Data inputs	1.0/0.066	20μA/40μA
	S	Select input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input (active Low)	1.0/0.033	20μA/20μA
	$\overline{INV}$	Output Inverting input (active Low)	1.0/0.033	20μA/20μA
	Q_0 - Q_4	Data outputs for 'F711A	750/106.7	15mA/64mA
	Q_0 - Q_4	Data outputs for 'F711-1	750/8.33	15mA/5mA
'F712A/ 'F712-1	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/0.066	20μA/40μA
	S_0, S_1	Select inputs	1.0/0.033	20μA/20μA
	Q_0 - Q_4	Data outputs for 'F712A	750/106.7	15mA/64mA
	Q_0 - Q_4	Data outputs for 'F712-1	750/8.33	15mA/5mA

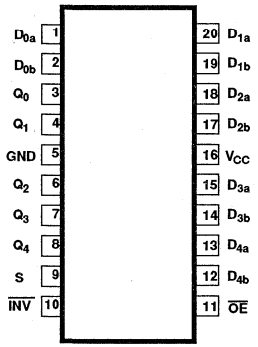
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

To improve speed and noise immunity, V_{CC} and GND side pins are used.

The 74F712A/712-1 consist of five 3-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 'F712A has two select (S_0,S_1) inputs to determine which set of five inputs will be propagated to the five outputs. The outputs source 15mA and sink 64mA. The 'F712-1 is the same as the 'F712A except that it has a 30 ohm termination impedance on each output to reduce line noise and the outputs sink 5mA.

PIN CONFIGURATION

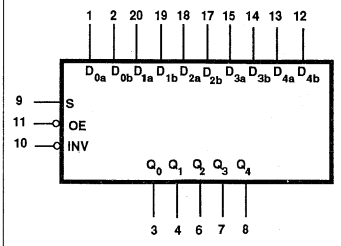
'F711A/'F711-1



TOP VIEW

LOGIC SYMBOL

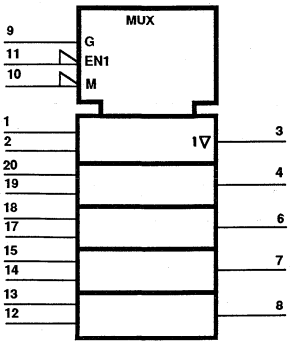
'F711A/'F711-1



V_{CC} = Pin 16
GND = Pin 5

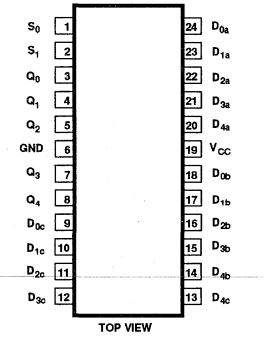
LOGIC SYMBOL(IEEE/IEC)

'F711A/'F711-1



PIN CONFIGURATION

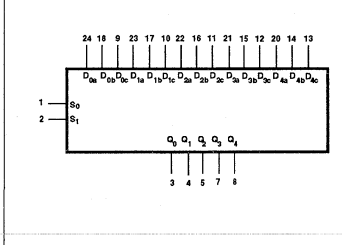
'F712A/'F712-1



TOP VIEW

LOGIC SYMBOL

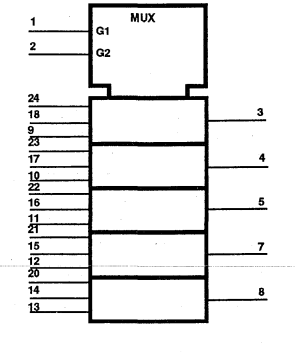
'F712A/'F712-1



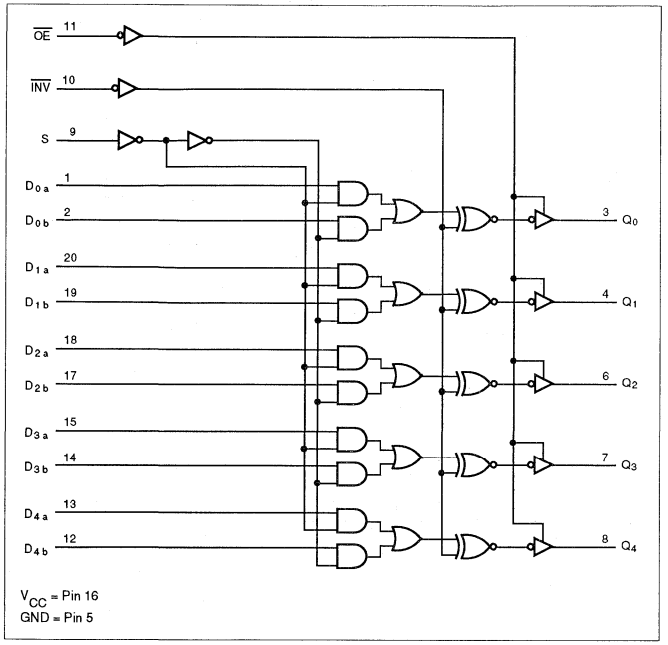
V_{CC} = Pin 19
GND = Pin 6

LOGIC SYMBOL(IEEE/IEC)

'F712A/'F712-1



LOGIC DIAGRAM for 'F711A/'F711-1

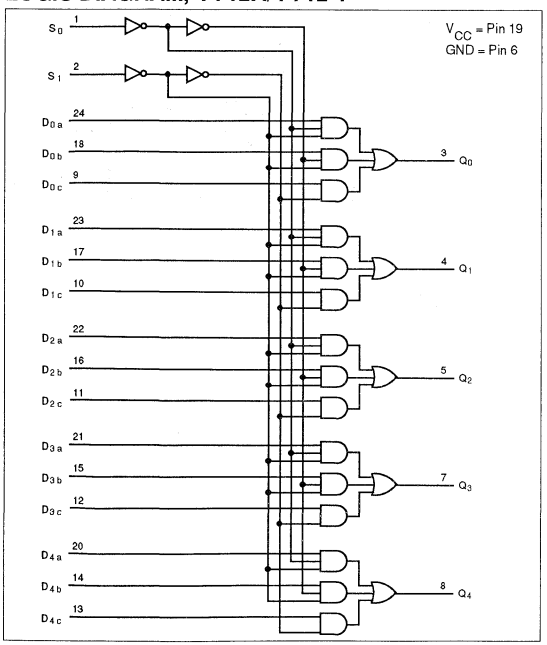


FUNCTION TABLE for 'F711A/'F711-1

INPUTS					OUTPUT
S	INV	OE	D_{na}	D_{nb}	Q_n
L	L	L	data a	data b	data a
H	L	L	data a	data b	data b
L	H	L	data a	data b	data a
H	H	L	data a	data b	data b
X	X	H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM, 'F712A/'F712-1



FUNCTION TABLE for 'F712A/'F712-1

INPUTS					OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	data a	data b	data c	data a
H	L	data a	data b	data c	data b
X	H	data a	data b	data c	data c

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	'F711A, 'F712A	96	mA
		'F711-1, 'F712-1	10	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OL}	High-level output current				-15	mA
I_{OL}	Low-level output current	'F711A, 'F712A			64	mA
		'F711-1, 'F712-1			5	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}= -3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH}= -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	'F711A/ 'F712A only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= MAX	±10%V_{CC}		0.38	0.55	V
				I_{OL}= 5mA	±5%V_{CC}		0.42	0.55	V
		'F711-1/ 'F712-1			±10%V_{CC}		0.38	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					-20	µA
		D_n only						-40	µA
I_{OZH}	Off-state output current High-level voltage applied	'F711A/ 'F711-1 only	V_{CC} = MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-50	µA
I_{OS}	Short circuit output current[3]	'F711-1/ 'F712-1	V_{CC} = MAX			-60		-150	mA
I_O	Output current[4]	'F711A/ 'F712A	V_{CC} = MAX, V_O= 2.25V			-60		-150	mA
I_{CC}	Supply current (total)	'F711A	I_{CCH}	V_{CC} = MAX			25	35	mA
			I_{CCL}				33	46	mA
			I_{CCZ}				27	40	mA
		'F711-1	I_{CCH}	V_{CC} = MAX			26	40	mA
			I_{CCL}				33	45	mA
			I_{CCZ}				28	45	mA
		'F712A	I_{CCH}	V_{CC} = MAX			20	27	mA
			I_{CCL}				30	40	mA
		'F712-1	I_{CCH}	V_{CC} = MAX			20	30	mA
			I_{CCL}				29	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

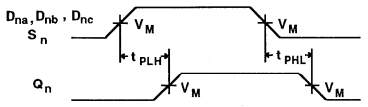
AC ELECTRICAL CHARACTERISTICS for 74F711A/74F711-1

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	74F711A	Waveform 1, 2	2.5 2.5	5.0 4.0	7.5 7.0	2.0 2.0	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S to Q_n		Waveform 1,3	7.0 5.0	9.0 8.0	12.0 11.0	5.5 4.5	13.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{INV}$ to Q_n		Waveform 1,3	6.0 4.0	9.0 8.0	12.5 11.0	5.0 3.5	14.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	2.5 2.5	4.0 4.5	6.5 7.0	2.0 2.0	7.0 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 8.0	2.0 2.5	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	74F711-1	Waveform 1, 2	3.0 2.0	4.5 4.5	7.5 7.5	2.0 2.5	9.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S, $\overline{INV}$ to Q_n		Waveform 1,3	6.5 4.5	10.0 8.5	13.5 11.5	5.5 4.0	14.5 12.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	9.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	2.0 3.5	4.5 5.5	7.0 8.5	2.0 3.0	8.0 9.5	ns

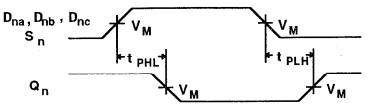
AC ELECTRICAL CHARACTERISTICS for 74F712A/74F712-1

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	74F712A	Waveform 1, 2	2.0 2.0	3.5 3.5	6.5 6.5	2.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n		Waveform 1	6.5 5.0	8.0 7.5	11.5 10.0	5.5 4.5	13.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	74F712-1	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n		Waveform 1	7.0 5.5	9.0 7.5	12.0 10.5	6.0 5.5	13.5 11.0	ns

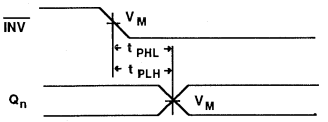
AC WAVEFORMS



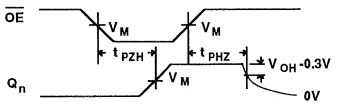
Waveform 1. Propagation Delay For Non-Inverting Output



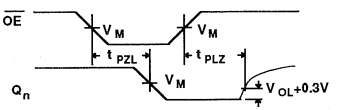
Waveform 2. Propagation Delay For Inverting Output



Waveform 3. Propagation Delay For $\overline{INV}$ To Output



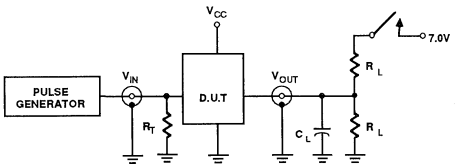
Waveform4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

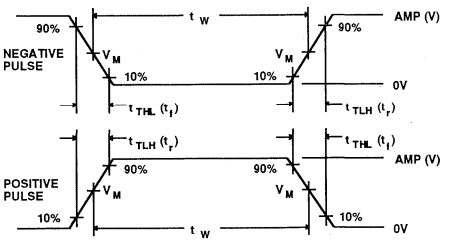
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

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ECN No.	01257
Date of issue	December 13, 1990
Status	Product Specification
FAST Products	

FAST 74F723A/723-1, 74F725A/725-1

Multiplexers

74F723A Quad 3-to-1 Data Selector Multiplexer (3-State)
74F723-1 Quad 3-to-1 Data Selector Multiplexer With 30 ohm Equivalent Output Termination Impedance (3-State)
74F725A Quad 4-to-1 Data Selector Multiplexer
74F725-1 Quad 4-to-1 Data Selector Multiplexer With 30 ohm Equivalent Output Termination Impedance

FEATURES for 74F723A/723-1

- **Consists of four 3-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **Inverting or non-inverting data path capability by an Inverting (INV) input**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **Multiple side pins for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)**
- **3-State outputs sink 64mA ('F723A only)**
- **30 ohm termination impedance on each output-74F723-1**

FEATURES for 74F725A/725-1

- **Consists of four 4-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **Equivalent to two 'F253s without 3-state**
- **Outputs sink 48mA ('F725A only)**
- **30 ohm termination impedance on each output-74F725-1**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F723A	5.5ns	25mA
74F723-1	7.0ns	26mA
74F725A	5.5ns	20mA
74F725-1	6.5ns	20mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F723AN, N74F723-1N, N74F725AN, N74F725-1N
24-Pin Plastic SOL	N74F723AD, N74F723-1D, N74F725AD, N74F725-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F723A/ 'F723-1	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/0.066	20μA/40μA
	S_0, S_1	Select inputs	1.0/0.033	20μA/20μA
	INV	Output Inverting input	1.0/0.033	20μA/20μA
	OE	Output Enable input	1.0/0.033	20μA/20μA
'F723A	Q_0 - Q_3	Data outputs	750/106.7	15mA/64mA
'F723-1	Q_0 - Q_3	Data outputs	750/8.33	15mA/5mA
'F725A/ 'F725-1	D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/0.066	20μA/40μA
	S_0, S_1	Select inputs	1.0/0.033	20μA/20μA
'F725A	Q_0 - Q_3	Data outputs	750/106.7	15mA/64mA
'F725-1	Q_0 - Q_3	Data outputs	750/8.33	15mA/5mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

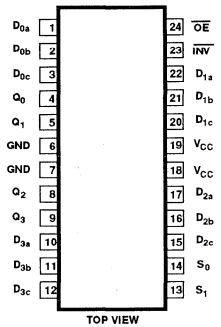
The 74F723A/723-1 consist of four 3-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. Select (S_0,S_1) inputs control which line is to be selected, as defined in the Function Table for 'F723A/723-1. When the inverting input (INV) is Low, the input data path is inverted.

To improve speed and noise immunity, V_{CC} and GND side pins are used. The 3-state outputs source 15mA and sink 64mA. The 74F723-1 is the same as 74F723A except that it has a 30 ohm termination impedance on each output to reduce line noise and the 3-state outputs sink 5mA.

The 74F725A/725-1 consist of four 4-to-1 multiplexers designed for general multiplexing purpose. The select (S_0,S_1) inputs control which line is to be selected, as defined in the Function Table for 'F725A/725-1. The outputs source 15mA and sink 64mA. The 74F725-1 is the same as the 74F725A except that it has a 30 ohm termination impedance on each output to reduce line noise and the outputs sink 5mA.

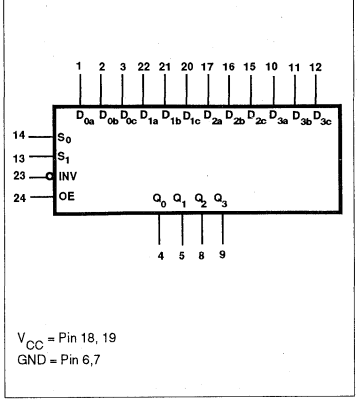
PIN CONFIGURATION

'F723A/'F723-1



LOGIC SYMBOL

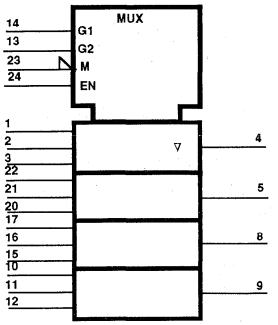
'F723A/'F723-1



V_{CC} = Pin 18, 19
GND = Pin 6,7

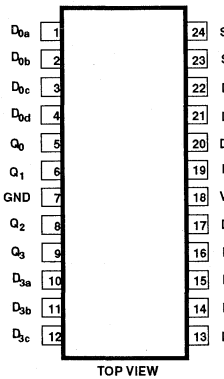
LOGIC SYMBOL(IEEE/IEC)

'F723A/'F723-1



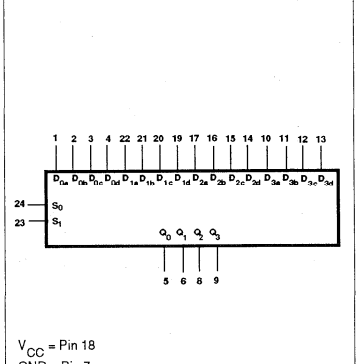
PIN CONFIGURATION

'F725A/'F725-1



LOGIC SYMBOL

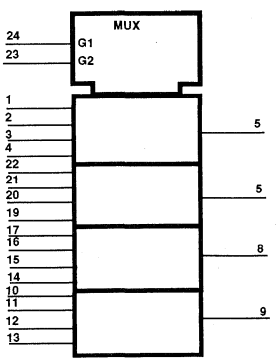
'F725A/'F725-1



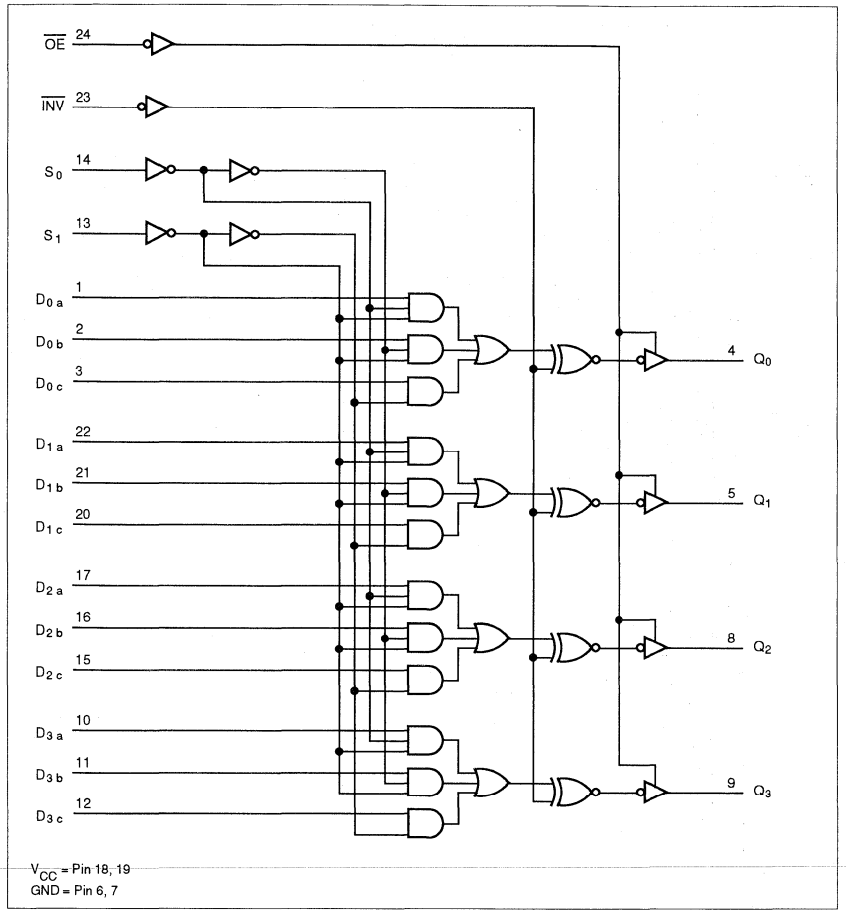
V_{CC} = Pin 18
GND = Pin 7

LOGIC SYMBOL(IEEE/IEC)

'F725A/'F725-1



LOGIC DIAGRAM for 'F723A/'F723-1

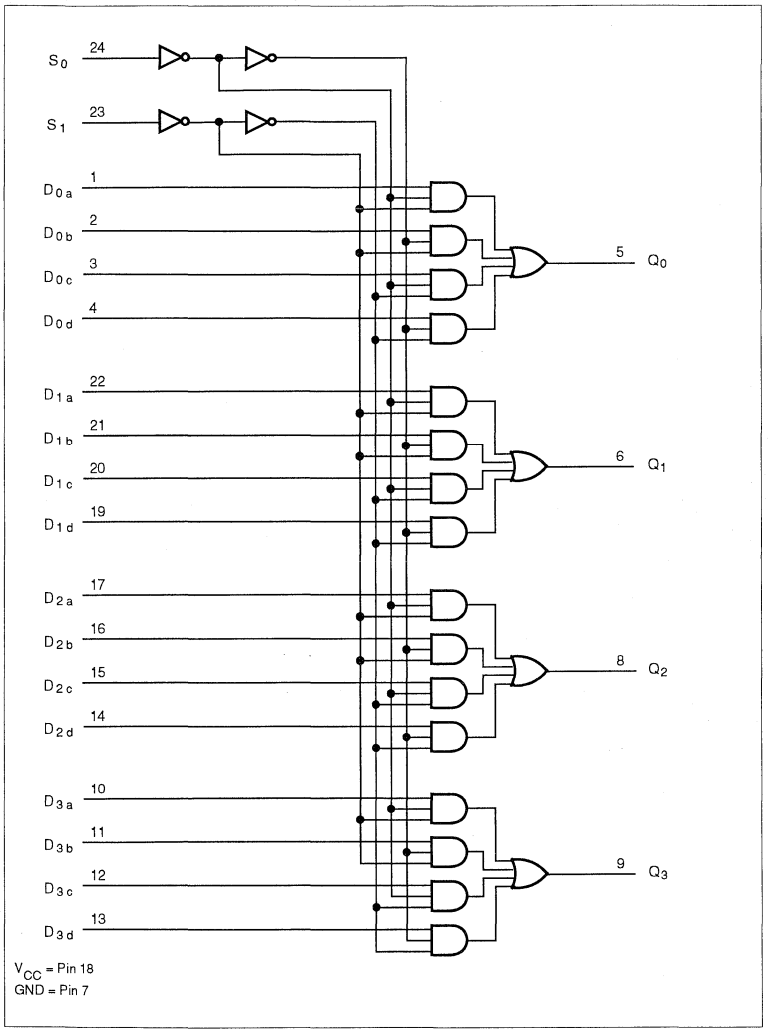


FUNCTION TABLE for 'F723A/'F723-1

INPUTS							OUTPUT
S_0	S_1	INV	OE	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	L	L	data a	data b	data c	data a
L	L	H	L	data a	data b	data c	data a
H	L	L	L	data a	data b	data c	data b
H	L	H	L	data a	data b	data c	data b
X	H	L	L	data a	data b	data c	data c
X	H	H	L	data a	data b	data c	data c
X	X	X	H	X	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM for 'F725A/'F725-1



FUNCTION TABLE for 'F725A/'F725-1

INPUTS						OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	D_{nd}	Q_n
L	L	data a	data b	data c	data d	data a
H	L	data a	data b	data c	data d	data b
L	H	data a	data b	data c	data d	data c
H	H	data a	data b	data c	data d	data d

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	'F723-1, 'F725-1	10	mA
		'F723A, 'F725A	96	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	'F723-1, 'F725-1			5	mA
		'F723A, 'F725A			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	'F723-1/ 'F725-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= 5mA	±10%V_{CC}		0.38	0.50	V
					±5%V_{CC}		0.38	0.50	V
		'F723A/ 'F725A		I_{OL}= MAX	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V					-20	µA
		D_n only						-40	µA
I_{OZH}	Off-state output current High-level voltage applied	'F723/ 'F723-1 only	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short circuit output current[3]	'F723-1/ 'F725-1	V_{CC} = MAX			-60		-150	mA
I_O	Output current[4]	'F723A/ 'F725A	V_{CC} = MAX, V_O = 2.25V			-60		-150	mA
I_{CC}	Supply current (total)	'F723A	I_{CCH}	V_{CC} = MAX			23	30	mA
			I_{CCL}				29	40	mA
			I_{CCZ}				25	40	mA
		'F723-1	I_{CCH}	V_{CC} = MAX			23	35	mA
			I_{CCL}				29	40	mA
			I_{CCZ}				26	40	mA
		'F725A	I_{CCH}	V_{CC} = MAX			16	25	mA
			I_{CCL}				24	35	mA
		'F725-1	I_{CCH}	V_{CC} = MAX			17	25	mA
			I_{CCL}				25	35	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

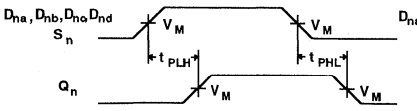
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	'F723A	Waveform 1, 2	2.5 2.0	5.0 4.5	8.0 7.0	2.0 2.0	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1, $\overline{INV}$ to Q_n		Waveform 1, 2	6.5 4.0	9.0 7.5	12.5 11.0	4.0 3.5	14.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$-to Q_n		Waveform 4 Waveform 5	2.0 2.5	4.0 4.5	6.5 7.0	2.0 2.0	7.5 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$-to Q_n		Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 7.5	2.0 2.5	7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	'F723-1	Waveform 1, 2	2.5 2.5	6.0 5.0	8.5 8.0	2.5 2.0	9.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1, $\overline{INV}$ to Q_n		Waveform 1, 2	7.0 5.0	10.0 9.0	14.0 12.5	6.0 4.5	16.0 13.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$-to Q_n		Waveform 4 Waveform 5	3.0 3.0	4.5 5.0	7.5 7.5	2.5 3.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$-to Q_n		Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	7.0 8.5	2.0 3.0	8.0 9.5	ns

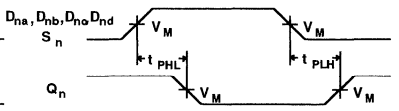
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to Q_n	'F725A	Waveform 1, 2	2.0 2.0	3.5 3.5	6.5 6.5	2.0 2.0	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n		Waveform 1	6.0 5.0	8.5 7.0	11.5 10.0	5.5 4.5	13.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to Q_n	'F725-1	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 6.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n		Waveform 1	6.5 5.0	9.0 8.5	12.0 10.5	5.5 5.0	14.0 11.0	ns

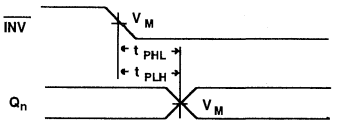
AC WAVEFORMS



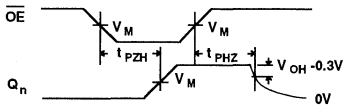
Waveform 1. Propagation Delay For Non-Inverting Output



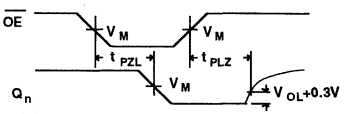
Waveform 2. Propagation Delay For Inverting Output



Waveform 3. Propagation Delay For $\overline{INV}$ To Output



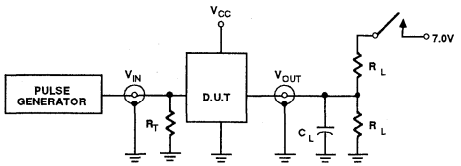
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

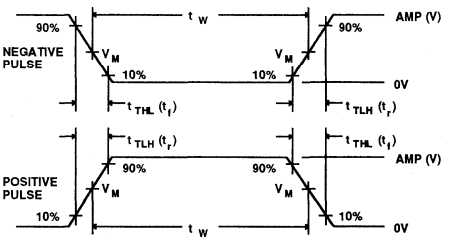
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0097
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Date of issue	January 28, 1988
Status	Product Specification
FAST Products	

FAST 74F732, 74F733 Multiplexers

74F732 Quad Data Multiplexer, Inverting (3-State)
74F733 Quad Data Multiplexer, Non-Inverting (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F732	6.0ns	65mA
74F733	6.0ns	75mA

FEATURES

- **Quad 2-to-1 Multiplexer (two busses to one bus)**
- **Data can flow in either direction between busses (A → B, A → C, B → C, B → A, C → A, C → B)**
- **A built-in "break-before-make" feature eliminates current glitches and simplifies PC board design**
- **Output Enable for each bus to allow flexible contention control**
- **3-State outputs sink 64mA**

DESCRIPTION

The 74F732/74F733 are Quad Data Multiplexers designed to provide a simple means to control the flow of bidirectional data between three data busses.

The 74F732/74F733 consist of four multiplexers. Each multiplexer has three I/O (A_n, B_n, C_n) pins and uses one Output Enable pin ($\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$). There are two Select (S_0, S_1) pins and a Direction (DIR) pin to control data flow paths for all four multiplexers.

ORDERING INFORMATION

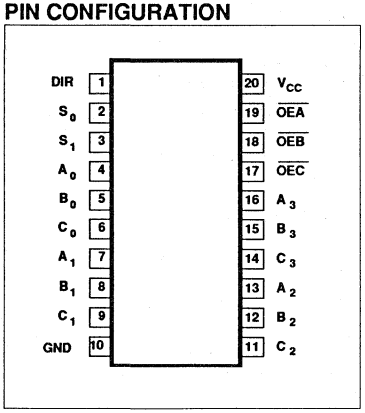
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F732N, N74F733N
20-Pin Plastic SOL	N74F732D, N74F733D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

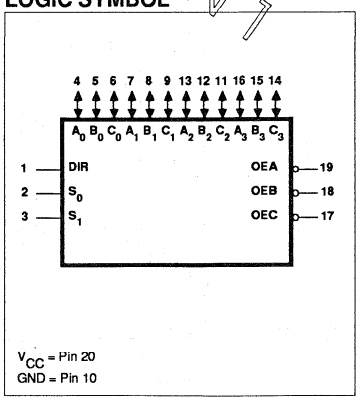
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Data inputs for Bus A	3.5/1.0	70μA/0.6mA
B_0 - B_3	Data inputs for Bus B	3.5/1.0	70μA/0.6mA
C_0 - C_3	Data inputs for Bus C	3.5/1.0	70μA/0.6mA
DIR	Direction control input	1.0/1.0	20μA/0.6mA
S_0 - S_1	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OEA}$, $\overline{OEB}$ $\overline{OEC}$	Output Enable inputs (Active Low)	1.0/1.0	20μA/0.6mA
A_0 - A_3	Data output for Bus A	750/106.7	15mA/64mA
B_0 - B_3	Data output for Bus B	750/106.7	15mA/64mA
C_0 - C_3	Data output for Bus C	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

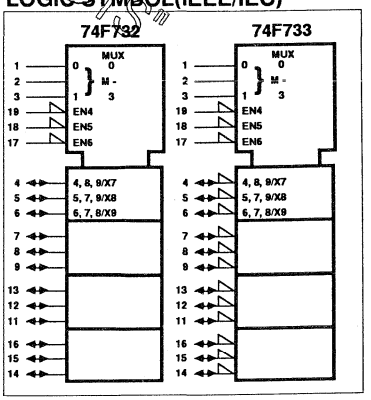
PIN CONFIGURATION



LOGIC SYMBOL

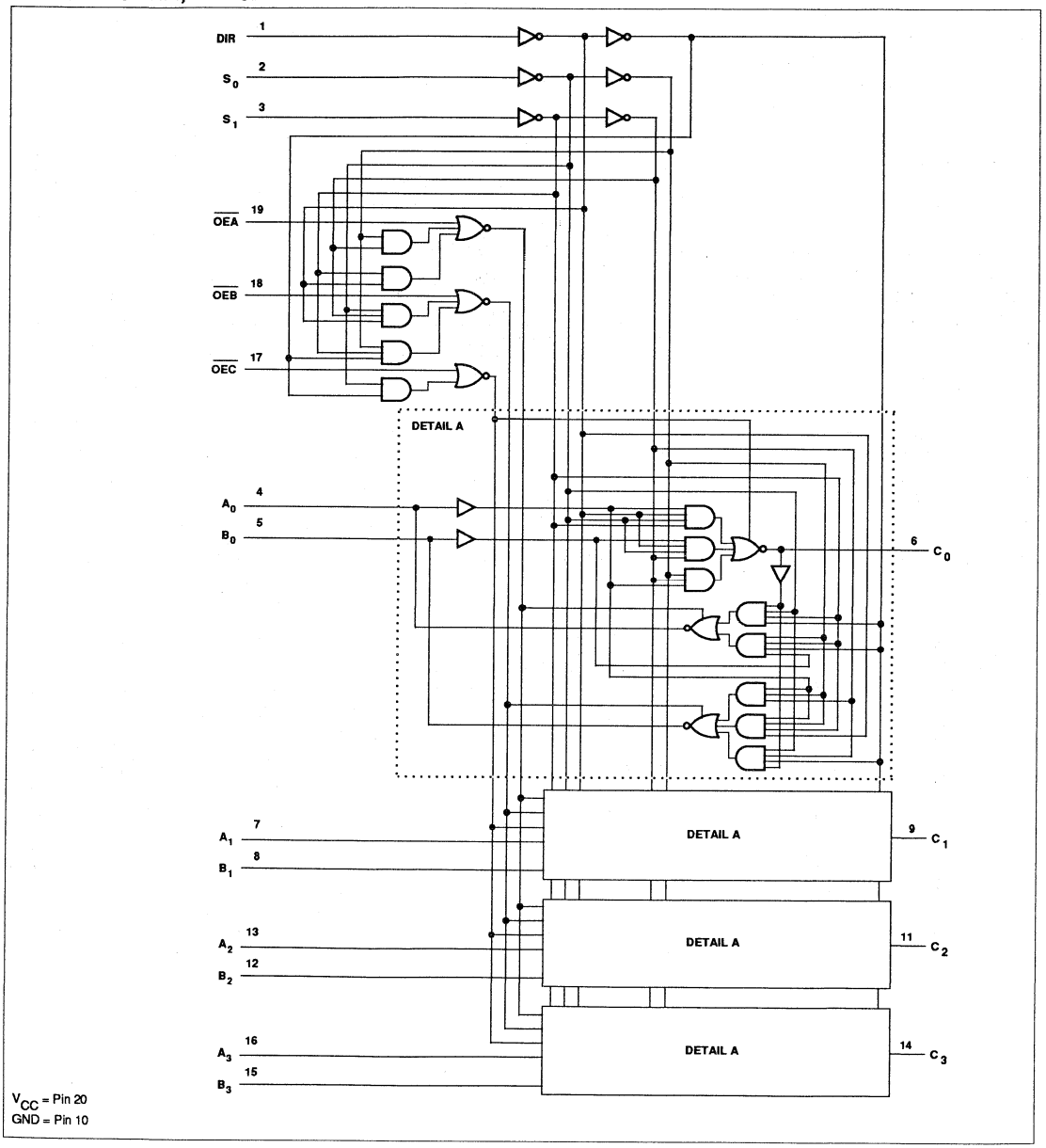


LOGIC SYMBOL(IEEE/IEC)

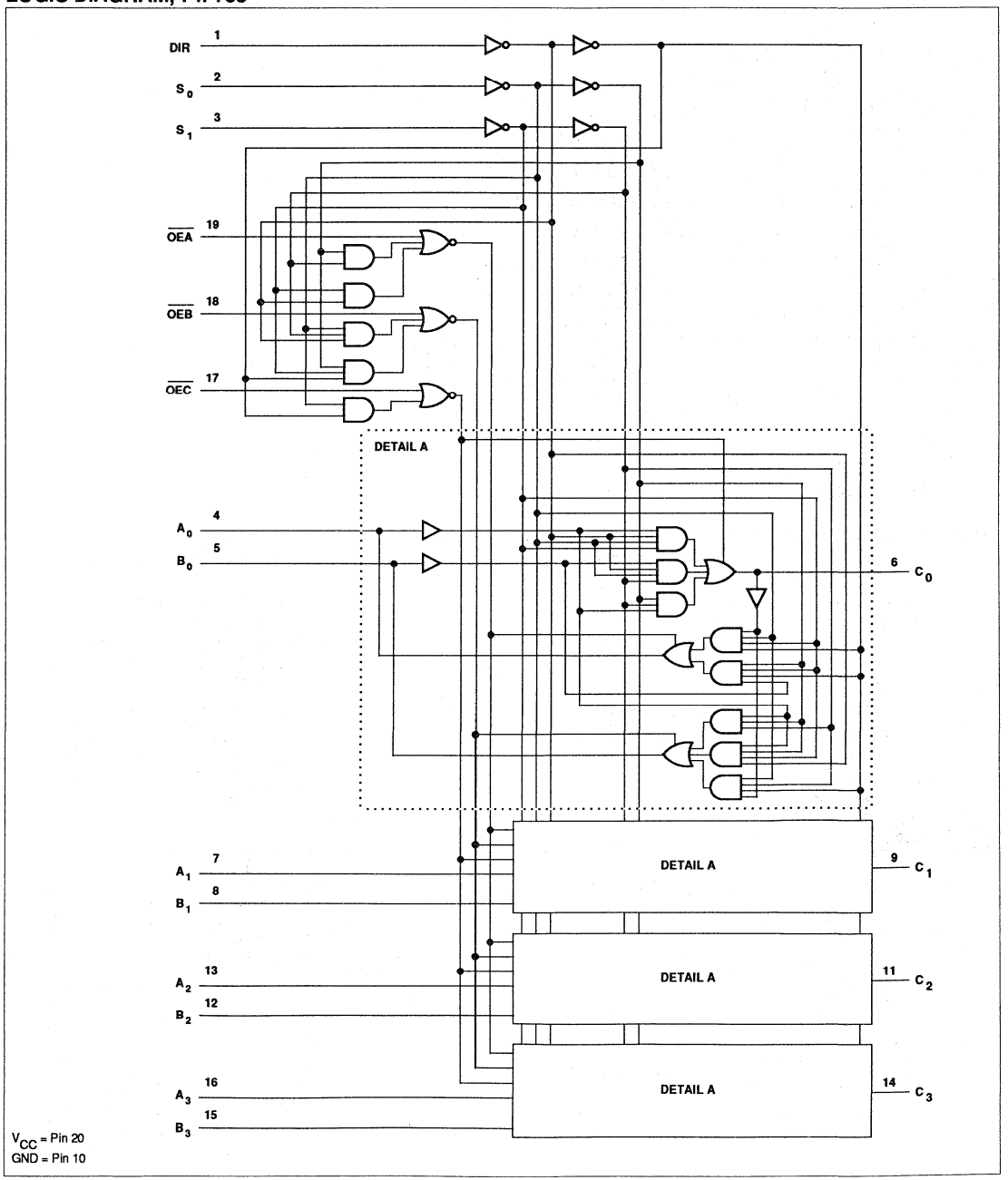


With the Select control, data can flow in the following directions between busses: A to B, A to C, B to A, B to C, C to B, A to B and C. A built-in "break-before-make" feature eliminates current glitches common to systems using 3-State transceivers to accomplish the same function.

LOGIC DIAGRAM, 74F732



LOGIC DIAGRAM, 74F733



FUNCTION TABLE

INPUTS						OPERATING MODE
DIR	S_0	S_1	$\overline{OEA}$	$\overline{OEB}$	$\overline{OEC}$	
X	X	X	H	X	X	Bus A disabled except for input
X	X	X	X	H	X	Bus B disabled except for input
X	X	X	X	X	H	Bus C disabled except for input
L	L	L	X	H*	L	Data flow from Bus A to Bus C
H	L	L	L	H*	X	Data flow from Bus C to Bus A
L	L	H	H*	X	L	Data flow from Bus B to Bus C
H	L	H	H*	L	X	Data flow from Bus C to Bus B
L	H	L	X	L	H*	Data flow from Bus A to Bus B
H	H	L	L	X	H*	Data flow from Bus B to Bus A
X	H	H	X	L	L	Data flow from Bus A to Bus B and Bus C
X	H	H	X	H	L	Data flow from Bus A to Bus C
X	H	H	X	L	H	Data flow from Bus A to Bus B

H = High voltage level
L = Low voltage level
X = Don't care
* = If this is not High then the corresponding outputs will be High (74F732) or Low (74F733)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.4		V
				I_{OH} = -15mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ DIR, S_0, S_1	V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	Low-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ DIR, S_0, S_1	V_{CC} = MAX, V_I = 0.5 V					-0.6	mA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_3 B_0 - B_3 C_0 - C_3	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_3 B_0 - B_3 C_0 - C_3	V_{CC} = MAX, V_O = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F732	I_{CCH}	V_{CC} = MAX			55	80	mA
			I_{CCL}				75	105	mA
			I_{CCZ}				65	100	mA
		74F733	I_{CCH}	V_{CC} = MAX			70	100	mA
			I_{CCL}				80	115	mA
			I_{CCZ}				80	110	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F732

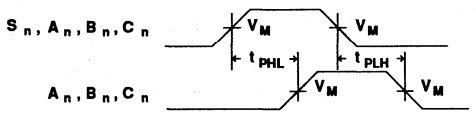
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n to A_n, B_n, C_n	Waveform 1, 2	2.0 1.0	4.5 3.0	8.0 6.0	2.0 1.0	8.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (NINV)	Waveform 1	4.5 4.5	7.0 7.0	10.0 10.0	4.0 4.0	11.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (INV)	Waveform 2	5.0 2.5	7.0 4.5	10.0 7.5	4.5 2.5	10.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 4.0	4.5 6.5	7.5 9.5	1.5 3.5	8.5 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	7.0 7.0	1.5 2.0	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	4.0 5.5	7.5 8.5	11.0 11.5	3.0 5.0	13.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	1.0 1.0	6.0 4.5	9.0 7.5	1.0 1.0	10.0 8.0	ns

AC ELECTRICAL CHARACTERISTICS for 74F733

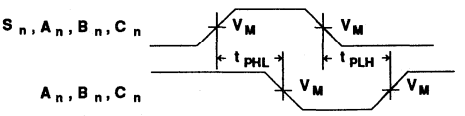
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n to A_n, B_n, C_n	Waveform 1, 2	1.5 1.5	4.0 4.0	7.0 7.0	1.0 1.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (NINV)	Waveform 1	3.0 4.0	5.0 6.0	7.5 9.0	2.5 3.5	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (INV)	Waveform 2	5.0 3.0	7.5 5.0	10.5 8.0	4.5 3.0	13.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.5 3.5	5.0 5.5	7.5 8.5	2.0 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 2.0	4.0 4.5	7.0 7.0	1.5 2.0	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	4.5 5.5	7.5 8.5	11.0 12.0	4.0 5.0	13.0 13.5	ns
t_{PHZ} t_{PLZ}*	Output Disable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	1.5 7.0	4.5 11.5	7.5 14.5	1.0 7.0	8.0 16.0	ns

* Because of the 3-state output characteristics, the pick-off point is V_{OL} +0.8V.

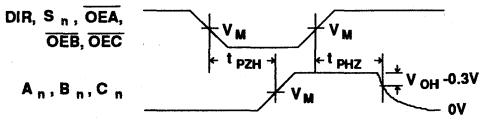
AC WAVEFORMS



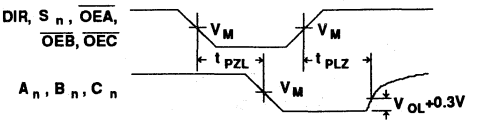
Waveform 1. Propagation Delay, Select And Data Busses



Waveform 2. Propagation Delay, Select And Data Busses



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

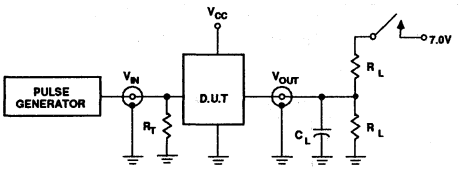


Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

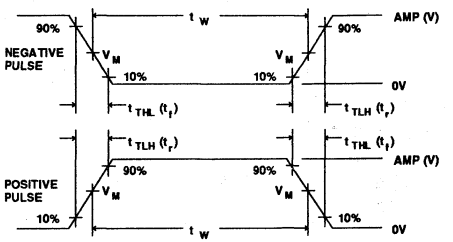
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0270
ECN No.	98220
Date of issue	November 27, 1989
Status	Product Specification
FAST Products	

FAST 74F756, 74F757, 74F760 Buffers

74F756 Octal Inverter Buffer (Open Collector)
74F757 Octal Buffer (Open Collector)
74F760 Octal Buffer (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F756	9.0ns	40mA
74F757	9.0ns	45mA
74F760	9.0ns	45mA

FEATURES

- **Octal bus interface**
- **Open collector versions of 74F240, 74F241 and 74F244**

DESCRIPTION

The 74F756, 74F757 and 74F760 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The 74F756 is the open collector version of 74F240, 74F757 is the open collector version of 74F241 and 74F760 is the open collector version of 74F244. These devices feature two Output Enables, $\overline{OE}_a$ and $\overline{OE}_b$ (or OE_b for the 'F757), each controlling four of the outputs.

ORDERING INFORMATION

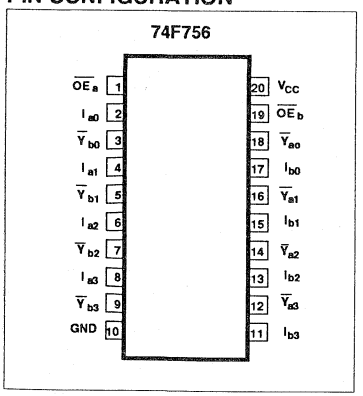
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F756N, N74F757N, N74F760N
20-Pin Plastic SOL	N74F756D, N74F757D, N74F760D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

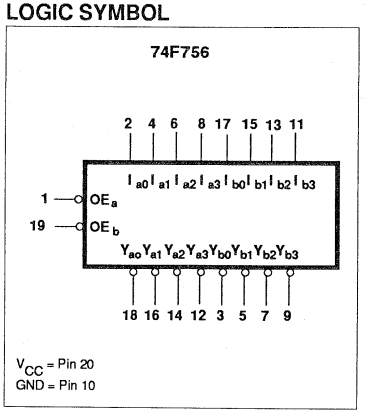
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/1.67	20µA/1.0mA
$\overline{OE}_a$, $\overline{OE}_b$	Output enable input (active Low)	1.0/1.67	20µA/1.0mA
OE_b	Output enable input (active High 'F757)	1.0/1.67	20µA/1.0mA
Y_{an}, Y_{bn}	Data outputs ('F757, 'F760)	OC/106.7	OC/64mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs ('F756)	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC= Open Collector

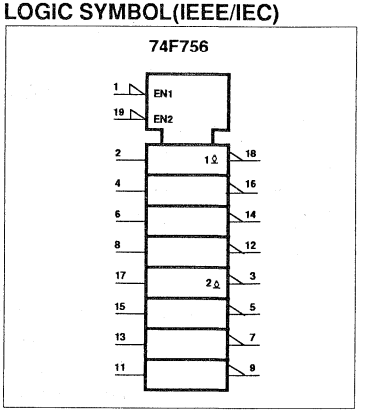
PIN CONFIGURATION



LOGIC SYMBOL

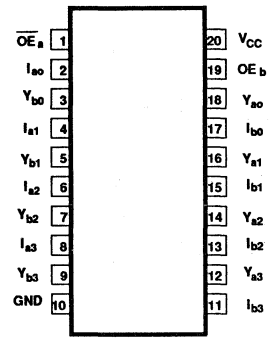


LOGIC SYMBOL(IEEE/IEC)



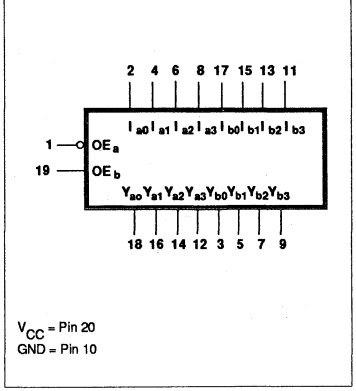
PIN CONFIGURATION

74F757



LOGIC SYMBOL

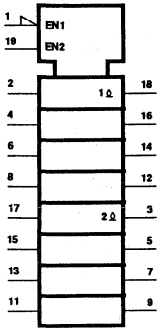
74F757



V_{CC} = Pin 20
GND = Pin 10

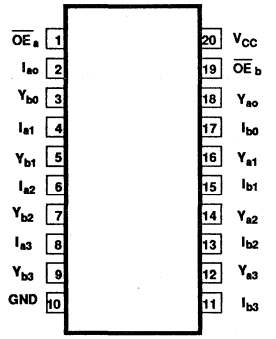
LOGIC SYMBOL(IEEE/IEC)

74F757



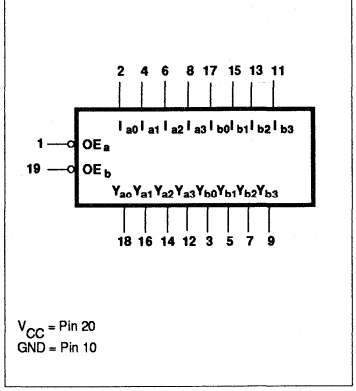
PIN CONFIGURATION

74F760



LOGIC SYMBOL

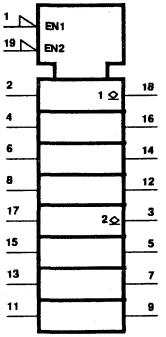
74F760



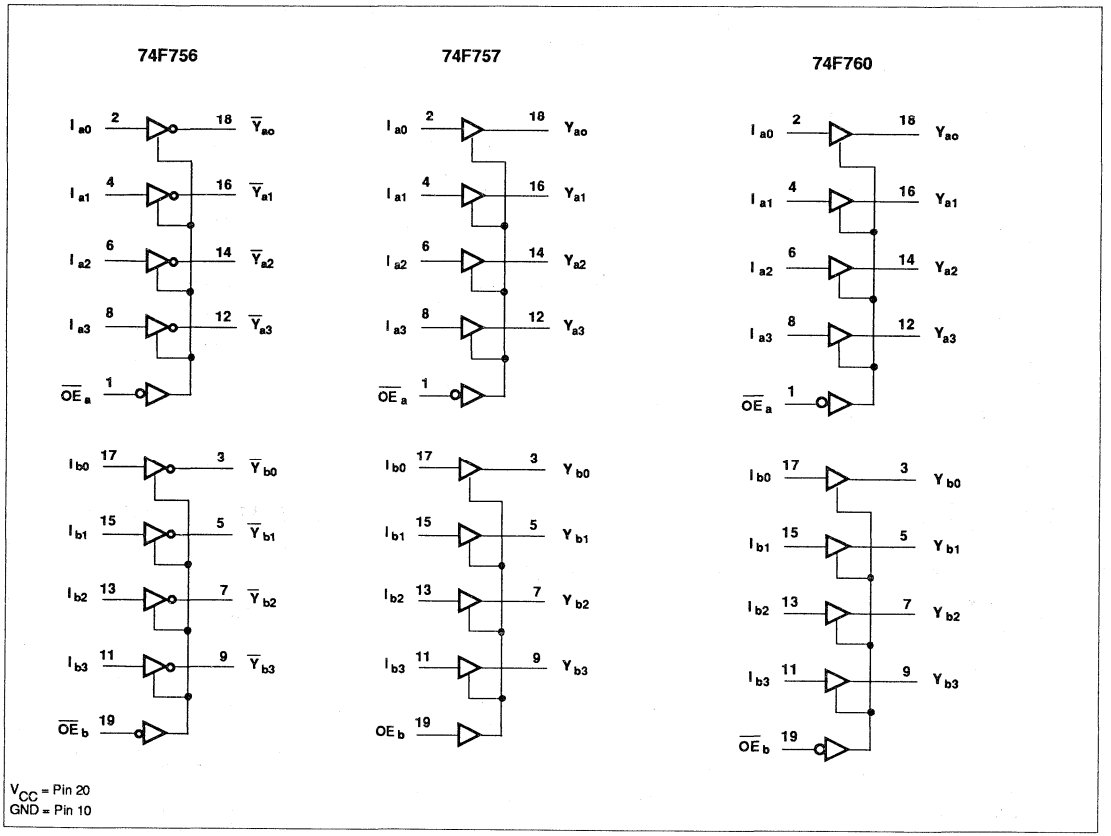
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

74F760



LOGIC DIAGRAM



FUNCTION TABLE, 74F756

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	H(off)	H(off)

FUNCTION TABLE, 74F760

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	H(off)	H(off)

FUNCTION TABLE, 74F757

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	H(off)	H(off)

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER				UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_K	Input clamp current			-18	mA
V_{OH}	High level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-1.0	mA
I_{CC}	Supply current (total)	74F756	I_{CCH}	V_{CC} = MAX				20	30	mA
			I_{CCL}					50	70	mA
		74F757	I_{CCH}					30	40	mA
			I_{CCL}					55	80	mA
		74F760	I_{CCH}					25	37	mA
			I_{CCL}					55	80	mA

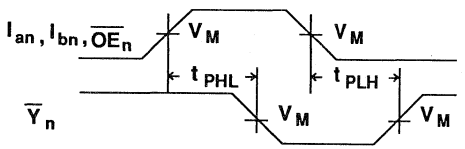
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

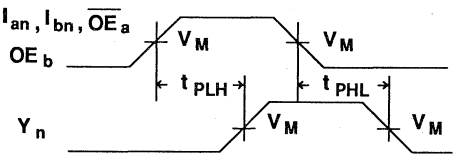
AC ELECTRICAL CHARACTERISITICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to $\overline{Y}_n$	74F756	Waveform 1, 2	8.5 1.0	11.0 3.0	14.0 6.0	8.5 1.0	15.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{Y}_n$		Waveform 1, 2	9.0 5.0	11.5 7.0	14.5 10.0	9.0 4.5	15.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F757	Waveform 1, 2	7.5 3.0	10.5 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_a$ or OE_b to Y_n		Waveform 1, 2	9.0 4.5	10.5 7.0	15.0 10.0	8.5 4.0	16.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F760	Waveform 1, 2	7.5 3.5	10.0 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to Y_n		Waveform 1, 2	9.5 5.0	11.5 7.0	14.5 10.0	9.0 4.5	15.0 10.5	ns

AC WAVEFORMS



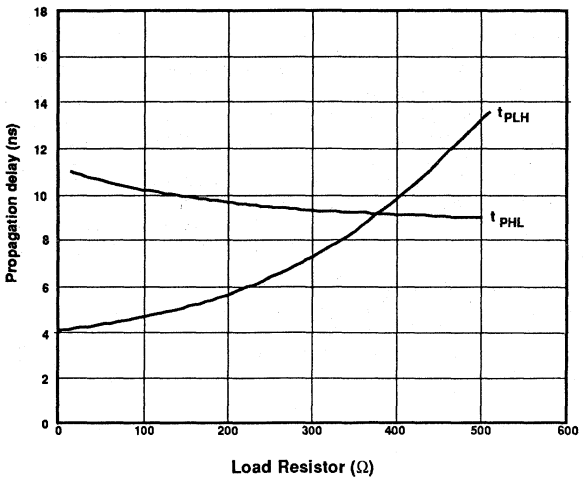
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs

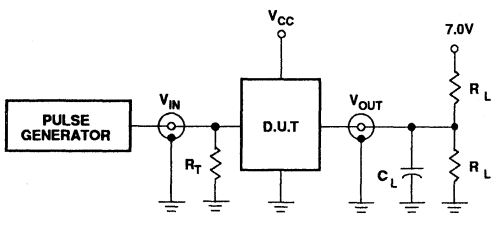
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

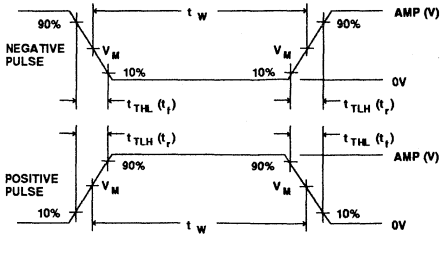


NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500 Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DRAM dual-ported controllers

74F764-1/74F765-1

FEATURES

- Allows two microprocessors to access the same bank of dynamic RAM
- Performs arbitration, signal timing, address multiplexing and refresh
- 9 Address output pins allow direct control of up to 256K dynamic RAMs
- External address multiplexing enables control of 1Mbit (or greater) dynamic RAMs
- Separate refresh clock allows adjustable refresh timing
- 74F764-1 has an on-chip 18-bit address input latch
- 74F764-1/765-1 allow control of dynamic RAMs with row access times down to 40ns
- 74F764-1/765-1 output drivers designed for first reflected wave switching

DESCRIPTION

The 74F764-1/765-1 DRAM Dual-ported Controller is a high-speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F764-1 vs. 74F765-1

The 74F764-1, though functionally and pin-to-pin compatible with the 74F765-1, differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

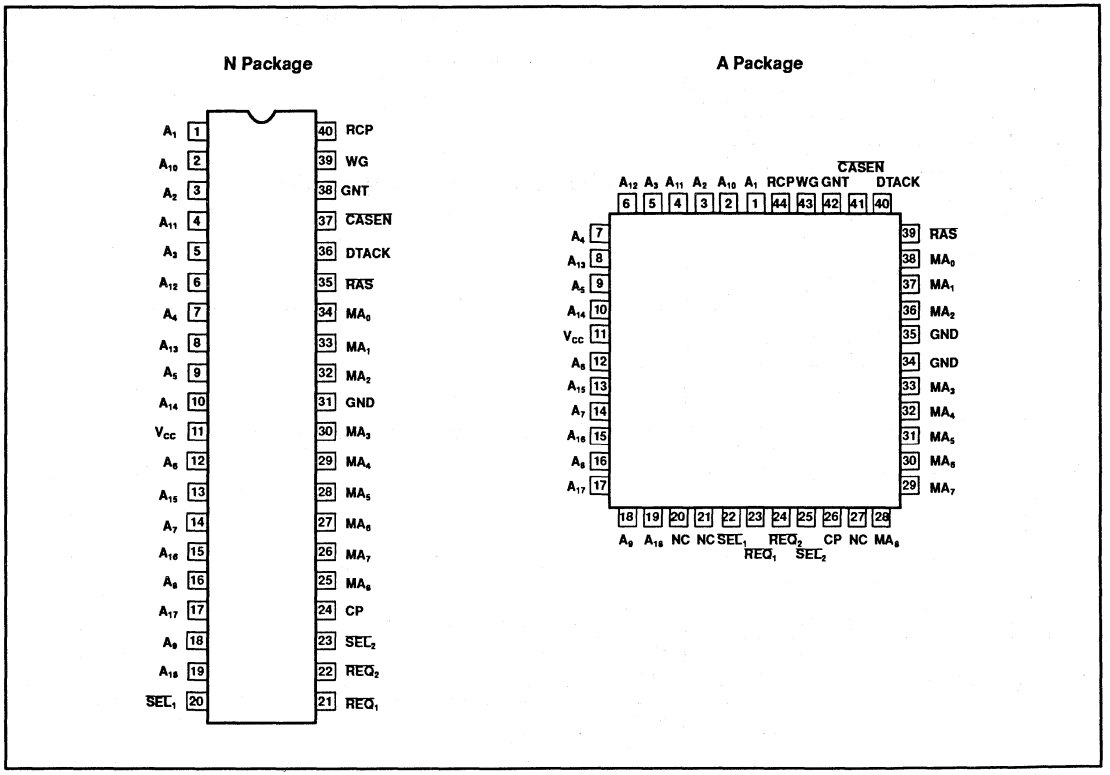
The specialized outputs eliminate the need for signal terminations in essentially all applications.

Both devices are available in 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

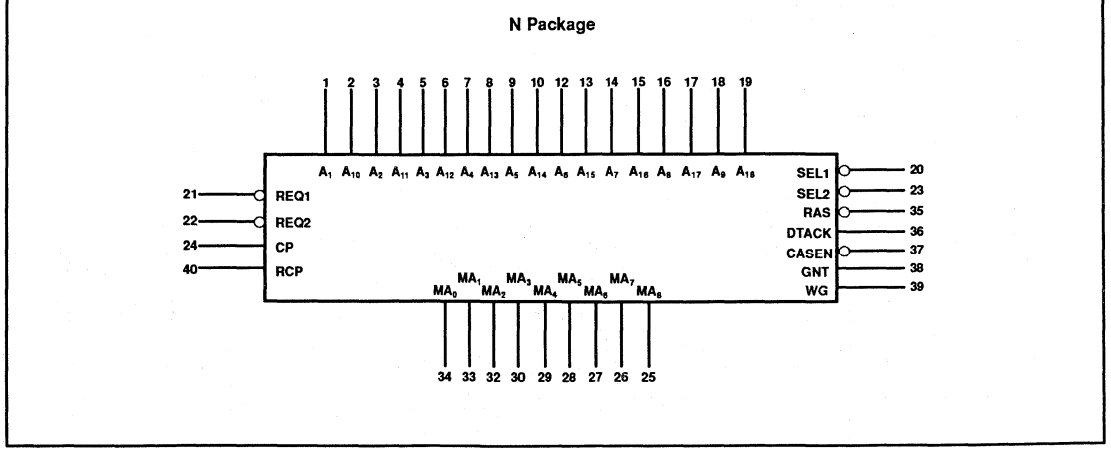
ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%, T_A = 0°C to 70°C
Plastic Dip	74F764-1N, 74F765-1N
PLCC–44	74F764-1A, 74F765-1A

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A_1	1	1	I	Address inputs used to generate memory row address
A_2	3	3	I	
A_3	5	5	I	
A_4	7	7	I	
A_5	9	9	I	
A_6	12	12	I	
A_7	14	14	I	
A_8	16	16	I	
A_9	18	18	I	
A_{10}	2	2	I	Address inputs used to generate memory column address
A_{11}	4	4	I	
A_{12}	6	6	I	
A_{13}	8	8	I	
A_{14}	10	10	I	
A_{15}	13	13	I	
A_{16}	15	15	I	
A_{17}	17	17	I	
A_{18}	19	19	I	
$\overline{REQ}_1$	21	23	I	Memory access request from Microprocessor 1
$\overline{REQ}_2$	22	24	I	Memory access request from Microprocessor 2
CP	24	26	I	Clock input which determines the master timing
RCP	40	44	I	Refresh clock determines the period of refresh for each row after it is internally divided by 64
$\overline{SEL}_1$	20	22	O	Select signal is activated in response to active $\overline{REQ}_1$ input, indicating selection of Microprocessor 1
V_{CC}	11	11		Power supply +5V ±10%
GND	31	34 35		Ground
$\overline{SEL}_2$	23	25	O	Select signal is activated in response to active $\overline{REQ}_2$ input, indicating selection of Microprocessor 2
MA_0	34	38	O	Memory address output pins, designed to drive address lines of the DRAM
MA_1	33	37	O	
MA_2	32	36	O	
MA_3	30	33	O	
MA_4	29	32	O	
MA_5	28	31	O	
MA_6	27	30	O	
MA_7	26	29	O	
MA_8	25	28	O	
GNT	38	42	O	Grant output, activated upon start of a memory access cycle
$\overline{RAS}$	35	39	O	Row Address Strobe, used to latch the row address into the bank of DRAM (to be connected directly to the $\overline{RAS}$ inputs of the DRAMs)
WG	39	43	O	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
$\overline{CASEN}$	37	41	O	Column Address Strobe Enable is used to latch the column address into the bank of DRAMs
DTACK	36	40	O	Data Transfer Acknowledge indicates that data on the DRAM output lines is valid or the proper access time has been met

ARCHITECTURE

The 74F764-1/765-1 DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 74F764-1/765-1 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{REQ}$ inputs will be serviced by activating the corresponding $\overline{SEL}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress. The arbitration is accomplished by sampling the $\overline{REQ}_1$ and $\overline{REQ}_2$ inputs on different edges of the CP clock. $\overline{REQ}_1$ is sampled on the rising edge and $\overline{REQ}_2$ on the falling edge (refer to Figures 1 and 2).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated every 64 RCP cycles. The refresh counter is incremented at the end of every refresh cycle, and provides the refresh address.

Since $\overline{SEL}$ outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the $\overline{SEL}$ outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock for the 74F764-1/765-1 should be equal to:

(Tras(of the DRAM) + 22 – 10)/4ns plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate $\overline{REQ}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If however, a refresh cycle is in process, and there is only one active $\overline{REQ}$ input, the $\overline{SEL}$ output corresponding to the active input $\overline{REQ}$ will be asserted but the GNT output will not go High until after the completion of the refresh cycle (see Figures 8 and 9).

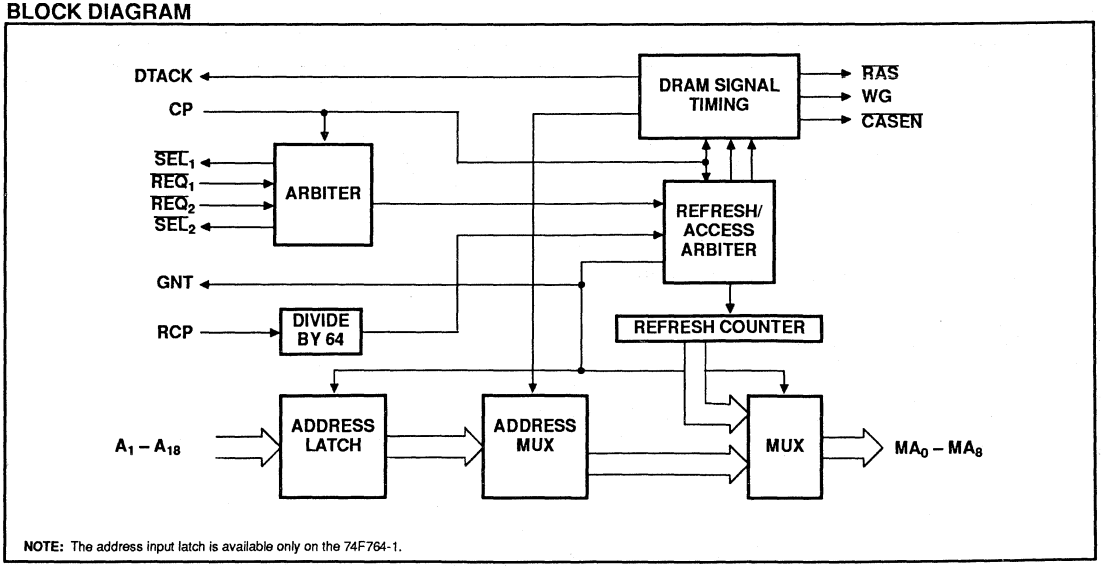
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the $\overline{SEL}$ output for the other processor will not be issued, though GNT is asserted at that time, because the toher processor is performing an access cycle. This will ensure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the $\overline{SEL}$ output corresponding to the awaiting $\overline{REQ}$ input will be asserted, followed by the GNT output. If however, there were any pending refresh requests, assertion of the GNT output will be held OFF until the refresh request has been serviced.

When GNT goes High, the A_1–A_{18} address inputs to the 74F764-1/765-1 are latched internally and the A_1–A_9 signals are propagated to the MA0–MA8 outputs. The address inputs are not latched by the 74F765-1 and therefore, A_1–A_9 inputs propagate directly to the MA_0–MA_8 outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{RAS}$ output is asserted.

BLOCK DIAGRAM



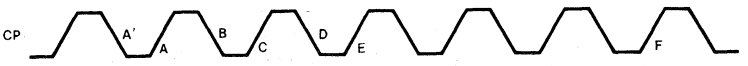
NOTE: The address input latch is available only on the 74F764-1.

One half-clock cycle later, the A10–A18 latch outputs on the 74F764/764A or A10–A18 inputs to the 74F765/765A are selected and propagated to the MA0–MA8 outputs (refer to Figures 1 and 2). The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

A half-clock cycle is again allowed for the A_{10}–A_{18} signals to propagate and stablize. $\overline{CASEN}$ then becomes valid. $\overline{CASEN}$ can be used as $\overline{CAS}$ output or decoded with Higher-order address signals to produce multiple $\overline{CAS}$ signals. After $\overline{CASEN}$ is valid, the controller will wait for 2 $^1/_2$ clock cycles before negating $\overline{RAS}$, making a total $\overline{RAS}$ pulse width of approximately 4 clock cycels. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

All controller output signals are held in this final state until the selected processor withdraws its request by driving its $\overline{REQ}$ input High. When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

A refresh cycle is serviced by propagating the 9 refresh counter address signals to the MA0–MA8 outputs. After a half-clock cycle the RAS output is asserted for four cycles and then negated for three clock cycles to meet the RAS precharge requirements of the DRAMS (see Figures 4 and 5).



A' $\overline{REQ_2}$ sampled

A $\overline{REQ_1}$ sampled ($\overline{REQ_2}$ disabled by $\overline{SEL_1}$ circuitry)
$\overline{SEL_1}$ triggered ($\overline{SEL_1}$ triggered by $\overline{REQ_1}$ sample circuitry)

B GNT triggered
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
$A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs

C $\overline{RAS}$ triggered

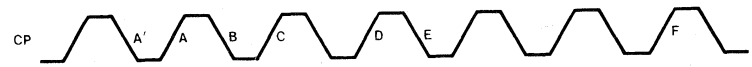
D WG triggered
$A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

* Only on the F764-1.

Figure 1. Sequence of Events for $\overline{REQ_1}$ Memory Access Cycle for 74F764-1/765-1



A' $\overline{REQ_2}$ sampled
$\overline{SEL_2}$ triggered ($\overline{SEL_2}$ triggered by $\overline{REQ_2}$ sampling circuitry)

A $\overline{REQ_1}$ is not sampled (disabled by $\overline{SEL_2}$ circuitry)

B GNT triggered
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
$A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs

C $\overline{RAS}$ triggered

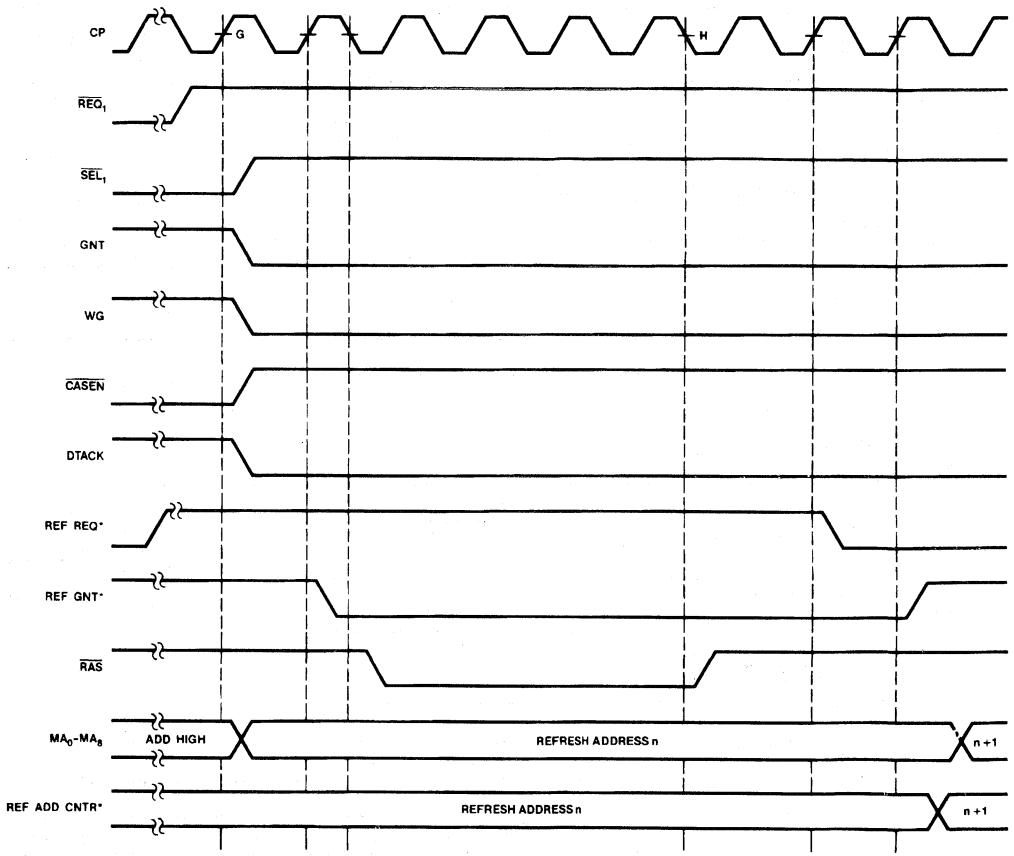
D WG triggered
$A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

* Only on the F764-1.

Figure 2. Sequence of Events for $\overline{REQ_2}$ Memory Access Cycle for 74F764-1/765-1



NOTE:
* These are internal signals only.

Figure 3. Refresh Cycle Timing following a $\overline{REQ_1}$ Memory Access Cycle for All Devices

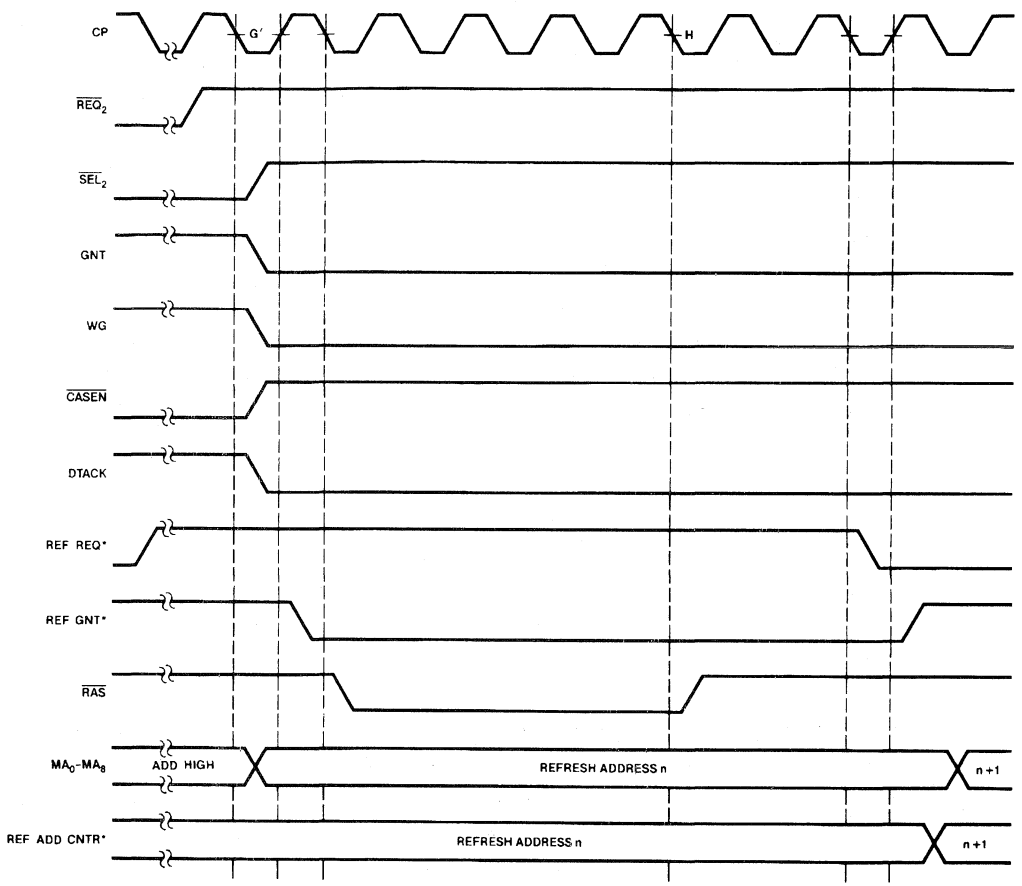


Figure 4. Refresh Cycle Timing following a $\overline{REQ}_2$ Memory Access Cycle for All Devices

USING THE 74F764-1/765-1 TO ADDRESS 1MBIT DRAMs

The addressing capabilites of the DRAM dual-ported controllers can be extedned to address 1Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 5 shows an application, using an external 2-to-1 multiplexer to address 1Mbit dynamic RAMs. The 9-bit internal refresh counter of the controller provides 512 row addresses which more than meet the refreshing needs for most industry standard 1Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 512 rows.

Additional address bits (for larger DRAMs) may also be multiplexed externally as long as the DRAM refreshing requirements do not exceed 512 row addresses.

The WG output of the controller should be used to multiplex between the external row and column address bits. However, it is important that the propagation delay through the external mulitplexer does not cause column address setup violations on the dynamic RAM.

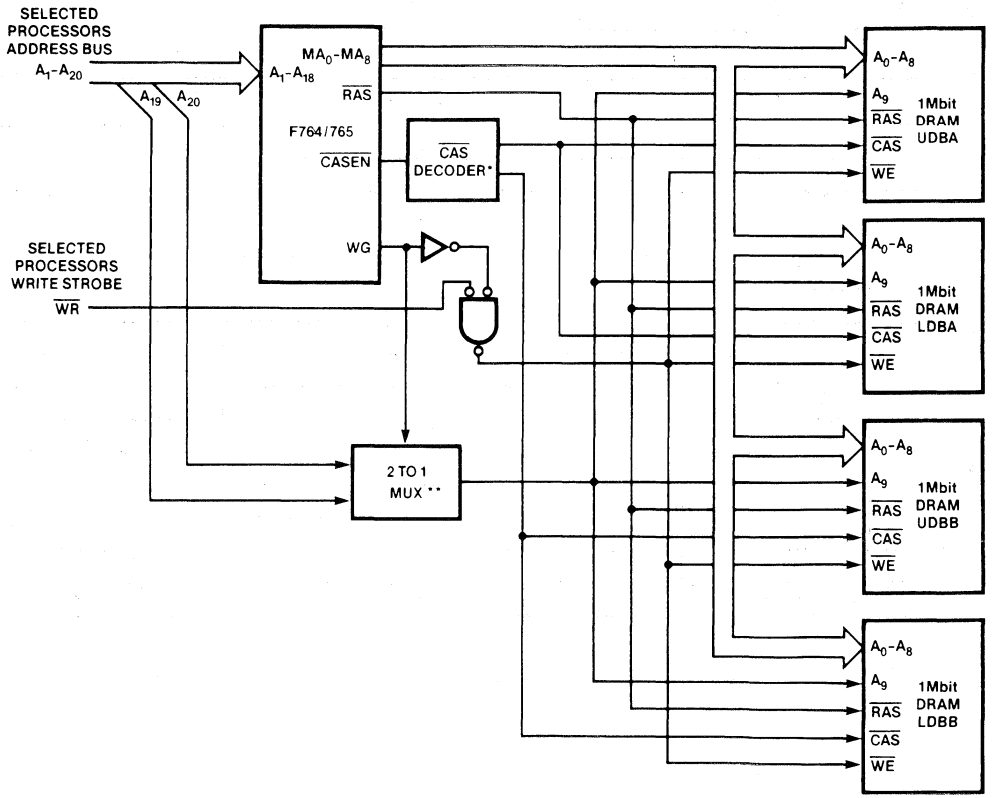


Figure 5. Using the Controller to Address 1Mbit DRAMs

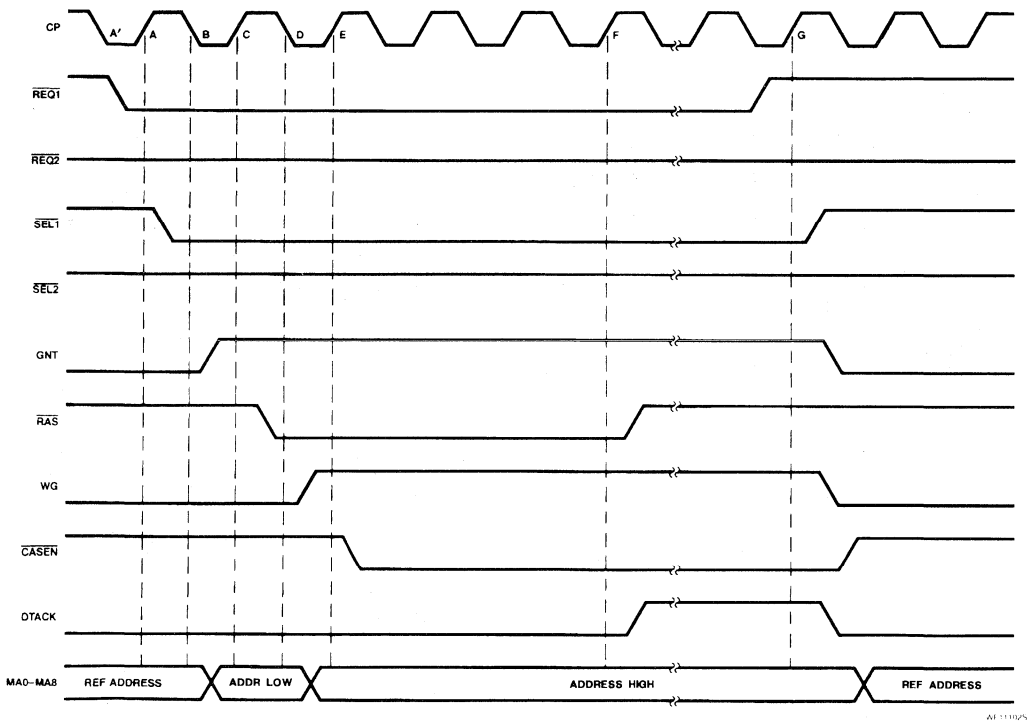


Figure 6. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing for 74F764-1/765-1

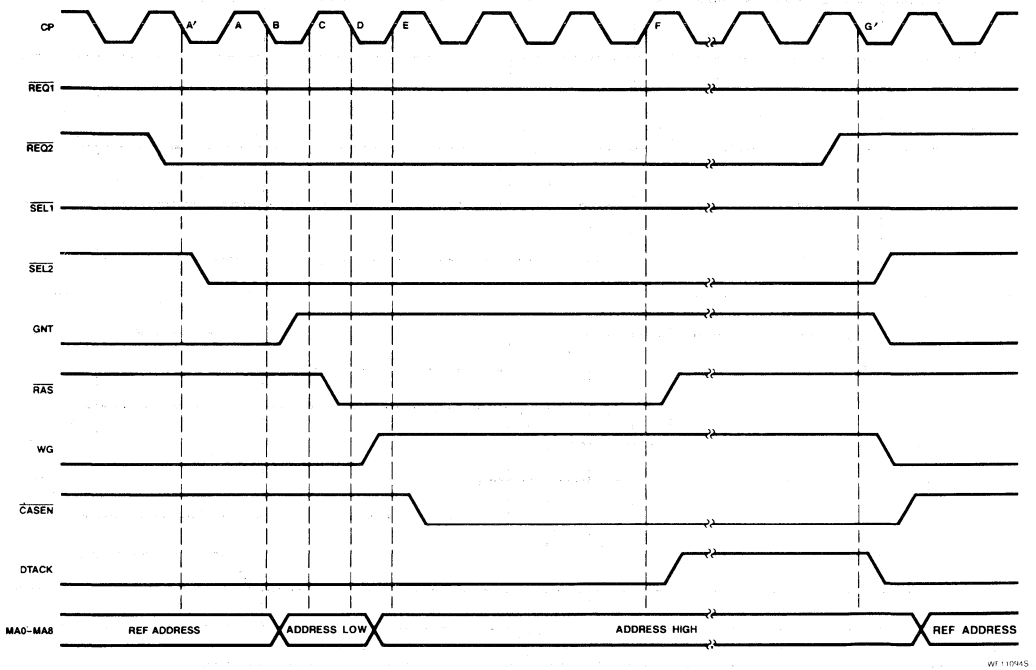


Figure 7. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing for 74F764-1/765-1

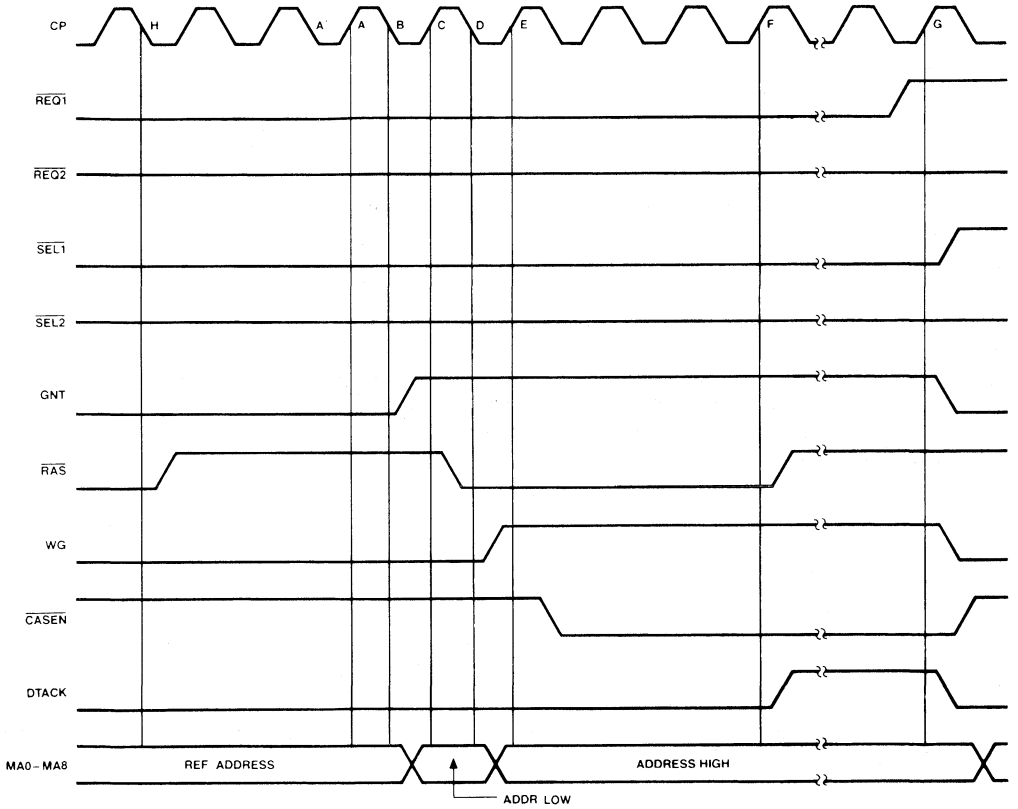


Figure 8. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing following a Refresh Cycle for 74F764-1/765-1

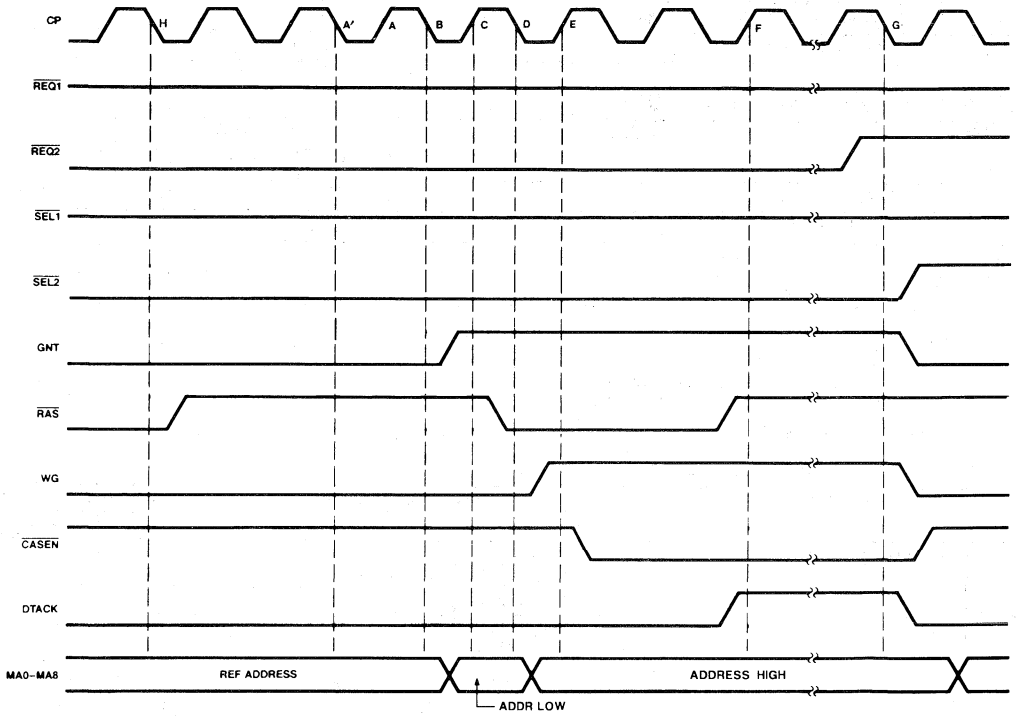


Figure 9. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing following a Refresh Cycle for 74F764-1/765-1

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the oprating free-air temperature range.)

SYMBOL	PARAMETER	74F764-1/765-1	UNIT
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_{IN}	Input Voltage	-0.5 to +7.0	V
I_{IN}	Input Current	-30 to +5	mA
V_{OUT}	Voltage applied to Output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to Output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F764-1/765-1			UNIT
		MIN	NORM	MAX	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	High-level Input Voltage	2.0			V
V_{IL}	Low-level Input Voltage			0.8	V
I_{IK}	Input Clamp Current			-18	mA
I_{OH}	High-level Output Current[3]			-20	mA
I_{OL}	Low-level Output Current[3]			8	mA
T_A	Operating free-air temperature range				°C

NOTE:

3. Transient currents will exceed these values in actual operation.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F764-1/765-1			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = -20mA	±10% V_{CC}	2.4	2.70		V
			V_{IH} = MIN		±5% V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = 8mA	±10% V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5% V_{CC}		0.30	0.50	V
V_{OL2}[3]	Low-level output voltage			I_{OL2}[3] =75mA	±5% V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.7	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.2	-0.6	mA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX			-80	-150	-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				120	165	mA
		I_{CCL}					125	170	mA

NOTES:

1. For the conditions shown as MIN or MAX, use the appropriate value under the recommended oprating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of hihg-speed test appartus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over the normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	74F764-1/765-1					UNIT
		T_A = +25°C, V_{CC} = +5.0V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 300pF, R_L = 70Ω		
		MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	100	150		100		MHz
t_{PLH}	Propagation delay CP(G) to $\overline{SEL}_1$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A) to $\overline{SEL}_1$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(G') to $\overline{SEL}_2$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A') to $\overline{SEL}_2$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(B) to GNT	9	12	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G') to GNT	20	23	26	17	28	ns
t_{PLH}	Propagation delay CP(B) to MA(row address)	11	14	17	10	19	ns
t_{PHL}		14	18	22	13	24	
t_{PLH}	Propagation delay CP(F or H) to $\overline{RAS}$	11	14	16	10	18	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$	13	17	20	12	22	ns
t_{PLH}	Propagation delay CP(D) to WG	9	11	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G') to WG	20	23	26	19	26	ns
t_{PLH}	Propagation delay CP(D) to MA(column address)	12	14	17	11	19	ns
t_{PHL}		14	18	21	13	23	
t_{PLH}	Propagation delay CP(G or G') to $\overline{CASEN}$	14	17	20	12	22	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$	14	16	19	13	21	ns
t_{PLH}	Propagation delay CP(F) to DTACK	10	12	15	9	17	ns
t_{PHL}	Propagation delay CP(G or G') to DTACK	20	23	26	19	28	ns
	74F765-1 Only						
t_{PLH}	Propagation delay $A_1 - A_{18}$ to $MA_0 - MA_8$	9	11	14	8	16	ns
t_{PHL}		9	12	15	8	17	

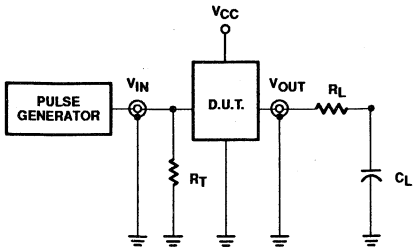
AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER	74F764-1/765-1					UNIT
		T_A = +25°C, V_{CC} = +5.0V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 300pF, R_L = 70Ω		
		MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP	3	1		4		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP to $\overline{REQ}_1$, $\overline{REQ}_2$	2	0		3		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	5	3		5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width High or Low	5			5		ns
	74F764-1 Only						
$t_s(H)$ $t_s(L)$	Setup time, High or Low $A_1 - A_{18}$ to CP (↓)	0	-1[1]		1		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP (↓) to $A_1 - A_{18}$	5	3		6		ns

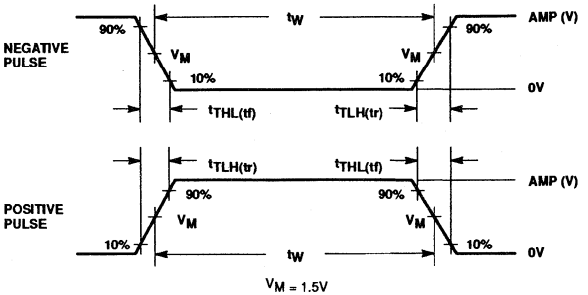
NOTE:

1. These numbers indicate that the address inputs have a negative setup time and could be valid 1ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will ensure that setup time for Address Bus 1 is not violated.

TEST CIRCUIT AND WAVEFORMS FOR ALL DEVICES



Test Circuit for Simulating RAM Boards



Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	T_W	T_{TLH}	T_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:
R_L = Load resistor to GND, see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

APPLICATIONS

The DRAM dual-ported controller can be designed into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (microcontrollers) and the data bus may differ in size.

Figure 10 shows a 68000 processor sharing a 64K × 8 (two banks each consisting of sixteen 16K × 1 devices) memory with a Z-80 processor. Since neither Z-80 nor 68000 have multiplexed address and data bus, the 74F765-1 is appropriate.

Since the Z-80 has an 8-bit wide data bus, data buffers are used to convert the 16-bit memory data bus to an 8-bit wide processor bus. Address bit (A_0) from the Z-80 serves as an enable to one of the two data buffers at a given time. Address bit (A15) from either the Z-80 or the 68000 distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

When the Z-80 is selected and A_{15} is a zero, all even bytes will be accessed from UDBA and all odd bytes from LDBA. Similarly, when A_{15} is a one, UDBB will contain all even bytes and LDBB all odd bytes.

For 68000, Upper and Lower Data Strobes ($\overline{UDS}$ and $\overline{LDS}$) determine whether a byte or word transfer will take place. The $\overline{WAIT}$ input on the Z-80 is asserted when $\overline{REQ_1}$ is generated, and is negated when the GNT output is asserted by the controller. The additional gating circuitry is to ensure that $\overline{DTACK}$ to the 68000 is asserted only when it is selected.

Figure 11 shows two 8086 processors sharing 1MByte (two banks each consisting of sixteen 256K × 1 devices) of dynamic RAM. Using 74F764 in this application may eliminate the need for an external address latch.

Similarly, Figure 12 shows two 68020 processors sharing the same amount of memory.

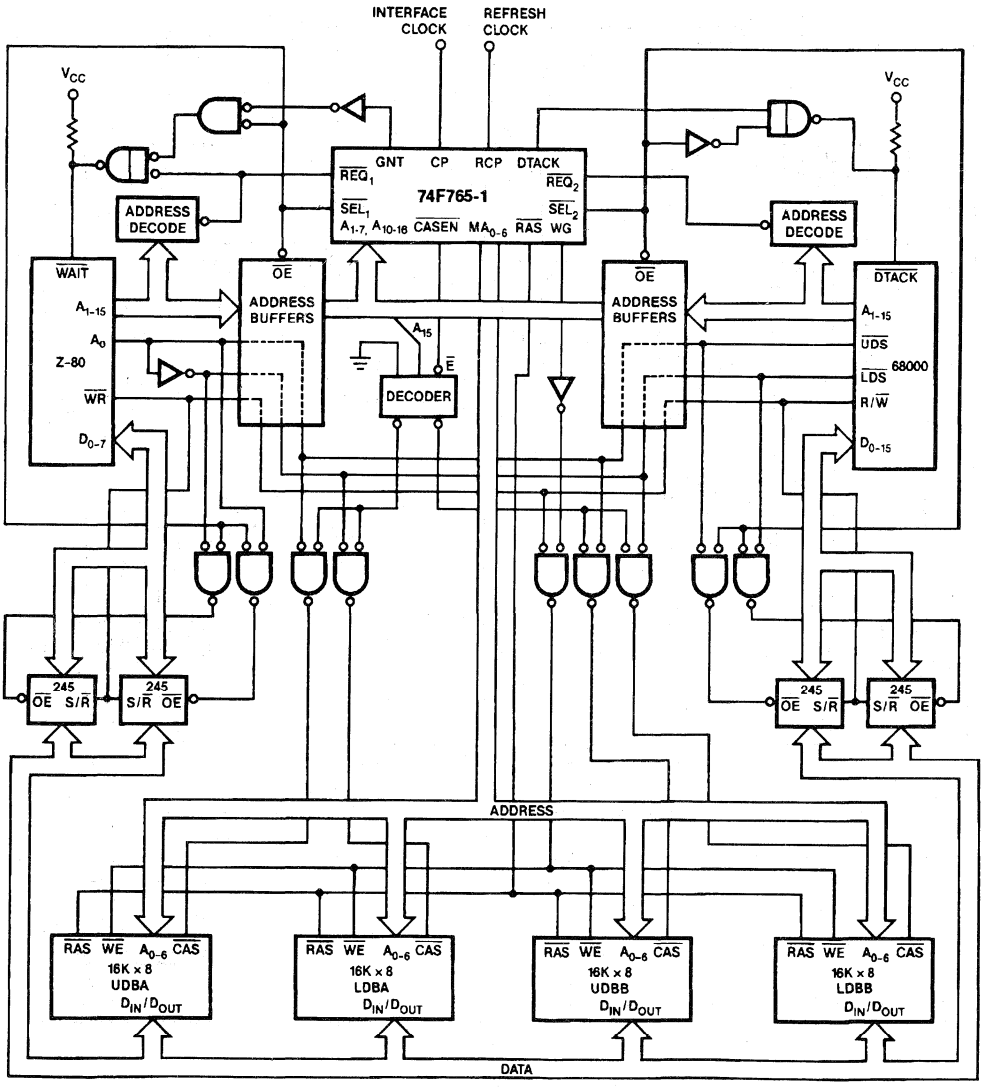
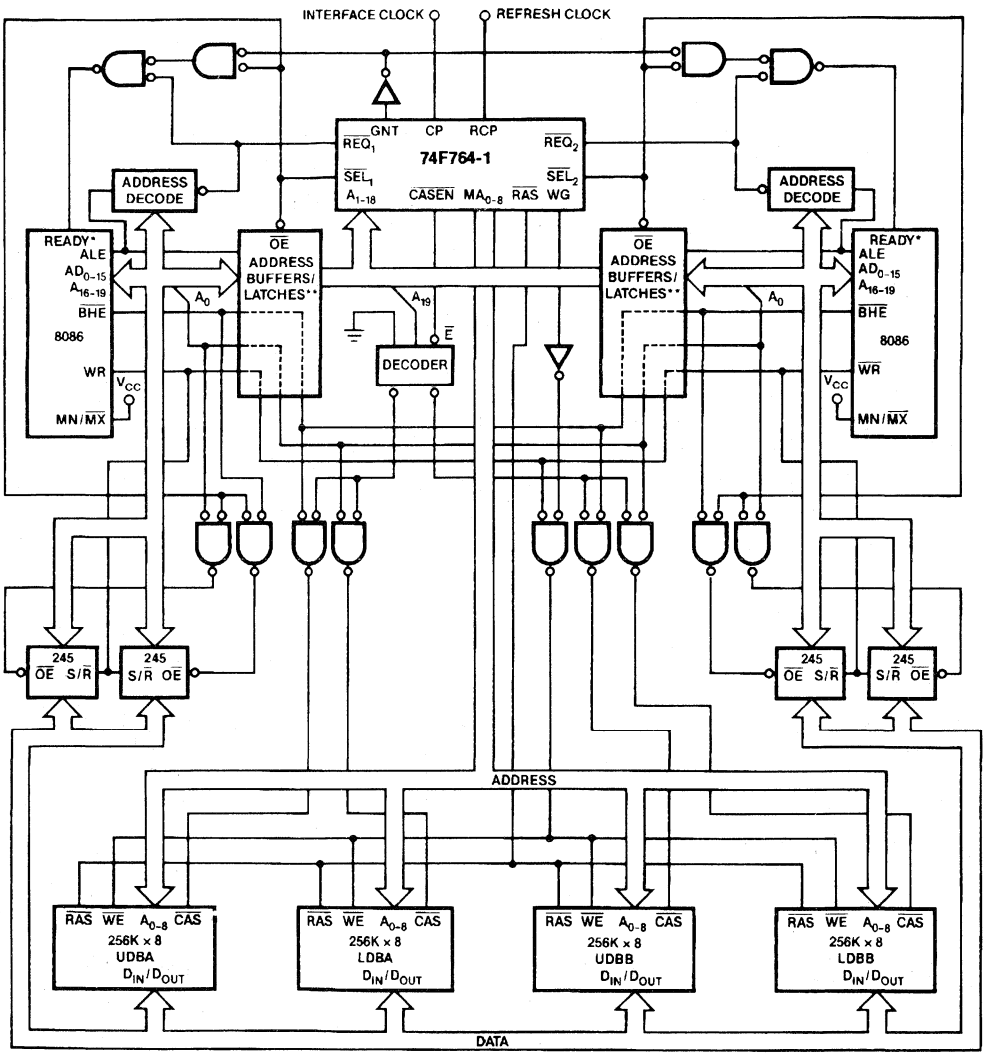


Figure 10. A 68000 Processor sharing 64K × 8 DRAM with a Z-80



* It might be necessary to synchronize READY by the 8284A. Please refer to the 8086 data sheet.
** Whether or not the 8086 address bus needs to be latched externally, should be determined by the relative speeds of the 8086 and the controller.

Figure 11. Two 8086 Processors sharing 1MByte of DRAM

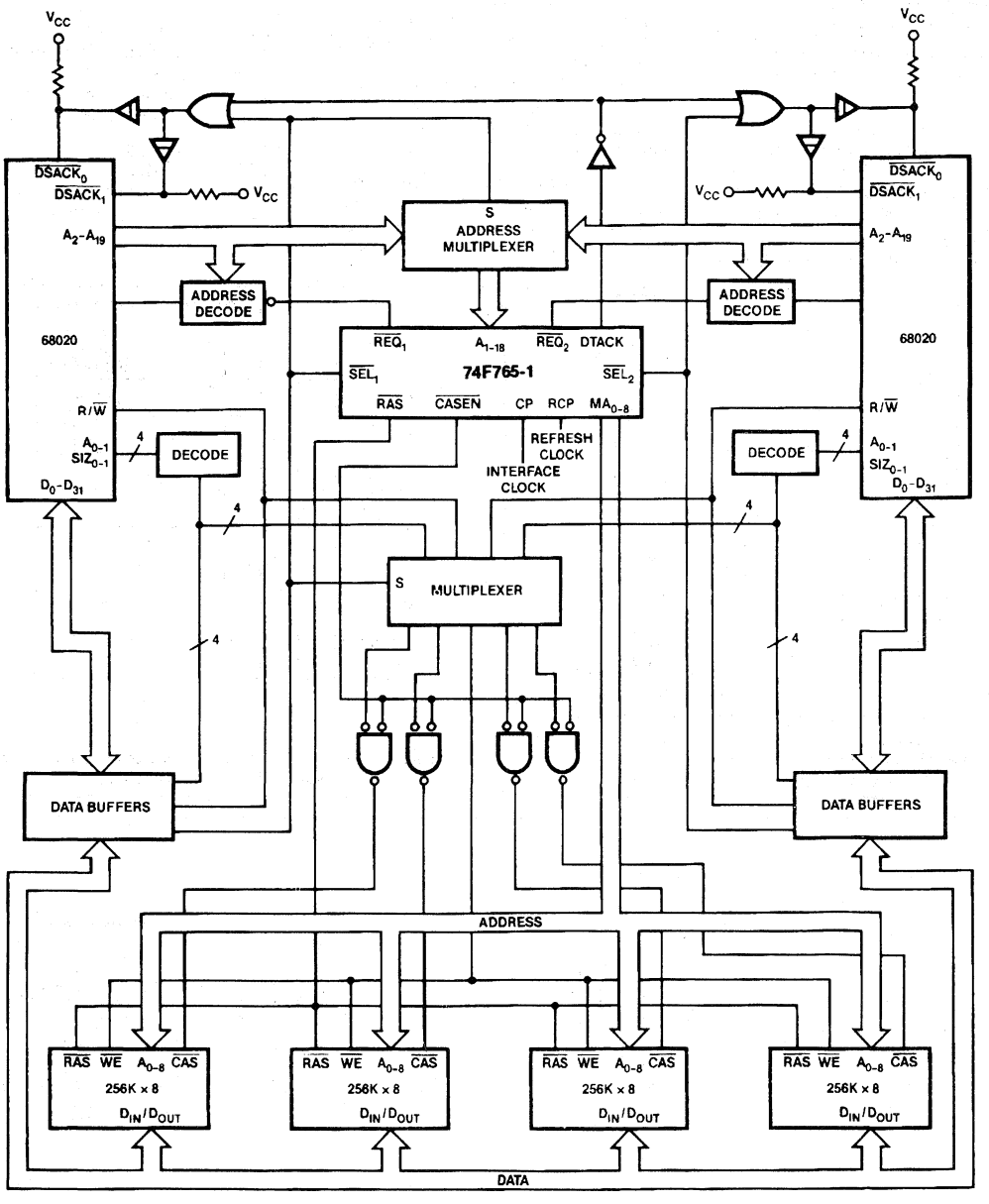


Figure 12. Two 68020 Processors sharing 1MByte of DRAM

74F764-1 FAMILY LINE DRIVING CHARACTERISTICS

The 74F764-1/765-1 are designed to provide first reflected wave switching with as wide a range of characteristic impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP-housed memory arrays is usually around 70Ω. If a signal line has settled out in a High state at 4 volts and must be pulled down to 0.8 volts or less on the incident wave, the DRAM controller output must sink (4-0.8)/70A or 46mA at 0.8 volts. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be switched on the incident wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady state operation at these currents may result in electromigration).

Figures 13 and 14 show the output I/V characteristics of the DRAM controller family of devices. These figures also demonstrate a graphical method for determining the first reflected wave characteristics of the devices.

When driving any type of memory arrays with the 74F764-1/765-1, the schottky diode termination shown in Figure 15 can be used (most of these will need no termination at all).

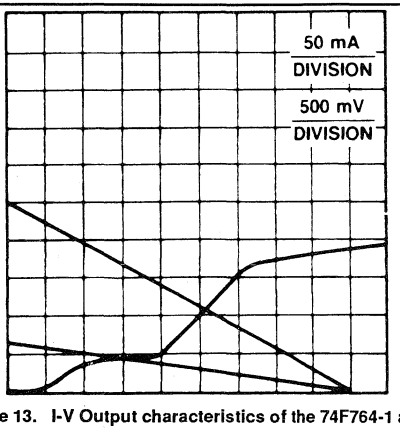


Figure 13. I-V Output characteristics of the 74F764-1 and 765-1 in the Low State. Any unterminated line impedance between 18Ω and 70Ω (both shown) will typically switch on the first reflected wave without violating the -1V minimum input voltage specification typical of DRAMs.

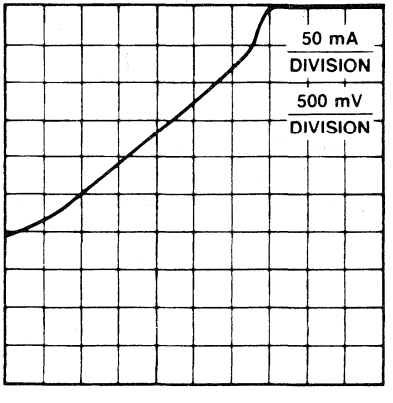


Figure 14. I-V Output characteristics of the 74F764-1 and 765-1 while in the High state.

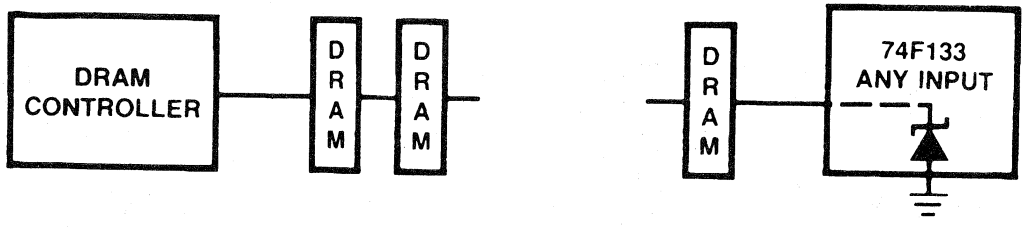


Figure 15.

Pi–bus transceiver | 74F776

FEATURES

- Octal latched transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with Pi–bus and IEEE 896 Futurebus standards
- Built–in precision band–gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch–free power up/power down operation
- Multiple package options
- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F776	6.5ns	80mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
28–pin plastic DIP (600 mil)[1]	N74F776N	I74F776N
28–pin PLCC[1]	N74F776A	I74F776A

Note to ordering information

1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	PNP latched inputs	3.5/0.117	70µA/70µA
B0 – B7	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA	A output enable input (active high)	1.0/0.033	20µA/20µA
$\overline{OEB0}$, $\overline{OEB1}$	B output enable inputs (active low)	1.0/0.033	20µA/20µA
$\overline{LE}$	Latch enable input (active low)	1.0/0.033	20µA/20µA
A0 – A7	3–state outputs	150/40	3mA/24mA
B0 – B7	Open collector outputs	OC/166.7	OC/100mA

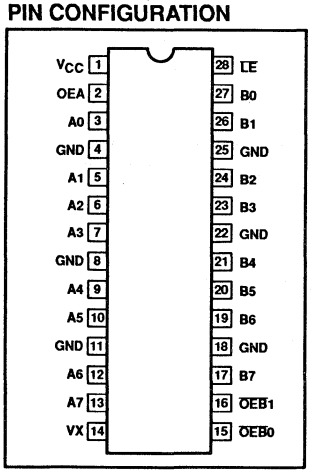
Notes to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.
2. OC = Open collector.

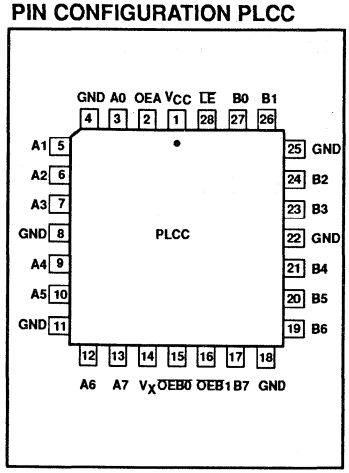
DESCRIPTION

The 74F776 is an octal bidirectional latched transceiver and is intended to provide the electrical interface to a high performance wired–OR bus. The B port inverting drivers are low–capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a 100 mV threshold region and a 4ns glitch filter. (Continues)

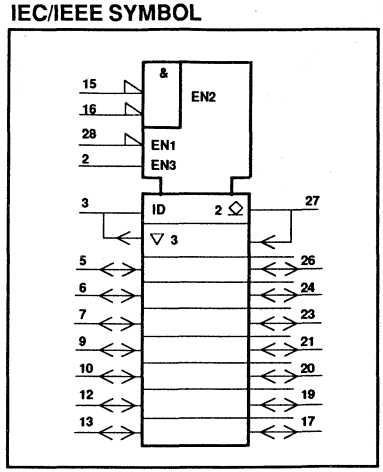
PIN CONFIGURATION



PIN CONFIGURATION PLCC



IEC/IEEE SYMBOL



DESCRIPTION (CONTINUED)

The 74F776 B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading. Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is less for BTL, so is its receiver threshold, therefore noise margins are excellent.

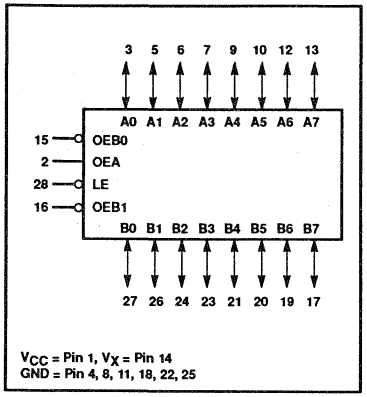
BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F776 A port has TTL 3–state drivers and TTL receivers with a latch function. A separate high–level control voltage input (V_X) is provided to limit the A side output level to a given voltage level (such as 3.3V). For 5.0V systems, V_X is simply tied to V_{CC}.

The 74F776 has a designed feature to control the B output transitions during power sequencing. There are two possible sequencing, They are as follows:

1. When $\overline{LE}$ = low and $\overline{OEB}n$ = low then the B outputs are disabled until the $\overline{LE}$ circuitry takes control. Then the B outputs will follow the A inputs, making a maximum of one transition during power–up (or down).
2. If $\overline{LE}$ = high or $\overline{OEB}n$ = high then the B outputs will be disabled during power–up (or down).

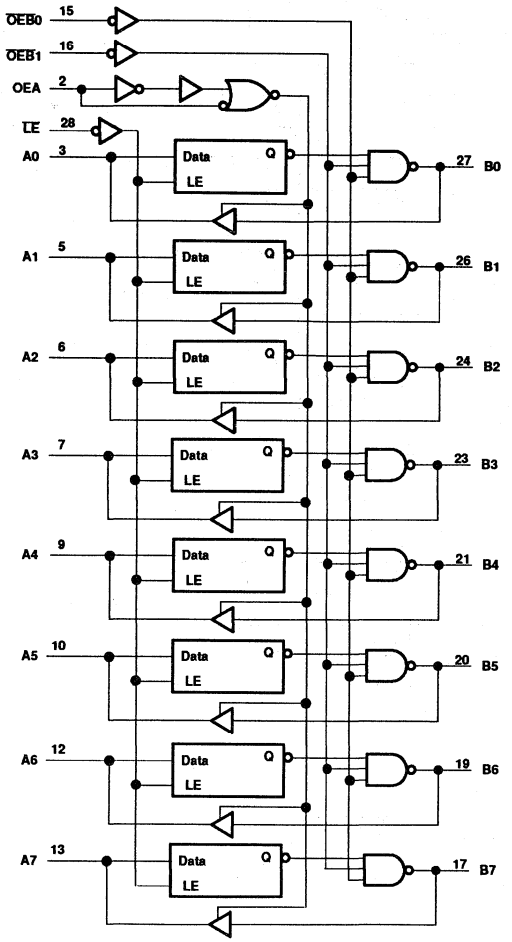
LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A0 – A7	3, 5, 6, 7, 9, 10, 12, 13	I/O	PNP latched input/3–state output (with V_X control option)
B0 – B7	27, 26, 24, 23, 21, 20, 19, 17	I/O	Data input with special threshold circuitry to reject noise/ open collector output, high current drive
$\overline{OEB0}$	15	Input	Enables the B outputs when both pins are low
$\overline{OEB1}$	16	Input	
OEA	2	Input	Enables the A outputs when high
$\overline{LE}$	28	Input	Latched when high (a special feature is builit in for proper enabling times)
V_X	14	Input	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{cc}$ for normal use)

LOGIC DIAGRAM



V_{CC} = Pin 1, V_X = Pin 14,
GND = Pin 4, 8, 11, 18, 22, 25

FUNCTION TABLE

INPUTS						LATCH	OUTPUTS		OPERATING MODE
An	Bn*	$\overline{LE}$	OEA	$\overline{OEB0}$	$\overline{OEB1}$	STATE	An	Bn	
H	X	L	L	L	L	H	Z	Z	A 3–state, data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	A 3–state, latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
–	L	H	H	L	L	H (2)	L	Z(2)	
–	–	H	H	L	L	Qn	Qn	Qn	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3–state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Qn	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3–state, data from B to A
–	L	L	H	H	X	L	L	Z	
–	H	H	H	H	X	Qn	H	Z	
–	L	H	H	H	X	Qn	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3–state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Qn	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3–state, data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Qn	H	Z	
–	L	H	H	X	H	Qn	L	Z	

Notes to function table

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. – = Input not externally driven
5. Z = High impedance "off" state
6. Q_n = High or Low voltage level one setup time prior to the low–to–high $\overline{LE}$ transition.
7. (1) = Condition will cause a feedback loop path: A to B and B to A.
8. (2) = The latch must be preconditioned such that B inputs may assume a high or low level while $\overline{OEB0}$ and $\overline{OEB1}$ are low and $\overline{LE}$ is high.
9. B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_X	Threshold control		–0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}$n, OEA, $\overline{LE}$	–0.5 to +7.0	V
		A0 – A7, B0 – B7	–0.5 to +5.5	V
I_{IN}	Input current		–40 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	A0 – A7	48	mA
		B0 – B7	200	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Except B0 – B7	2.0			V
		B0 – B7	1.6			V
V_{IL}	Low–level input voltage	Except B0 – B7			0.8	V
		B0 – B7			1.45	V
I_{ik}	Input clamp current	Except A0 – A7			–18	mA
		A0 – A7			–40	mA
I_{OH}	High–level output current	A0 – A7			–3	mA
I_{OL}	Low–level output current	A0 – A7			24	mA
		B0 – B7			100	mA
T_{amb}	Operating free air temperature	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
I_{OH}	High–level output current	B0 – B7	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power–off output current	B0 – B7	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High–level output voltage	A0 – A7[4]	V_{CC} = MIN,	I_{OH} = –3mA, V_X = V_{CC}	2.5		V_{CC}	V
			V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –4mA, V_X = 3.13V and 3.47V	2.5			V
V_{OL}	Low–level output voltage	A0 – A7[4]	V_{CC} = MIN,	I_{OL} = 20mA, V_X = V_{CC}			0.50	V
		B0 – B7	V_{IL} = MAX	I_{OL} = 100mA			1.15	V
			V_{IH} = MIN	I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A0 – A7	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A0 – A7	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		A0 – A7, B0 – B7	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High–level input current	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 2.7V, Bn –An =0V				20	µA
		B0 – B7	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low–level input current	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 0.5V				–20	µA
		B0 – B7	V_{CC} = MAX, V_I = 0.3V				–100	µA
I_{OZH} + I_{IH}	Off state output current, high level voltage applied	A0 – A7	V_{CC} = MAX, V_O = 2.7V				70	µA
I_{OZL} + I_{IL}	Off state output current, low level voltage applied	A0 – A7	V_{CC} = MAX, V_O = 0.5V				–70	µA
I_X	High–level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA = $\overline{OEB}$n = 2.7V, A0 – A7 = 2.7V, B0 – B7 = 2.0V,		–100		100	µA
			V_{CC} = MAX, V_X = 3.13 & 3.47V, $\overline{LE}$ = OEA = 2.7V, $\overline{OEB}$n = A0 – A7 = 2.7V, B0 – B7 = 2.0V,		–10		10	µA
I_{OS}	Short circuit output current[3]	A0 – A7 only	V_{CC} = MAX, Bn = 1.8V, OEA = 2.0V, $\overline{OEB}$n = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			65	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}				75	100	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} =1.8v and V_{IL} = 1.3V.

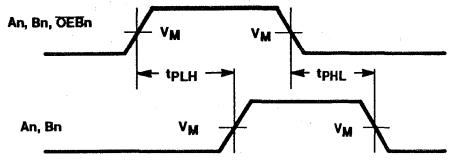
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1	5.5 4.5	8.0 6.0	12.0 9.0	5.5 4.5	12.0 9.0	5.5 4.5	12.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low, OEA to An	Waveform 3, 4	8.0 8.5	10.5 11.0	13.5 13.5	7.5 8.0	15.0 15.5	7.5 8.0	15.5 15.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low, OEA to An	Waveform 3, 4	2.0 2.0	3.5 4.5	6.0 7.0	1.5 2.0	6.5 7.5	1.5 2.0	6.5 7.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D = 30pF, R_U = 9Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1	3.0 3.0	5.0 4.5	7.0 7.5	2.5 2.5	8.0 8.5	2.0 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to Bn	Waveform 1	3.5 3.5	5.0 5.0	8.0 8.0	3.0 2.5	9.0 9.0	2.5 2.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}$n to An	Waveform 1	3.0 3.5	4.5 5.5	7.0 9.0	2.5 3.5	8.0 10.0	2.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B port 1.3V to 1.7V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	5.0 4.5	0.5 0.5	5.0 4.5	ns

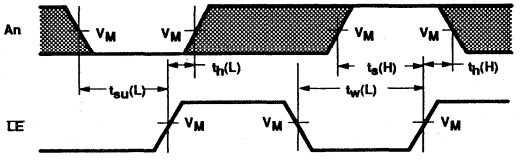
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An to $\overline{CE}$	Waveform 2	3.5 4.5			4.5 5.0		4.5 5.0		ns
t_h(H) t_h(L)	Hold time, high or low An to $\overline{CE}$	Waveform 2	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_w (L)	$\overline{CE}$ pulse width, low	Waveform 2	4.0			5.0		5.0		ns

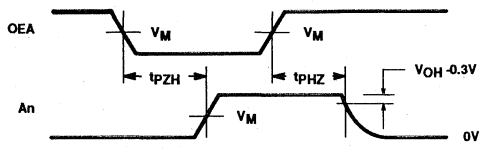
AC WAVEFORMS



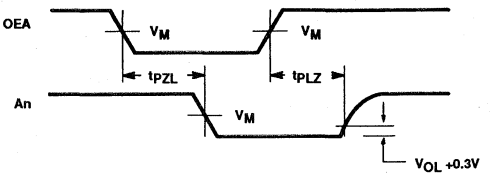
Waveform 1. Propagation delay for data to output



Waveform 2. Data setup and hold times and $\overline{LE}$ pulse width



Waveform 3. 3-state output enable time to high level and output disable time from high level



Waveform 4. 3-state output enable time to low level and output disable time from low level

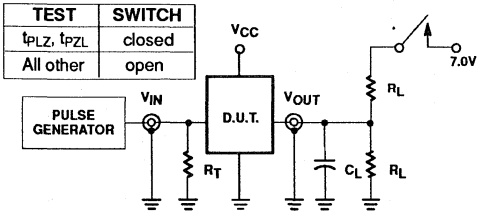
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

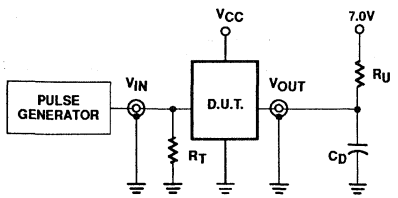
TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

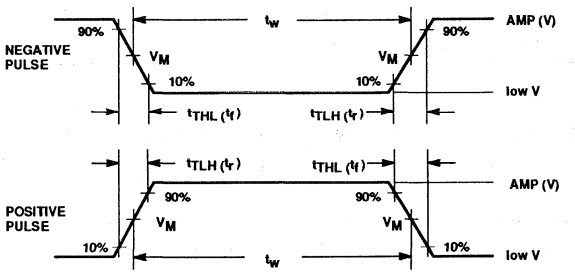
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–state outputs on A port



Test circuit for outputs on B port



Input pulse definition

family	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	2.0V	1.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_U = Pull up resistor; see AC electrical characteristics for value.
C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Triple bidirectional latched bus transceiver (3–State + Open Collector)

74F777

FEATURES

- Latching transceiver
- High drive Open Collector output current with minimum output swing
- Compatible with Test Mode (TM) bus specification
- Controlled output ramp
- Multiple package options
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F777 is a triple bidirectional latched bus transceiver and is intended to provide the electrical interface to a high performance wired–OR bus. This bus has a loaded characteristics impedance range of 20 to 50 ohms and is terminated on each end with a 30 to 40 ohm resistor.

The 74F777 is a triple bidirectional transceiver with Open Collector B and 3–State A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100mA from 2 volts to minimize crosstalk and ringing on the bus.

A separate output threshold clamp voltage (V_X) is provided to prevent the A port output High level from exceeding future high density processor supply voltage levels. For 5 volt systems, V_X is simply tied to V_{CC}.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F777	7.0ns	45mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
20–pin plastic DIP (300 mil)	N74F777N	I74F777N
20–pin PLCC	N74F777A	I74F777A

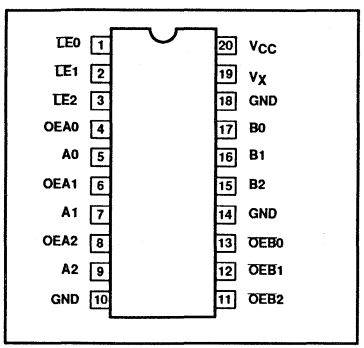
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A2	PNP latched inputs	3.5/0.117	70µA/70µA
B0 – B2	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA0 – OEA2	A output enable inputs (active–High)	1.0/0.033	20µA/20µA
$\overline{OEB0}$ – $\overline{OEB2}$	B output enable inputs (active–Low)	1.0/0.033	20µA/20µA
$\overline{LE0}$ – $\overline{LE2}$	Latch enable inputs (active–Low)	1.0/0.033	20µA/20µA
A0 – A2	3–State outputs	150/40	3mA/24mA
B0 – B2	Open Collector outputs	OC/166.7	OC/100mA

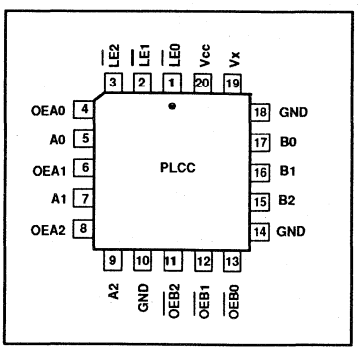
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.
2. OC = Open Collector.

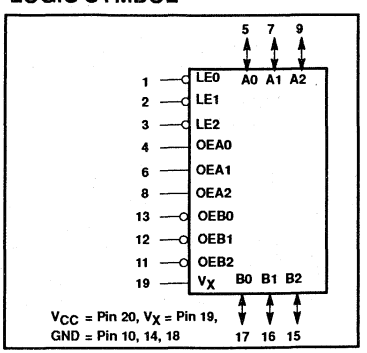
PIN CONFIGURATION



PIN CONFIGURATION PLCC

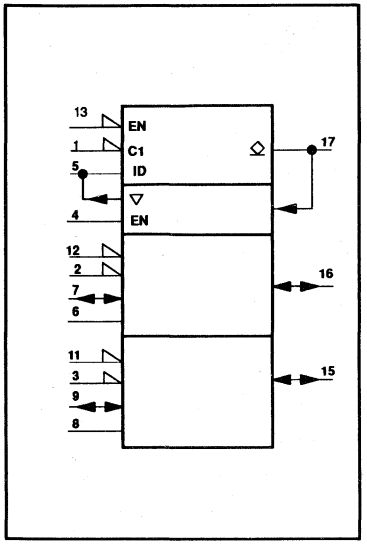


LOGIC SYMBOL

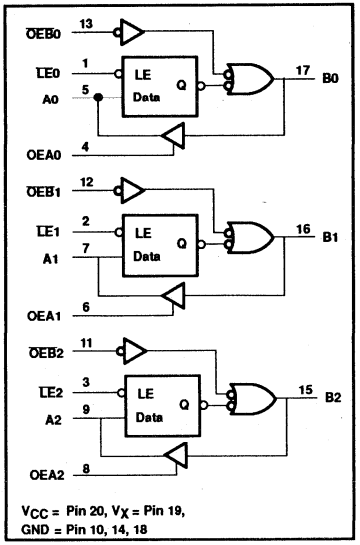


Triple bidirectional latched bus transceiver (3–State + Open Collector) 74F777

IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					LATCH	OUTPUTS		OPERATING MODE
An	Bn*	$\overline{LE}$n	OEAn	$\overline{OEB}$n	STATE	An	Bn	
H	X	L	L	L	H	Z	H**	A 3–State, data from A to B
L	X	L	L	L	L	Z	L	
X	X	H	L	L	Qn	Z	Qn	A 3–State, latched data to B
–	–	L	H	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
–	L	H	H	L	H (2)	L	Z(2)	
–	–	H	H	L	Qn	Qn	Qn	Latch state to A and B
H	X	L	L	H	H	Z	Z	B and A 3–State
L	X	L	L	H	L	Z	Z	
X	X	H	L	H	Qn	Z	Z	
–	H	L	H	H	H	H	Z	B 3–State, data from B to A
–	L	L	H	H	L	L	Z	
–	H	H	H	H	Qn	H	Z	
–	L	H	H	H	Qn	L	Z	

Notes to function table

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. – = Input not externally driven
5. Z = High impedance (off) state
6. Q_n = High or Low voltage level one setup time prior to the Low–to–High $\overline{LE}$ transition.
7. (1) = Condition will cause a feedback loop path: A to B and B to A.
8. (2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}$0 and $\overline{OEB}$1 are Low and $\overline{LE}$ is High.
9. B_n* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to Low state.
10. H** = Goes to level of pullup voltage.
11. Each latch is independent. The latches may be run in any combination of modes.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_X	Threshold control		–0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEBn}$, OEAn, $\overline{LEn}$	–0.5 to +7.0	V
		A0 – A2, B0 – B2	–0.5 to +5.5	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A0 – A2	48	mA
		B0 – B2	200	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Except B0 – B2	2.0			V
		B0 – B2	1.6			V
V_{IL}	Low–level input voltage	Except B0 – B2			0.8	V
		B0 – B2			1.43	V
I_{Ik}	Input clamp current	Except A0 – A2			–18	mA
		A0 – A2			–40	mA
I_{OH}	High–level output current	Except A0 – A2			–3	mA
I_{OL}	Low–level output current	A0 – A2			24	mA
		B0 – B2			100	mA
T_{amb}	Operating free–air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
I_{OH}	High–level output current	B0 – B2	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power–off output current	B0 – B2	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A0 – A2[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA, V_X = V_{CC}	2.5		V_{CC}	V
				I_{OH} = –4mA, V_X = 3.13V and 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A0 – A2[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA, V_X = V_{CC}			0.50	V
		B0 – B2		I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A0 – A2	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A0 – A2	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}$n, OEAn, $\overline{LE}$n	V_{CC} = MAX, V_I = 7.0V				100	µA
		A0 – A2, B0 – B2	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High–level input current	$\overline{OEB}$n, OEAn, $\overline{LE}$n	V_{CC} = MAX, V_I = 2.7V, Bn – An = 0V				20	µA
		B0 – B2	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low–level input current	$\overline{OEB}$n, OEAn $\overline{LE}$n	V_{CC} = MAX, V_I = 0.5V				–20	µA
		B0 – B2	V_{CC} = MAX, V_I = 0.3V				–100	µA
I_{OZH} + I_{IH}	Off–state output current, High level voltage applied	A0 – A2	V_{CC} = MAX, V_O = 2.7V				70	µA
I_{OZL} + I_{IL}	Off–state output current, Low level voltage applied	A0 – A2	V_{CC} = MAX, V_I = 0.5V				–70	µA
I_X	High level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEAn = $\overline{OEB}$n = 2.7V, A0 – A2 = 2.7V, B0 – B2 = 2.0V,		–100		100	µA
			V_{CC} = MAX, V_X = 3.13 & 3.47V, $\overline{LE}$ = OEAn = 2.7V, $\overline{OEB}$n = A0 – A2 = 2.7V, B0 – B2 = 2.0V		–10		10	µA
I_{OS}	Short circuit output current[3]	A0 – A2 only	V_{CC} = MAX, Bn = 1.8V, OEAn = 2.0V, $\overline{OEB}$n = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			40	60	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			55	80	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			45	67	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test condition.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} =1.8v and V_{IL} = 1.3V.

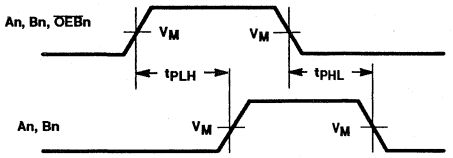
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 30pF, R_L = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 30pF, R_L = 9Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±10%, C_L = 30pF, R_L = 9Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1	8.5 7.5	10.5 9.5	13.0 12.0	8.0 7.5	14.5 12.5	8.0 7.5	14.5 12.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low $\overline{OE}$An to An	Waveform 3, 4	8.0 9.0	10.0 11.0	13.0 14.0	7.0 8.0	14.5 15.5	7.0 8.0	14.5 15.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low $\overline{OE}$An to An	Waveform 3, 4	1.5 1.5	3.0 3.0	6.0 6.0	1.0 1.0	6.5 6.0	1.0 1.0	6.5 6.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D = 30pF, R_U = 9Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±10%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1	3.0 5.0	4.5 6.5	7.0 9.0	2.5 4.5	8.0 10.0	2.5 4.5	8.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$n to Bn	Waveform 1	3.5 5.5	5.5 7.5	8.0 10.5	3.0 5.0	9.0 11.5	3.0 5.0	9.0 11.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OE}$Bn to An	Waveform 1	3.0 6.0	5.0 8.0	7.5 10.5	3.0 5.5	8.0 12.0	3.0 5.5	8.0 12.0	ns
t_{TLH} t_{THL}	Transition time, B port 1.3V to 1.7V, 1.7V to 1.3V	Test Circuits and Waveforms	0.5 0.5	4.0 2.0	4.5 4.5	0.5 0.5	7.0 4.5	0.5 0.5	7.0 4.5	ns

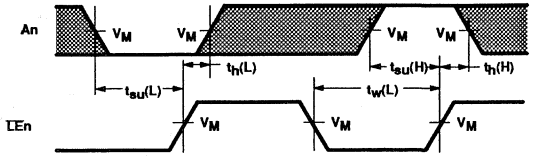
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D = 30pF, R_U = 9Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±10%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time An to $\overline{LE}$n	Waveform 2	4.0 4.5			4.5 4.5		4.5 4.5		ns
t_h (H) t_h (L)	Hold time An to $\overline{LE}$n	Waveform 2	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_w (L)	$\overline{LE}$n pulse width, Low	Waveform 2	5.5			6.5		6.5		ns

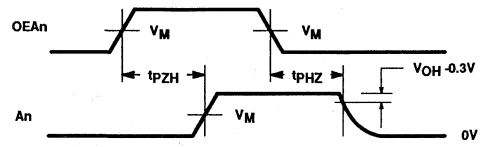
AC WAVEFORMS



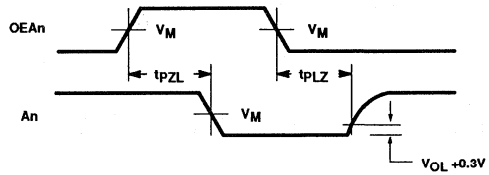
Waveform 1. Propagation delay, data to output and enable/disable time $\overline{OEB}$n to Bn



Waveform 2. Data set-up and hold times and $\overline{LE}$ pulse width



Waveform 3. 3-State output enable time to High level and output disable time from High level



Waveform 4. 3-State output enable time to Low level and output disable time from Low level

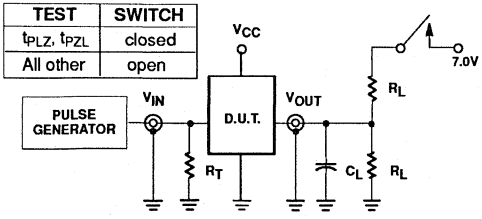
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

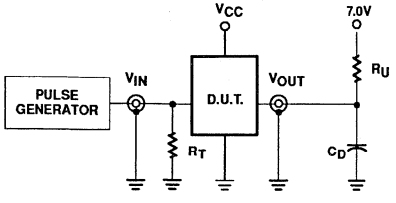
TEST CIRCUITS AND WAVEFORMS

SWITCH POSITION

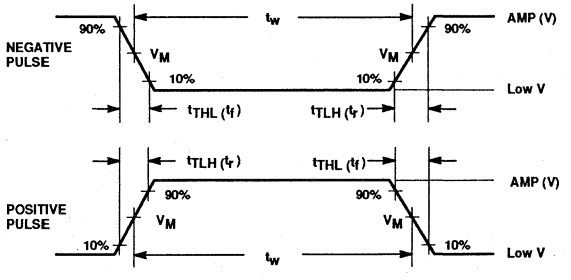
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–State outputs on A port



Test circuit for outputs on B port



Input pulse definition

family	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	2.0V	1.0V	1.5V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_U = Pull up resistor; see AC electrical characteristics for value.
C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

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Date of issue	September 20, 1989
Status	Product Specification
FAST Products	

FAST 74F779 Counter

8-Bit Bidirectional Binary Counter (3-state)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F779	145MHz	90mA

FEATURES

- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built-in look-ahead carry capability**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 145MHz typical**
- **Supply current 90mA typical**
- **See 'F269 for 24 pin separate I/O port version**
- **See 'F579 for 20 pin version**
- **See 'F1779 for extended function version of the 'F799**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F779N
16-Pin Plastic SOL	N74F779D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

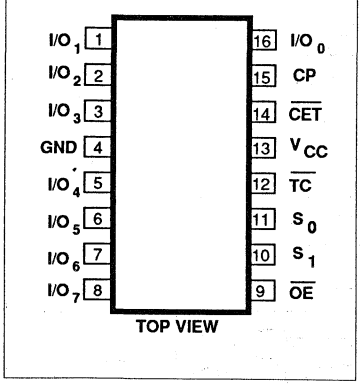
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70μA/0.6mA
	Data outputs	150/40	3.0mA/24mA
S_0, S_1	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20μA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

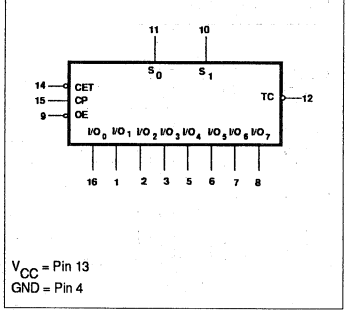
DESCRIPTION

The 74F779 is fully synchronous 8-stage Up/Down Counter with multiplexed 3-state I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0,S_1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock. When $\overline{CET}$ is HIgh the data outputs are held in their current state and $\overline{TC}$ is held High. The $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

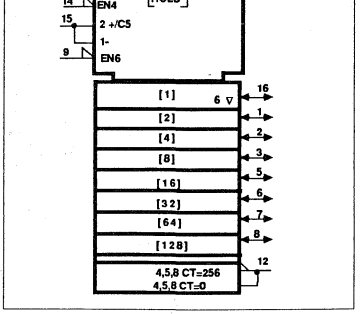
PIN CONFIGURATION



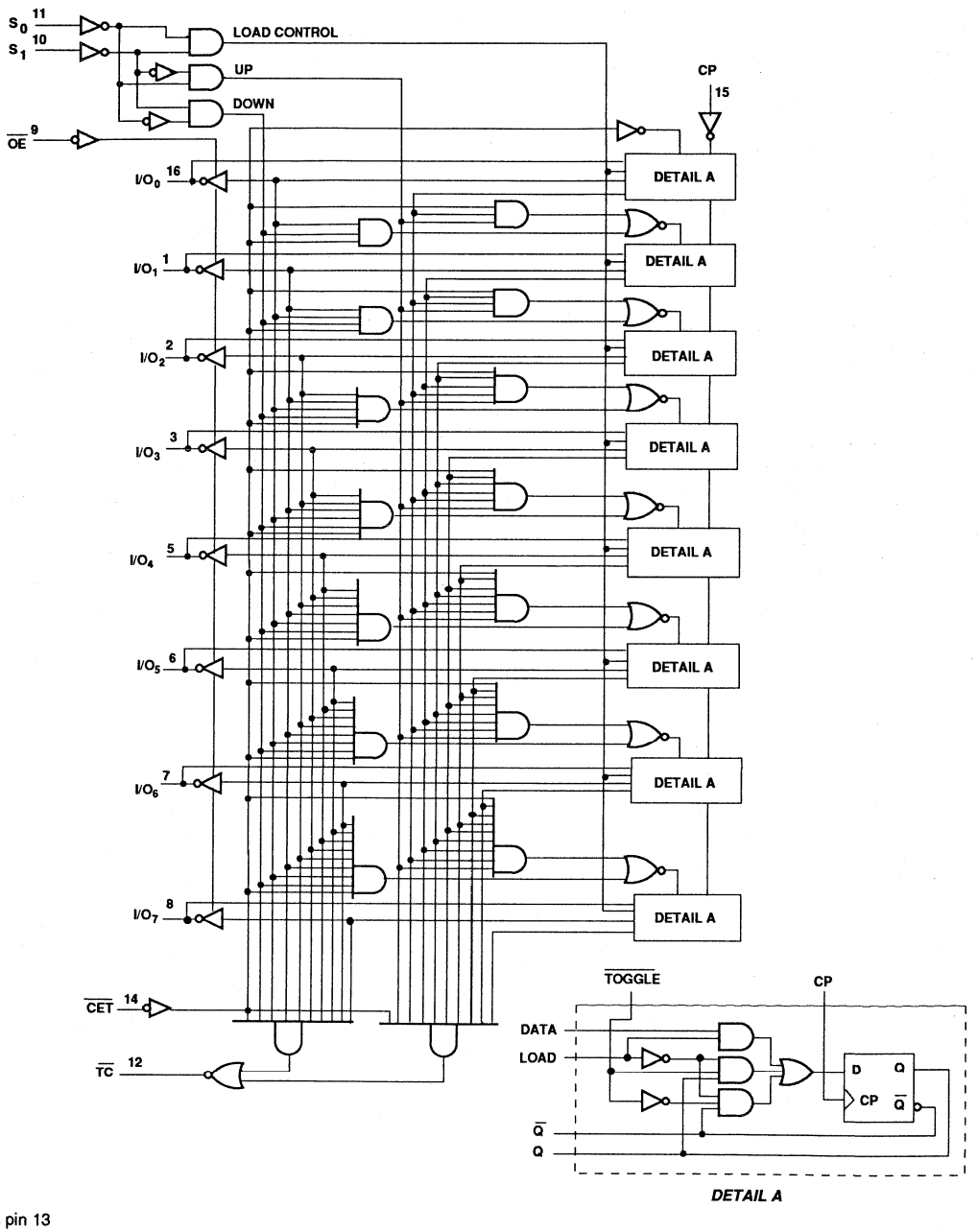
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 13
GND= pin 4

FUNCTION TABLE

INPUTS					OPERATING MODE
S_1	S_0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/O_0 to I/O_7 in high impedance
X	X	X	L	X	Flip-flop outputs appears on I/O lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held High)
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = S_0 and S_1 should never be Low voltage level at the same time in the hold mode only.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage	I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
		others	V_{CC} = 5.5V, V_I =7.0V					100	µA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	I/O_n	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{II}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				82	116	mA
		I_{CCL}					91	128	mA
		I_{CCZ}					97	136	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

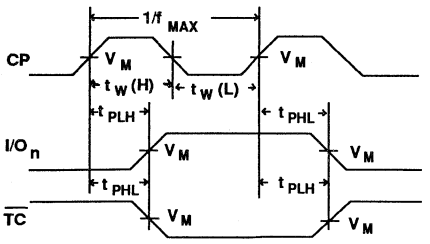
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	125	145		115		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.5 5.5	7.0 8.0	10.5 10.5	4.5 5.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 4.5	7.0 7.0	9.0 9.0	4.5 4.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.0 3.0	4.5 5.5	6.5 7.5	2.5 2.5	7.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	2.5 4.5	4.5 6.5	7.0 9.0	2.5 4.5	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.5 7.0	1.0 1.0	8.0 8.0	ns

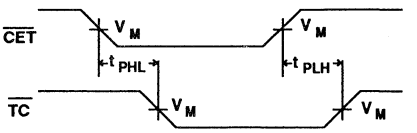
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ to CP	Waveform 3	5.0 5.5			5.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 3	8.0 8.0			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 4.0			4.0 4.0		ns

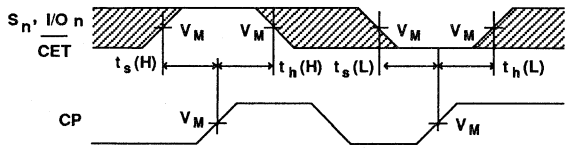
AC WAVEFORMS



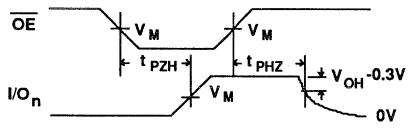
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



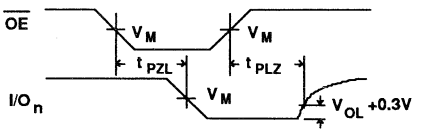
Waveform 2.
Propagation Delay, $\overline{CET}$ input to Terminal Count Output



Waveform 3. Data Setup And Hold Times



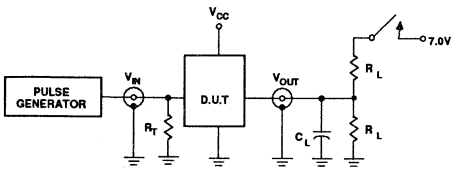
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

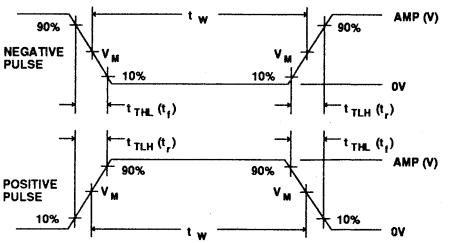
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

4-Bit asynchronous bus arbiter — 74F786

FEATURES

- Arbitrates between 4 asynchronous inputs
- Separate grant output for each input
- Common output enable
- On board 4 input AND gate
- Metastable–free outputs
- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F786	6.6ns	55mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
16–pin plastic DIP	N74F786N	I74F786N
16–pin plastic SO	N74F786D	I74F786D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{BR}0 - \overline{BR}3$	Bus request inputs (active low)	1.0/3.0	20µA/1.8mA
A, B, C, D	AND gate inputs	1.0/1.0	20µA/0.6mA
$\overline{EN}$	Common bus grant output enable input (active low)	1.0/1.0	20µA/0.6mA
YOUT	AND gate output	150/40	3.0mA/24mA
$\overline{BG}0 - \overline{BG}3$	Bus grant outputs (active low)	150/40	3.0mA/24mA

Note to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

DESCRIPTION

The 74F786 is an asynchronous 4–bit arbiter designed for high speed real–time applications. The priority of arbitration is determined on a first–come first–served basis. Separate bus grant ($\overline{BG}n$) outputs are available to indicate which one of the request inputs is served by the arbitration logic. All $\overline{BG}n$ outputs are enabled by a common enable ($\overline{EN}$) pin. In order to generate a bus request signal a separate 4 input AND gate is provided which may also be used as an independent AND gate. Unused bus request ($\overline{BR}$) inputs may be disabled by tying them high.

The 74F786 is designed so that contention between two or more request signals will not glitch or display a metastable condition. In this situation an increase in the $\overline{BR}n$ to $\overline{BG}n$ t_{PHL} may be observed. A typical 74F786 has an h = 6.6ns, t = 0.41ns and To = 5µsec.

Where:

h = Typical propagation delay through the device and t and To are device parameters derived from test results and can most nearly be defined as:

t = A function of the rate at which a latch in a metastable state resolves that condition.

To = A function of the measurement of the propensity of a latch to enter a metastable state. To is also a very strong function of the normal propagation delay of the device.

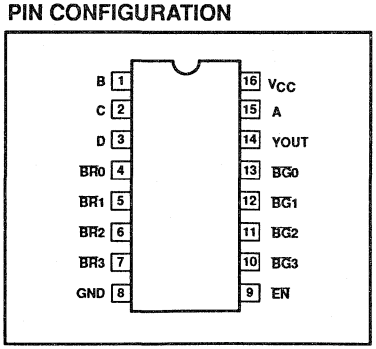
For further information, please refer to the 74F786 application notes.

FUNCTIONAL DESCRIPTION

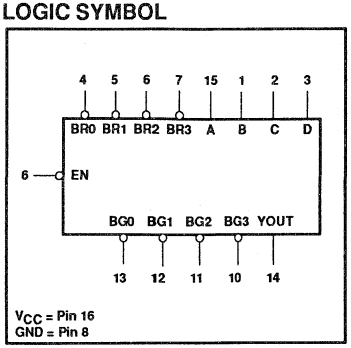
The $\overline{BR}n$ inputs have no inherent priority. The arbiter assigns priority to the incoming requests as they are received, therefore, the first $\overline{BR}$ asserted will have the highest priority. When a bus request is received its corresponding bus grant becomes active, provided that $\overline{EN}$ is low. If additional bus requests are made during this time they are queued. When the first request is removed, the arbiter services the bus request with the next highest priority. Removing a request while a previous request is being serviced can cause a grant to be changed when arbitrating between three or four requests. For that reason, the user should not remove ungranted requests when arbitrating between three or four requests. This does not apply to arbitration between two requests.

If two or more $\overline{BR}n$ inputs are asserted at precisely the same time, one of them will be selected at random, and all $\overline{BG}n$ outputs will be held in the high state until the selection is made. This guarantees that an erroneous $\overline{BG}n$ will not be generated even though a metastable condition may occur internal to the device. When the $\overline{EN}$ is in the high state the $\overline{BG}n$ outputs are forced high.

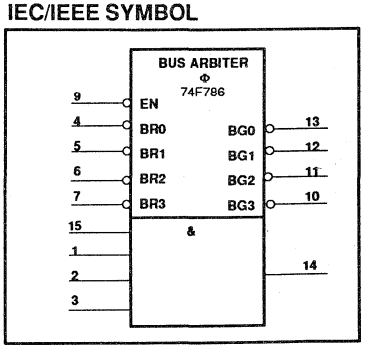
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME	FUNCTION
$\overline{BR0} - \overline{BR3}$	4, 5, 6, 7	Input	Bus request inputs (active low)	The logic of this device arbitrates between these four inputs. Unused inputs should be tied high.
A, B, C, D	15, 1, 2, 3	Input	Inputs of the 4–input AND gate	
$\overline{EN}$	9	Input	Enable input	When low it enables the $\overline{BG0} - \overline{BG3}$ outputs.
$\overline{BG0} - \overline{BG3}$	13, 12, 11, 10	Output	Bus grant outputs (active low)	These outputs indicate the selected bus request. $\overline{BG0}$ corresponds to $\overline{BR0}$, $\overline{BG1}$ to $\overline{BR1}$, etc.
YOUT	14	Output	Output of the 4–input AND gate	
GND	8	Ground	ground (0V)	
V_{CC}	16	Power	Positive supply voltages	

ARBITER FUNCTION TABLE

INPUTS					OUTPUTS			
$\overline{EN}$	$\overline{BR0}$	$\overline{BR1}$	$\overline{BR2}$	$\overline{BR3}$	$\overline{BG0}$	$\overline{BG1}$	$\overline{BG2}$	$\overline{BG3}$
L	1	X	X	X	L	H	H	H
L	X	1	X	X	H	L	H	H
L	X	X	1	X	H	H	L	H
L	X	X	X	1	H	H	H	L
H	X	X	X	X	H	H	H	H

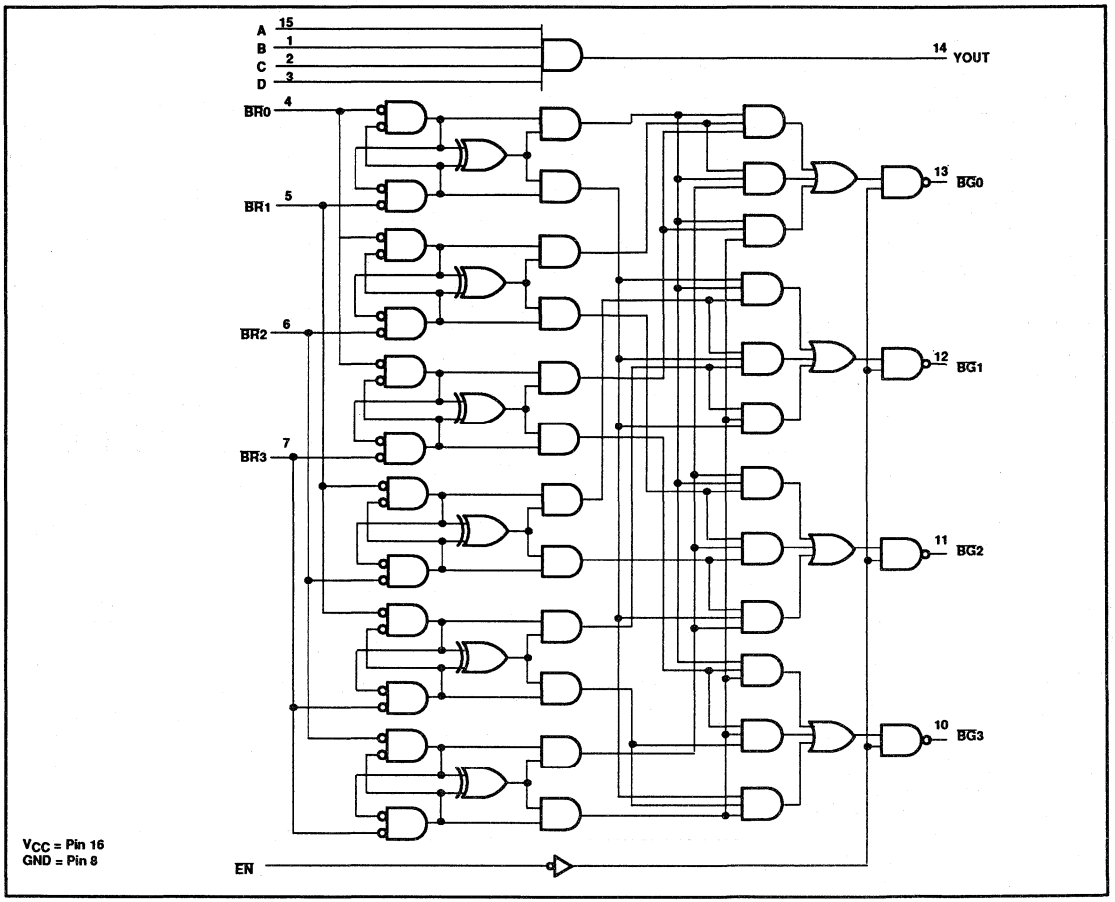
Notes to mode selection function table
1. H = High–voltage level
2. L = Low–voltage level
3. X = Don't care
4. 1 = First of inputs to go low

ARBITER FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	YOUT
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

Notes to AND function table
1. H = High–voltage level
2. L = Low–voltage level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		48	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				24	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN		±5%V_{CC}	2.7	3.3		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	A – D, $\overline{EN}$	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{BRn}$						-1.8	mA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				55	80	mA

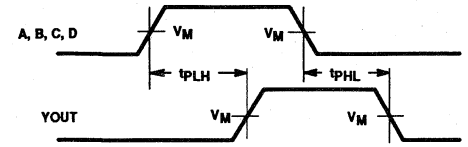
Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

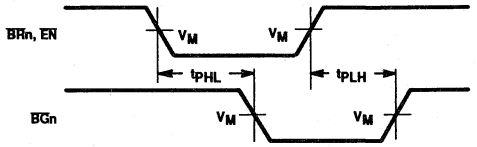
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay, A, B, C, D to YOUT	Waveform 1	2.5 2.5	4.5 4.5	7.5 7.5	2.0 2.5	8.5 7.5	2.0 2.5	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{BRn}$ to $\overline{BGn}$	Waveform 2	5.0 4.5	7.0 6.5	10.0 9.5	4.5 4.0	10.5 10.0	4.5 4.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{EN}$ to $\overline{BGn}$	Waveform 2	3.0 2.5	5.0 4.5	8.0 7.5	2.5 2.5	8.5 8.0	2.5 2.5	8.5 8.0	ns
t_{PHL}	Propagation delay, $\overline{BRa}$ to $\overline{BGb}$	Waveform 2	5.0	7.0	10.0	4.5	10.5	4.5	10.5	ns

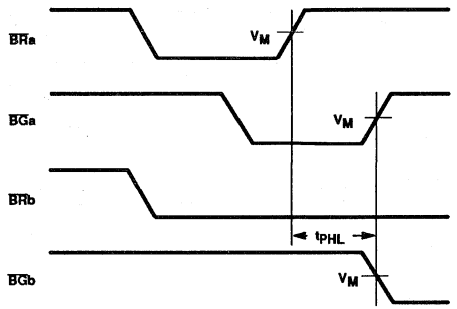
AC WAVEFORMS



Waveform 1. Propagation delay for AND gate to output



Waveform 2. Propagation delay for bus request or enable to bus grant output

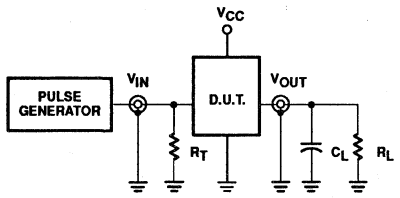


Waveform 3. Propagation delay for bus request to bus grant output

Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. a and b represents any of the bus requests or grants. $\overline{BG}$a low–to–high transition and the $\overline{BG}$b high–to–low transition occur simultaneously.

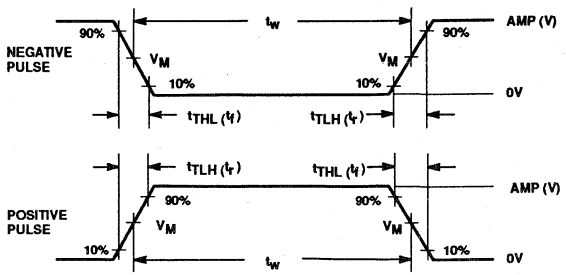
TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Hex 2-input NAND drivers | 74F804/1804

FEATURES

- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND – 74F804
  Center V_{CC} and GND – 74F1804
- Typical propagation delay of 2.5ns

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F804	2.5ns	9mA
74F1804	2.5ns	9mA

ORDERING INFORMATION

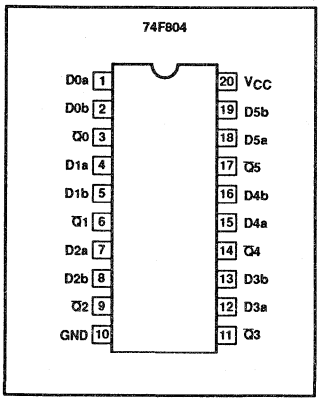
DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20–pin plastic DIP	N74F804N, N74F1804N
20–pin plastic SOL	N74F804D, N74F1804D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

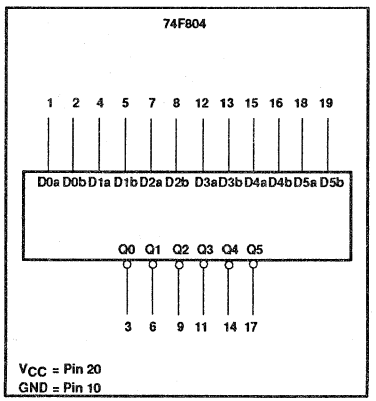
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna – Dnb	Data inputs	1.0/0.033	20µA/20µA
$\overline{Q}0 - \overline{Q}5$	Data outputs	2400/80	48mA/48mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

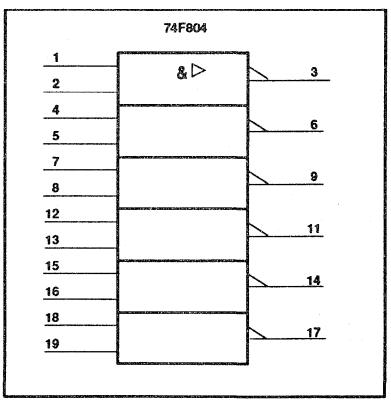
PIN CONFIGURATION



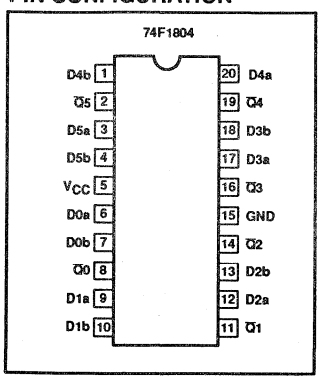
LOGIC SYMBOL



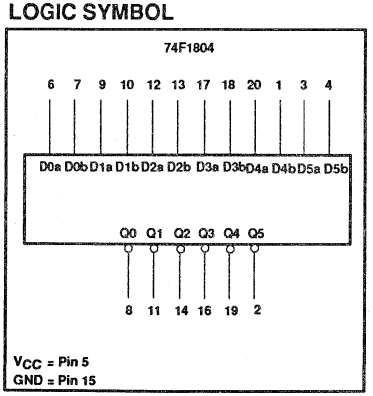
IEC/IEEE SYMBOL



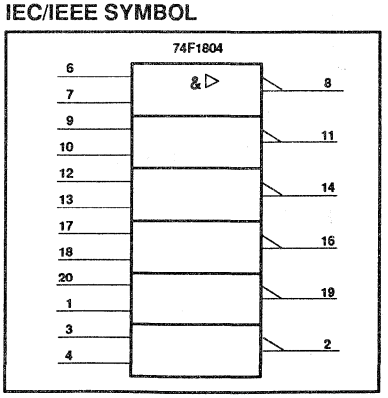
PIN CONFIGURATION



LOGIC SYMBOL

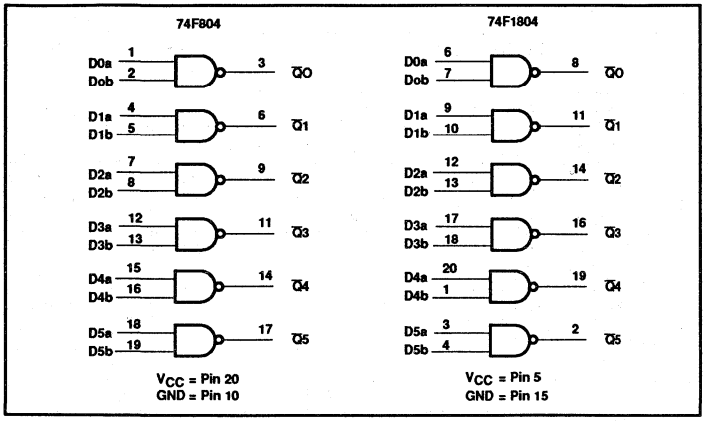


IEC/IEEE SYMBOL



Hex 2-input NAND drivers 74F804/1804

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
Da	Db	$\overline{Q}$
H	H	L
L	X	H
X	L	H

NOTES:
2. H = High voltage level
3. L = Low voltage level
4. X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free–air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–48	mA
I_{OL}	Low–level output current			48	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX		-60		-160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		2.0	3.0	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		15	20	mA

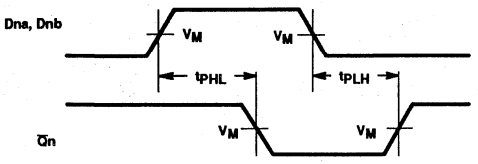
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

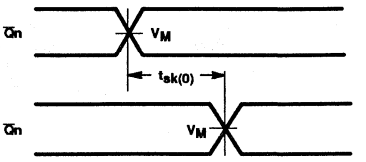
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Qn}$	Waveform 1	1.0 1.0	2.0 3.0	4.0 4.5	1.0 1.0	4.0 5.0	ns
$t_{sk(o)}$	Output skew[1,2]	Waveform 2			1.5		1.5	ns

NOTES:
1. [t_{PN} actual – t_{PM} actual] for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



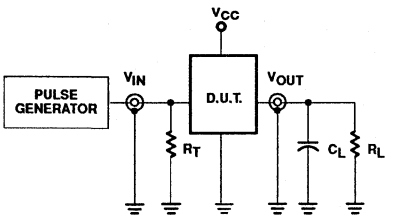
Waveform 1. Propagation delay for inverting outputs



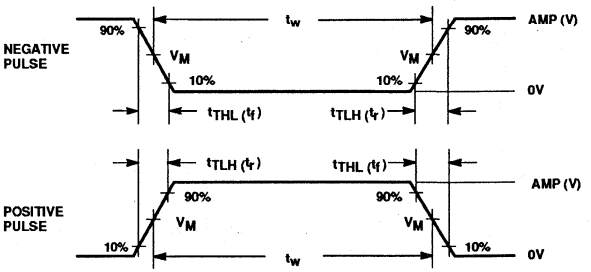
Waveform 2. Output skew

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	v_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Hex 2-input NOR drivers — 74F805/74F1805

FEATURES

- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND – 74F805
  Center V_{CC} and GND – 74F1805
- Typical propagation delay of 2.3ns

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F805	2.3ns	10mA
74F1805	2.3ns	10mA

ORDERING INFORMATION

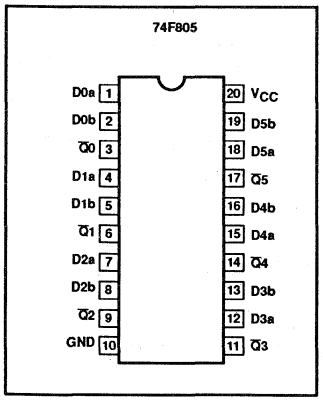
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20–pin plastic DIP	N74F805N, N74F1805N
20–pin plastic SOL	N74F805D, N74F1805D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

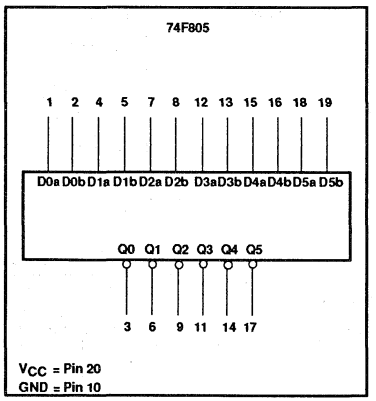
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna – Dnb	Data inputs	1.0/0.033	20µA/20µA
$\overline{Q}0 - \overline{Q}5$	Data outputs	2400/80	48mA/48mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

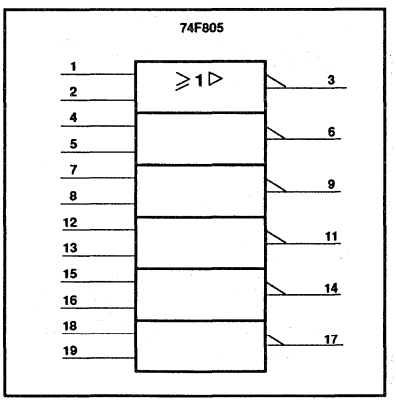
PIN CONFIGURATION



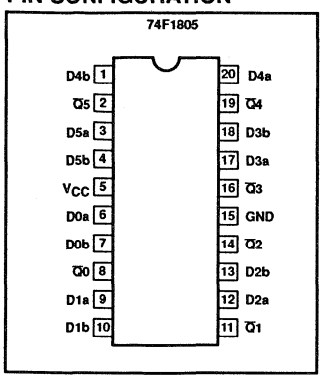
LOGIC SYMBOL



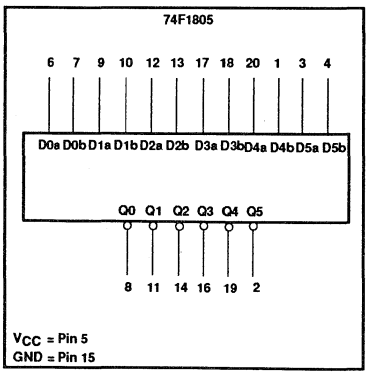
IEC/IEEE SYMBOL



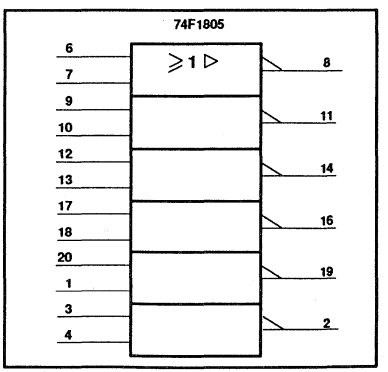
PIN CONFIGURATION



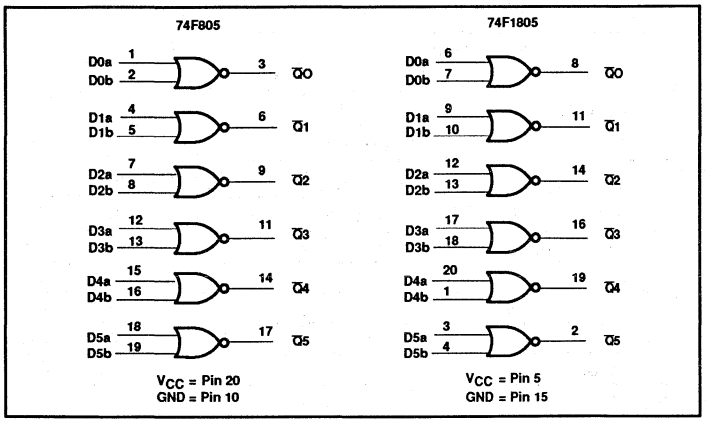
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
Dna	**Dnb**	$\overline{\text{On}}$
H	X	L
X	H	L
L	L	H

Notes to function table
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free–air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–48	mA
I_{OL}	Low–level output current			48	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		3.0	5.0	mA
		I_{CCL}		V_{IN} = 4.5V		17	25	mA

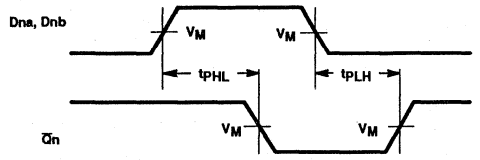
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

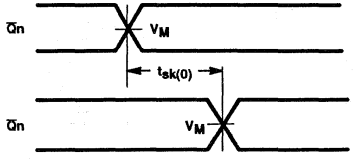
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	1.0 1.0	2.0 2.5	4.0 4.5	1.0 1.0	4.0 4.5	ns
$t_{sk(o)}$	Output skew[1,2]	Waveform 2			1.5		1.5	ns

NOTES:
1. [t_{PN} actual – t_{PM} actual] for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



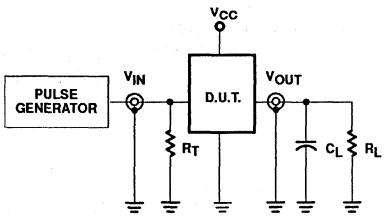
Waveform 1. Propagation delay for inverting output



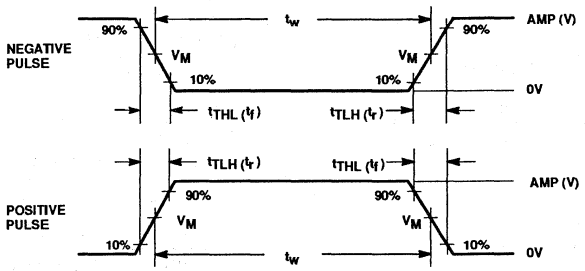
Waveform 2. Output skew

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Octal shift/count registered transceiver with adder and parity (3–State)

FAST 74F807

FEATURES

- High speed parallel registers with positive edge–triggered D–type flip–flops
- High speed full adder
- 8–bit parity generator
- High impedance PNP inputs for light bus loading
- Center V_{CC} and GND pins and controlled output buffers minimize ground–bounce problems
- 3–State glitch–free power–up and power–down
- Broadside pinout

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F807	115MHz	155mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
28–pin plastic DIP (300 mils)	N74F807N
28–pin SOL[1]	N74F807D
28–pin PLCC	N74F807A

Note to ordering information

1. Thermal mounting techiques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

DESCRIPTION

The 74F807 is a registered transceiver that also has the capability to perform count, shift, and add functions. It is also has the capability to generate a parity bit output. All of this is done within a 28–pin package.

The $\overline{MR}$ input is an overriding asynchronous reset which forces the STATOUT output low as well as the A and B busses.

The A and B busses have separate $\overline{OE}$ inputs ($\overline{OE}$A, $\overline{OE}$B]. These inputs have no bearing on the internal functioning of this device only on the output states. Both $\overline{OE}$ pins are enabled low.

All operating modes, other than clear, 3–State, and the two hold modes require the rising edge of the clock. All setup and hold times must be observed for proper functioning.

Data on the internal register can be switched on either the A or B ports for output.

Depeding on the state of the select inputs (S0, S1, S2), and carry in/ serial in/ clock enable (CI/SI/CE), the 74F807 has nine distinct operating modes:

1. Add mode w/carry in – the CI/SI/CE input is used as a carry in signal and the STATOUT output is the carry out signal. (In add mode the COUT is NOT registered. This means the carry output signal appears at the STATOUT output one clock prior to the related data.). In this mode, the CI/SI/CE input is added to the register contents and to the inputs. (The adder uses only the An inputs, not the Bn inputs.)

2. Add mode wo/carry in — same as above except the CI/SI/CE input is not included in the addition.

3. Count w/count enable (count) — the CI/SI/CE input is now used as the count enable input and the STATOUT output is terminal count. In this mode the CI/SI/CE input must be high to enable the count function. The register contents are incremented by one.

4. Count w/count enable (hold) — same as above except no incrementing occurs.

5. Count wo/count enable — same as number 3 except the CI/SI/CE input has no control over counting or holding.

6. Shift — The CI/SI/CE input now becomes the serial input and the STATOUT output becomes the serial output. In this mode the CI/SI/CE input is shifted into the Q0 register, Q0 into the Q1 register etc. The Q7 register is shifted into the STATOUT.

7. Load A inputs — The CI/SI/CE input has no bearing in either of the load modes. The STATOUT output becomes the parity out. The parity out is high for an odd number of registered bits high, and low for even number of registered bits high (even parity). In this mode the An inputs are loaded into the internal register and output to the B bus. If $\overline{OEA}$ = low the internal register would wrap around and be loaded again.

8. Load B inputs — same as number 7 except the A and B busses are switched.

9. Hold — Again the CI/SI/CE input is not used; the STATOUT output is still the parity out. In this mode either the A bus, B bus or both can be held with the registered data. No other operation is performed.

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
An, Bn	Data I/O inputs	3.5/0.166	70μA/70μA
$\overline{OEA}$, $\overline{OEB}$	A output enable inputs	1.0/0.033	20μA/20μA
CI/SI/CE	Carry in/serial in/clock enable input	1.0/0.033	20μA/20μA
CP	Clock input	1.0/0.033	20μA/20μA
$\overline{MR}$	Master reset input (active low)	1.0/0.033	20μA/20μA
Sn	Select inputs	1.0/0.033	20μA/20μA
STATOUT	Status out output	150/40	3mA/24mA
An, Bn	Data I/O outputs	150/40	3mA/24mA

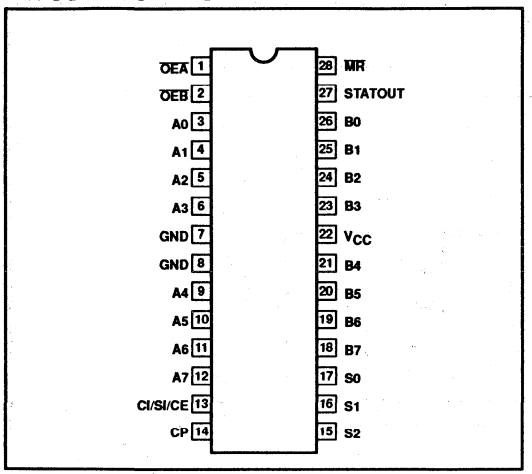
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

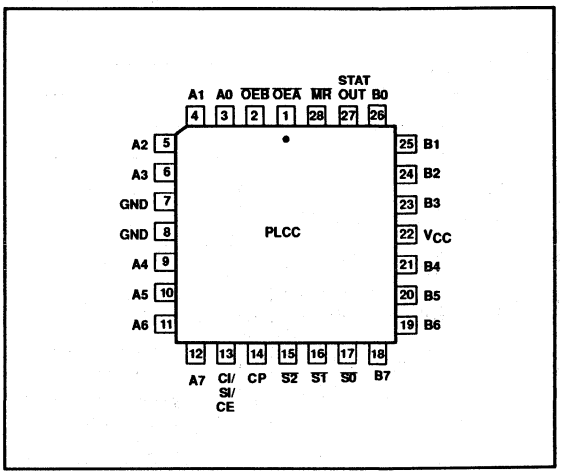
Octal shift/count registered transceiver with adder and parity (3–State)

FAST 74F807

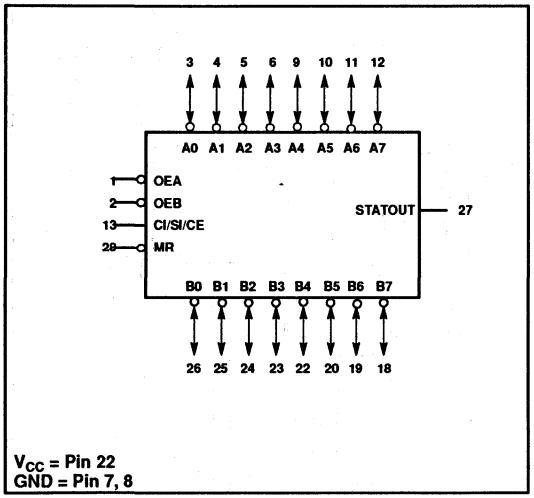
PIN CONFIGURATION



PIN CONFIGURATION PLCC

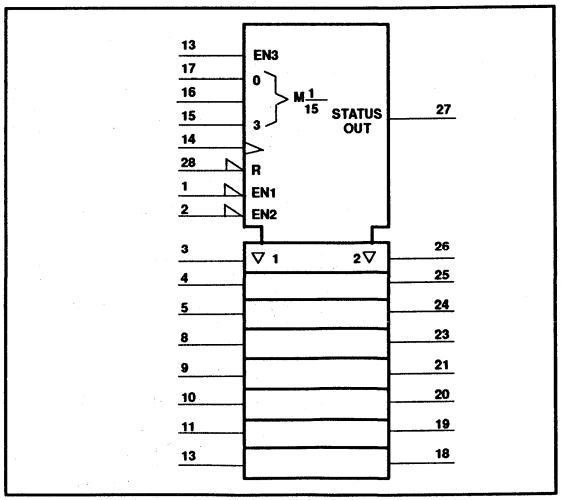


LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 7, 8

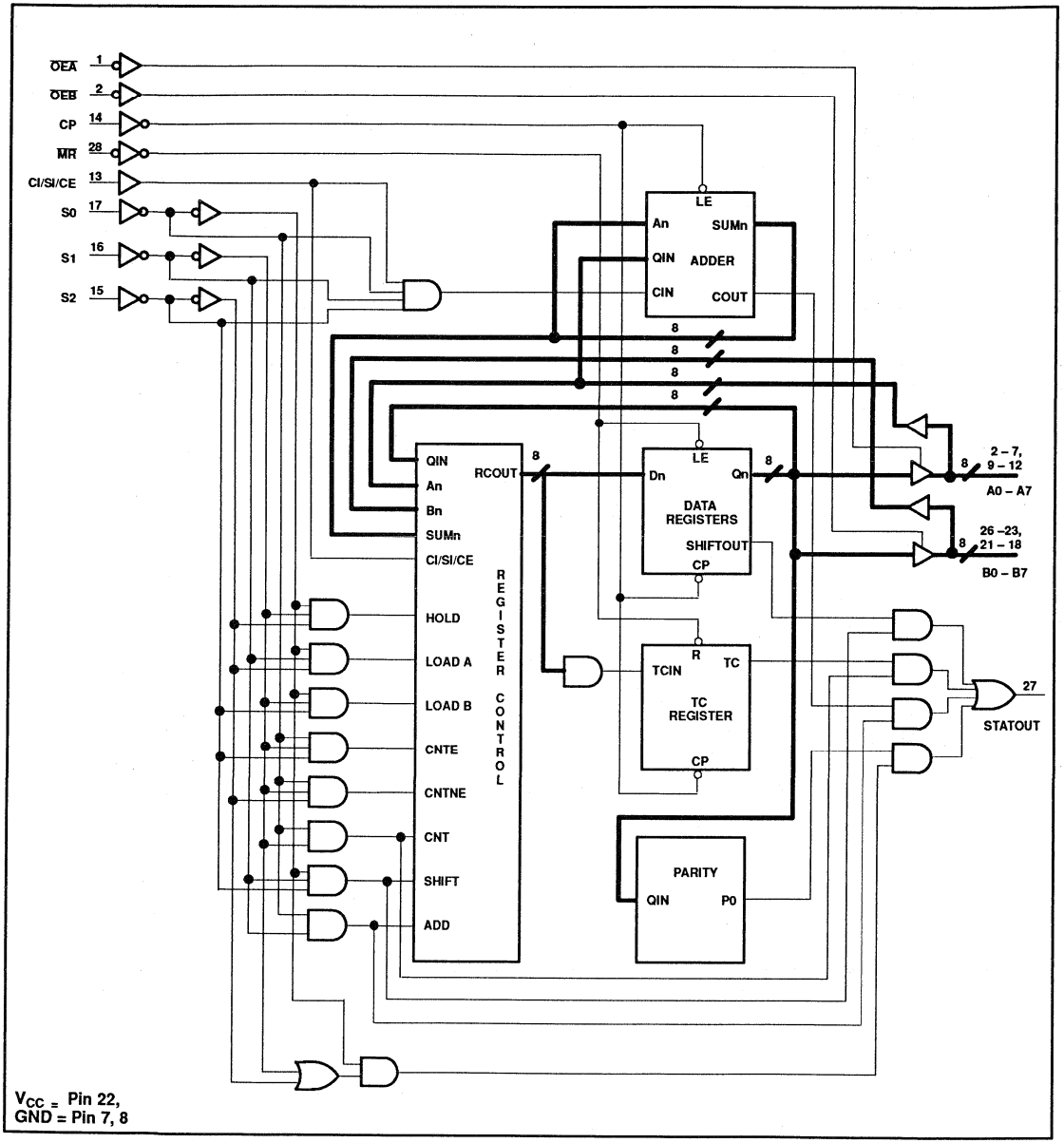
IEC/IEEE SYMBOL



Octal shift/count registered transceiver with adder and parity (3–State)

FAST 74F807

LOGIC DIAGRAM



Octal shift/count registered transceiver with adder and parity (3–State)

FAST 74F807

FUNCTION TABLE

INPUTS						INTERNAL REGISTER	OUTPUT	OPERATING MODE
$\overline{MR}$	CP	SO	S1	S2	CI/SI/CE	Qn	STATOUT	
L	X	X	X	X	X	L	L	Clear
H	↑	L	L	L	CI/SI/CE	CI/SI/CE + an0 + qn0	COUT	Add mode w/carry in
H	↑	L	L	H	X	an0 + qn0	COUT	Add mode wo/carry in
H	↑	L	H	L	H	qn0 + 1	TC (1)	Count w/count enable (count)
H	X	L	H	H	L	qn0	TC (1)	Count w/count enable (hold)
H	↑	L	H	H	X	qn0 + 1	TC (1)	Count wo/count enable
H	↑	H	L	L	CI/SI/CE	(3)	Q7	Shift
H	↑	H	L	H	X	An0	parity (2)	Load A ports
H	↑	H	H	L	X	Bn0	parity (2)	Load B ports
H	X	H	H	H	X	Qn0	parity (2)	Hold

Notes to function table

1. H = High–voltage level
2. L = Low–voltage level
3. a, b, q = Lower case indicate the state of the referenced output prior to the low–to–high clock transition
4. X = Don't care
5. Z = High impedance "off)" state
6. ↑ = Low–to–high clock transition.
7. (1) = Terminal count is high when the output is a terminal count (HHHHHHHH).
8. (2) = Parity is high for odd number of internal register bits high, low for even number of internal register bits high.
9. (3) = CI/SI/CE → Q0 → Q1, etc.

$\overline{OE}$ FUNCTION TABLE

INPUTS		OUTPUTS		MODE
$\overline{OE}$a	$\overline{OE}$b	An	Bn	
L	L	active output	active output	Enable A and B outputs
L	H	active output	input	Enable A outputs, B inputs
H	L	input	active output	A inputs, enable B outputs
H	H	input	input	A and B are inputs

NOTE: The outputs, whether An or Bn, are equal to the INTERNAL REGISTER Qn.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free–air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	48	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
Tstg	Storage temperature range	–65 to +150	°C

NOTE: When outputs are disabled the internal registers (Qn) operate as usual.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–3	mA
I_{OL}	Low–level output current			24	mA
T_{amb}	Operating free air temperature	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OZH} + I_{IH}	Off–state output current, high–level voltage applied	An, Bn	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied	An, Bn	V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			155	210	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

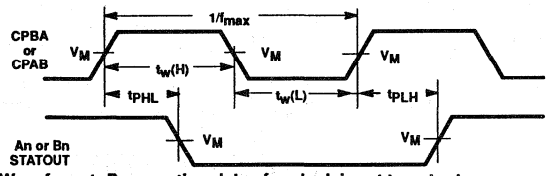
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50p, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	115		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to An or Bn (load)	Waveform 1	9.0 5.0	10.5 6.5	11.5 9.5	8.0 4.5	13.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to An or Bn (shift)	Waveform 1	9.0 4.5	10.5 6.5	12.5 9.5	8.0 4.5	15.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to An or Bn (count)	Waveform 1	9.0 5.0	11.5 6.5	14.0 9.5	8.0 4.5	15.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Bn (add)	Waveform 1	9.0 5.0	10.5 6.5	11.5 9.5	8.0 4.5	13.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to STATOUT (load A)	Waveform 1	17.5 12.5	19.5 14.5	22.5 17.0	15.5 11.5	26.5 19.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to STATOUT (shift)	Waveform 1	11.0 7.0	13.0 8.5	15.5 11.5	9.5 6.5	18.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to STATOUT (count)	Waveform 1	10.5 6.5	12.0 8.0	15.0 11.0	9.0 6.0	17.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to STATOUT (add)	Waveform 1	13.0 8.5	15.0 10.5	18.0 13.0	11.5 8.0	20.5 14.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to An or Bn (load A)	Waveform 3	6.5	8.0	11.0	6.0	12.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to STATOUT (load A)	Waveform 3	14.0	16.0	18.5	13.0	20.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to STATOUT (shift)	Waveform 3	8.5	10.0	12.5	8.0	14.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to STATOUT (count)	Waveform 3	8.5	10.0	12.5	8.0	14.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to STATOUT (add)	Waveform 3	10.5	12.0	14.5	9.5	16.0	ns
t_{PLH} t_{PHL}	Propagation delay An to STATOUT (add)	Waveform 4	6.5 8.0	14.0 14.0	23.5 22.5	5.5 7.5	26.5 27.0	ns
t_{PLH} t_{PHL}	Propagation delay CI/SI/CE to STATOUT	Waveform 4	19.5 21.0	21.5 22.5	24.0 25.5	17.0 20.0	28.0 29.5	ns
t_{PLH} t_{PHL}	Propagation delay Sn to STATOUT (load A)	Waveform 4	8.0 7.5	10.0 11.5	12.5 15.5	7.0 7.0	14.5 17.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to STATOUT (load B)	Waveform 4	6.5 8.0	10.0 12.0	13.0 15.0	5.5 7.0	15.0 16.5	ns
t_{PLH} t_{PHL}	Propagation delay Sn to STATOUT (add)	Waveform 4	19.0 18.5	21.0 20.0	23.5 23.0	17.0 17.5	27.5 26.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to STATOUT (shift)	Waveform 4	6.0 8.0	8.0 9.5	10.5 12.0	5.0 7.0	12.0 13.5	ns
t_{PZH} t_{PZL}	Output enable time, $\overline{OEA}$ to An or $\overline{OEB}$ to Bn	Waveform 6 Waveform 7	2.5 4.0	4.5 5.5	7.0 8.5	2.0 3.5	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time, $\overline{OEA}$ to An or $\overline{OEB}$ to Bn	Waveform 6 Waveform 7	2.0 3.5	4.5 5.5	7.5 8.5	2.0 3.0	9.0 9.5	ns

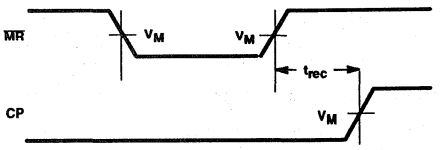
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An, Bn to CP (load)	Waveform 5	6.0 9.5			6.5 12.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An, Bn to CP (load)	Waveform 5	0.0 0.0			0.0 0.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An, Bn to CP (add)	Waveform 5	10.5 16.5			12.0 21.5		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An, Bn to CP (add)	Waveform 5	0.0 0.0			0.0 0.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Sn to CP (add)	Waveform 5	16.0 16.0			20.0 28.5		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Sn to CP (count)	Waveform 5	16.5 19.5			19.0 22.5		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Sn to CP (shift)	Waveform 5	11.0 7.0			13.0 8.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Sn to CP (load)	Waveform 5	17.5 6.5			20.5 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Sn to CP (all modes)	Waveform 5	0.0 0.0			0.0 0.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low CI/SI/CE to CP (add)	Waveform 5	10.0 18.0			11.5 22.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low CI/SI/CE to CP (count)	Waveform 5	8.5 16.0			10.0 18.5		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low CI/SI/CE to CP (shift)	Waveform 5	5.0 9.0			5.5 10.5		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low CI/SI/CE to CP (all modes)	Waveform 5	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or low	Waveform 1	5.5 4.5			6.0 4.5		ns
$t_w(L)$	$\overline{MR}$ pulse width, low	Waveform 3	4.5			5.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	2.0			2.0		ns

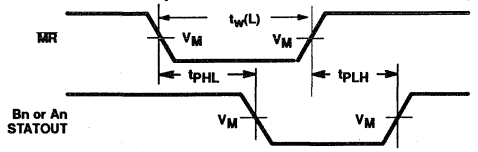
AC WAVEFORMS



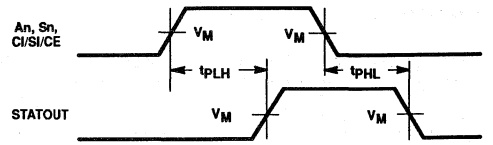
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



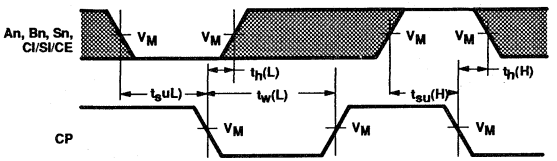
Waveform 2. Master reset to clock recovery time



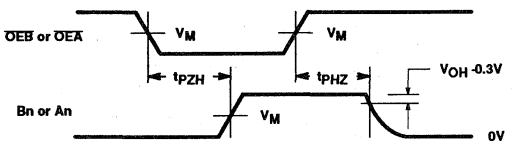
Waveform 3. Propagation delay for master reset to data or master reset to STATOUT



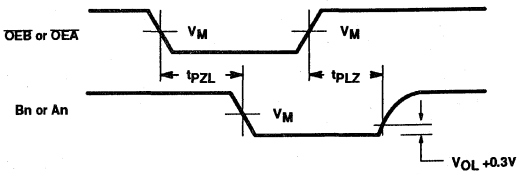
Waveform 4. Propagation delay for select to STATOUT, CI/SI/CE to STATOUT or data to STATOUT



Waveform 5. Data setup and hold times



Waveform 6. 3–State output enable time to high level and output disable time from high level



Waveform 7. 3-state output enable time to low level and output disable time from low level

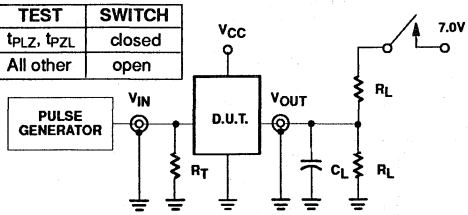
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



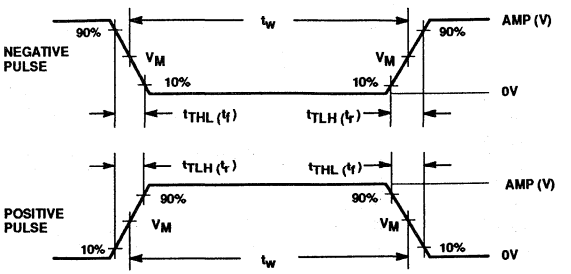
Test circuit for 3–State outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Hex 2-input AND drivers — 74F808/74F1808

FEATURES

- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND – 74F808
  Center V_{CC} and GND – 74F1808
- Typical propagation delay of 4.0ns
- Superior ground noise characteristics (implemented using ouput edge rate control)
- Increased source and sink current (64mA)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F808	4.0ns	24mA
74F1808	4.0ns	24mA

ORDERING INFORMATION

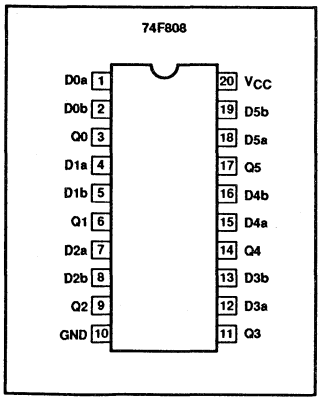
DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20–pin plastic DIP	N74F808N, N74F1808N
20–pin plastic SOL	N74F808D, N74F1808D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

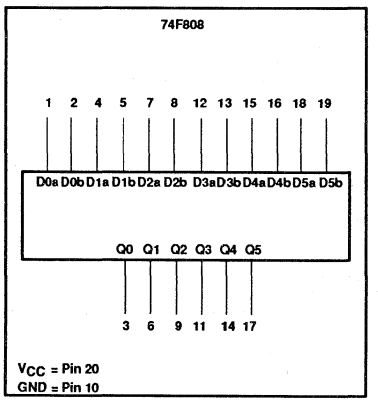
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna – Dnb	Data inputs	1.0/0.033	20µA/20µA
Q0 – Q5	Data outputs	3200/106.7	64mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

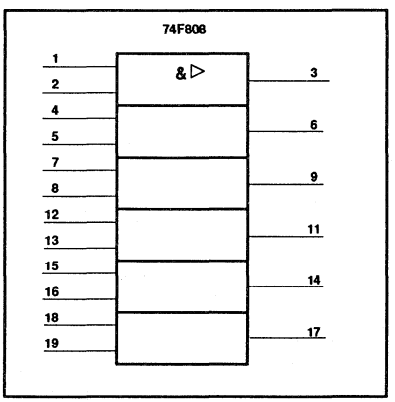
PIN CONFIGURATION



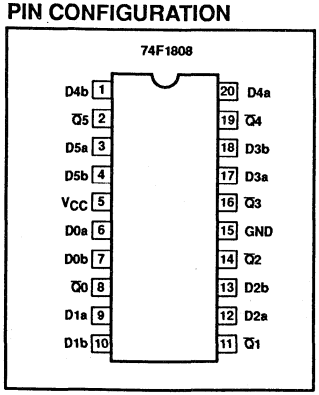
LOGIC SYMBOL



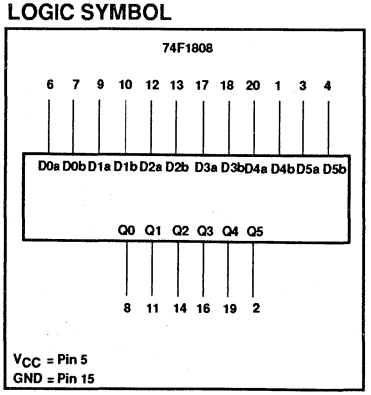
IEC/IEEE SYMBOL



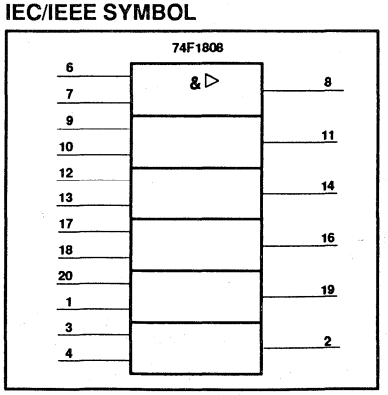
PIN CONFIGURATION



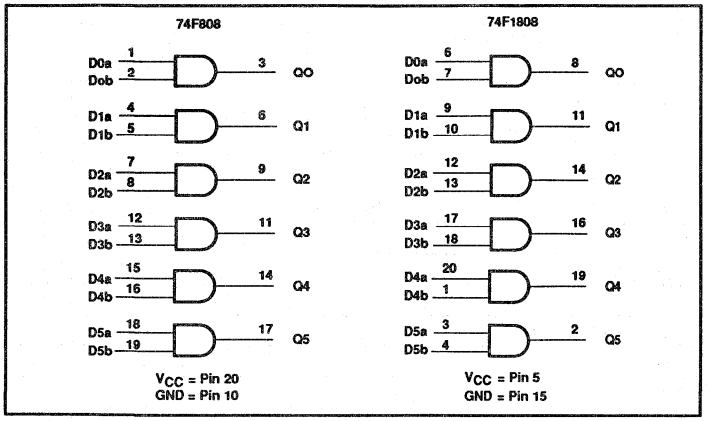
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
Da	Db	Q
H	H	H
L	X	L
X	L	L

NOTES:
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free–air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–64	mA
I_{OL}	Low–level output current			64	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX		-60		-180	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		19	27	mA
		I_{CCL}		V_{IN} = 4.5V		30	42	mA

NOTES:

3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
4. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
5. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.

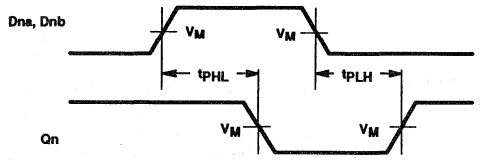
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	Waveform 1	2.0 2.0	4.5 3.5	6.3 6.0	2.0 1.5	6.8 6.5	ns
$t_{sk(o)}$	Output skew[1,2]	Waveform 2			2.5		3.0	ns

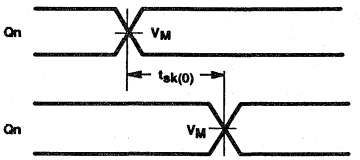
NOTES:

1. [t_{PN} actual – t_{PM} actual] for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



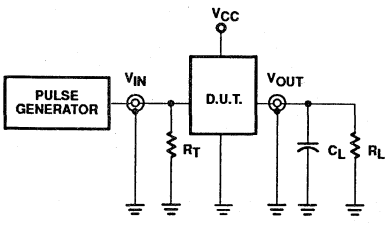
Waveform 1. Propagation delay for inverting outputs



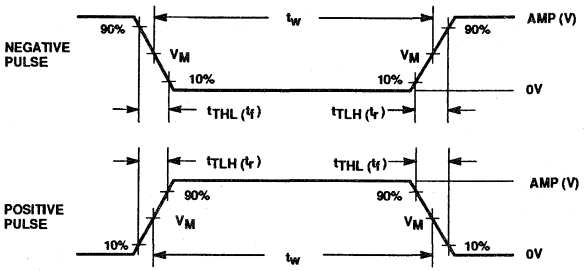
Waveform 2. Output skew

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	v_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Bus interface

74F821/822/823/ 824/825/826

74F821/74F822 10–bit bus interface registers, NINV/INV (3–state), 74F823/74F824 9–bit bus interface registers, NINV/INV (3–state), 74F825/74F826 8–bit bus interface registers, NINV/INV (3–state)

FEATURE

- High speed parallel registers with positive edge–triggered D–type flip–flops
- High performance bus interface buffering for wide data/address paths or busses carrying parity
- High impedance PNP base inputs for reduced loading (20μA in high and low states)
- I_{IL} is 20μA vs 1000μA for AM29821 series
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan–in as required with MOS microprocessor
- Positive and negative over–shoots are clamped to ground
- 3–state outputs glitch free during power–up and power–down
- Slim Dip 300 mil package
- Broadside pinout compatible with AMD AM 29821–29826 series
- Outputs sink 64mA and source 24mA
- Industrial temperature range available (–40°C to +85°C) for 74F823

DESCRIPTION

The 74F821 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of busses carrying parity.

The 74F821/74F822 are buffered 10–bit wide versions of the popular 74F374/74F534 functions.

The 74F822 is the inverted output version of 74F821.

The 74F823 and 74F824 are 9–bit wide buffered registers with clock enable ($\overline{CE}$) and master reset ($\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The 74F824 is the inverted version of 74F823.

The 74F825 and 74F826 are 8–bit buffered registers with all the 74F823/74F824 controls plus output enable ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for uses as an output port requiring high I_{OL}/I_{OH}.

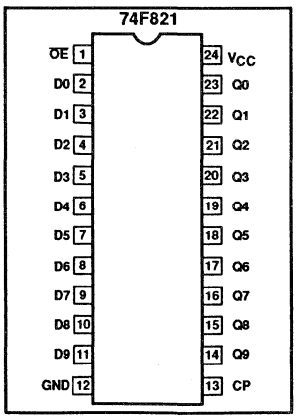
The 74F826 is the inverted version of 74F825.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F821, 74F822	180MHz	75mA
74F823, 74F824	180MHz	70mA
74F825, 74F826	180MHz	65mA

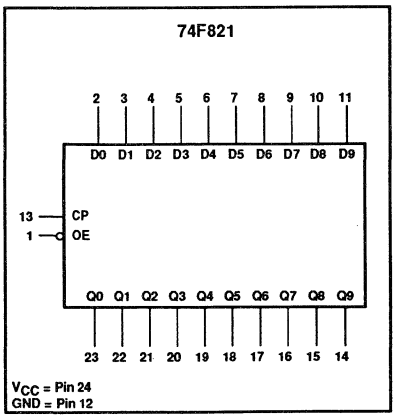
ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
24–pin plastic slim DIP (300mil)	N74F821N, N74F822N, N74F823N, N74F824N, N74F825N, N74F826N	I74F823N
24–pin plastic SOL	N74F821D, N74F822D, N74F823D, N74F824D, N74F825D, N74F826D	I74F823D

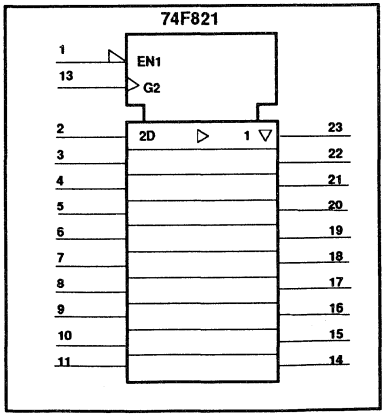
PIN CONFIGURATION



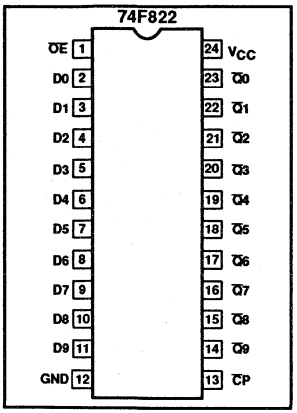
LOGIC SYMBOL



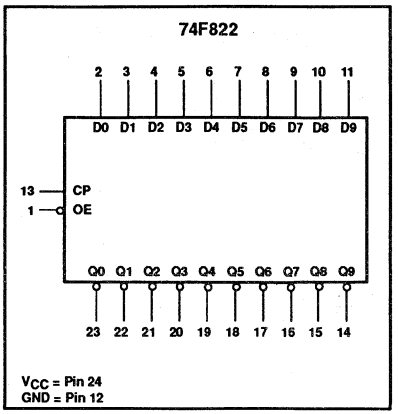
IEC/IEEE SYMBOL



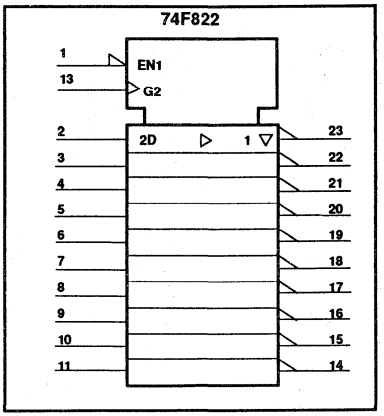
PIN CONFIGURATION



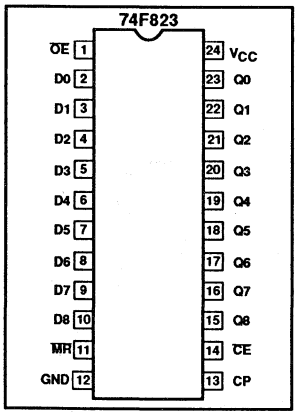
LOGIC SYMBOL



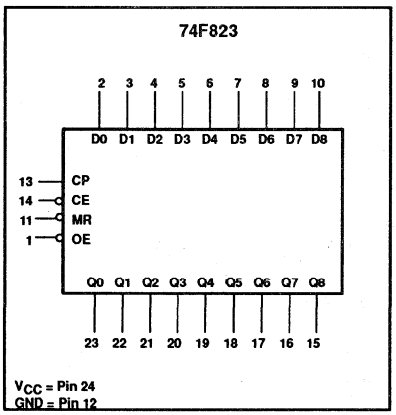
IEC/IEEE SYMBOL



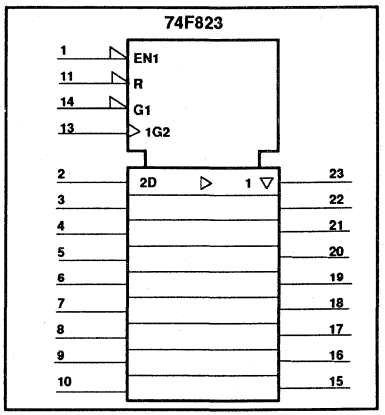
PIN CONFIGURATION



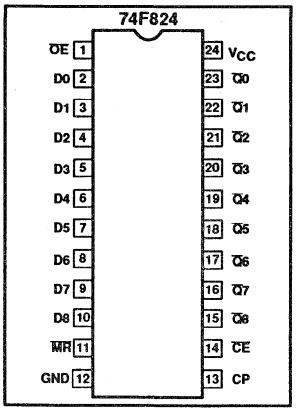
LOGIC SYMBOL



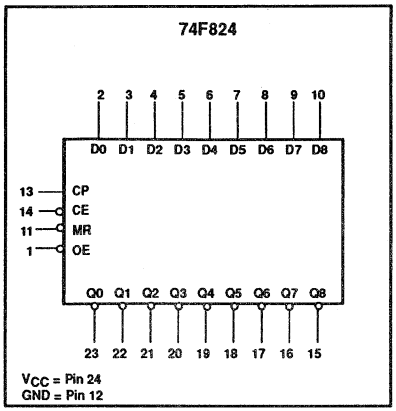
IEC/IEEE SYMBOL



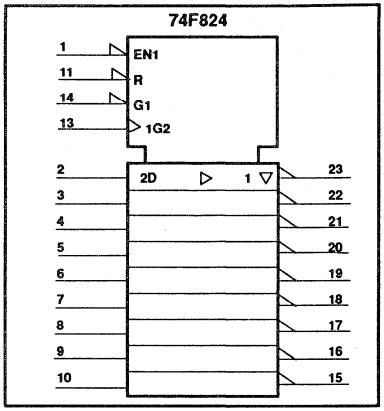
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



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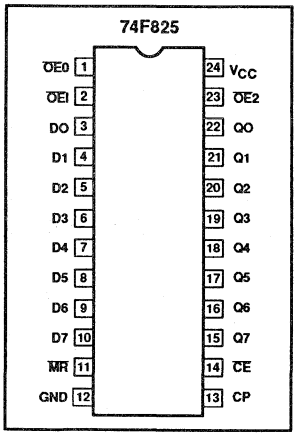
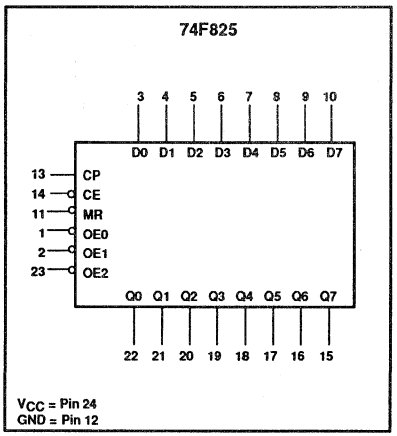
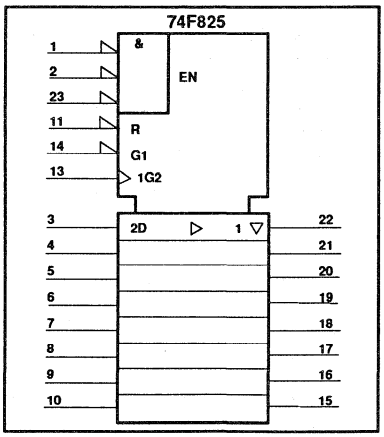


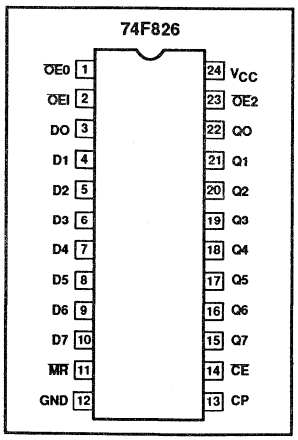
LOGIC SYMBOL



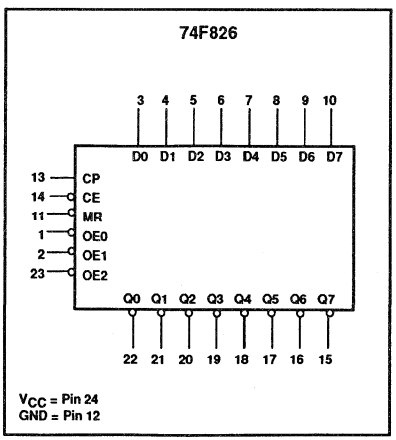
IEC/IEEE SYMBOL



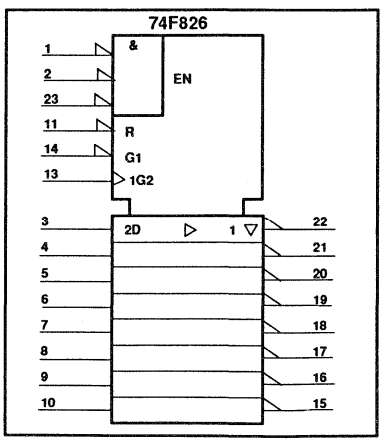
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL

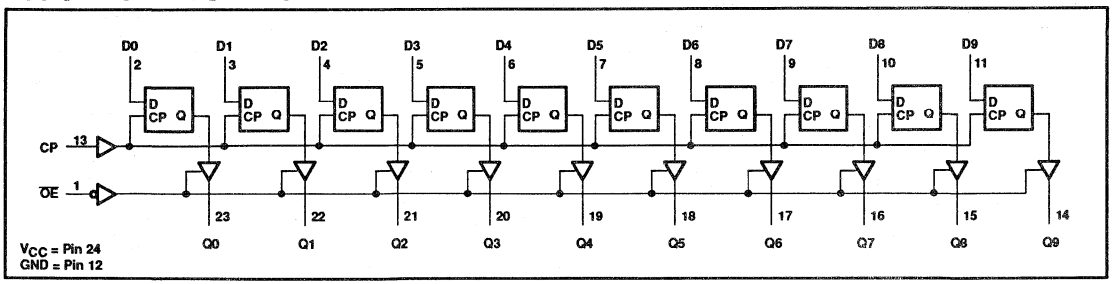


INPUT AND OUTPUT LOADING AND FAN OUT TABLE

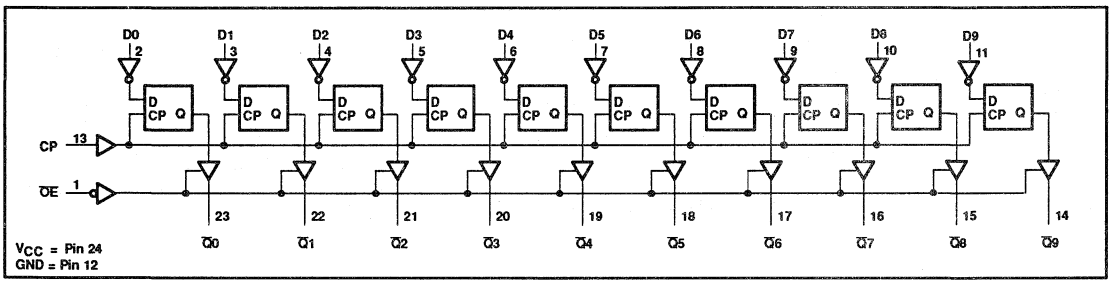
PINS		DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F821 'F822	Dn	Data inputs	1.0/1.0	20μA/0.6mA
	CP	Clock input	1.0/1.0	20μA/0.6mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20μA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA
'F823 'F824	Dn	Data inputs	1.0/1.0	20μA/0.6mA
	CP	Clock input	1.0/1.0	20μA/0.6mA
	$\overline{CE}$	Clock enable input (active low)	1.0/3.0	20μA/1.8mA
	$\overline{MR}$	Master reset input (active low)	1.0/3.0	20μA/1.8mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20μA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA
'F825 'F826	Dn	Data inputs	1.0/1.0	20μA/0.6mA
	CP	Clock input	1.0/1.0	20μA/0.6mA
	$\overline{CE}$	Clock enable input (active low)	1.0/3.0	20μA/1.8mA
	$\overline{MR}$	Master reset input (active low)	1.0/3.0	20μA/1.8mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20μA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM FOR 74F821



LOGIC DIAGRAM FOR 74F822

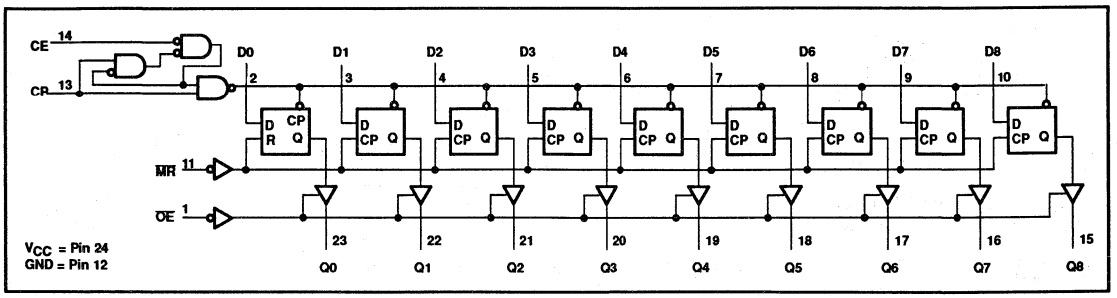


FUNCTION TABLE FOR 74F821 AND 74F822

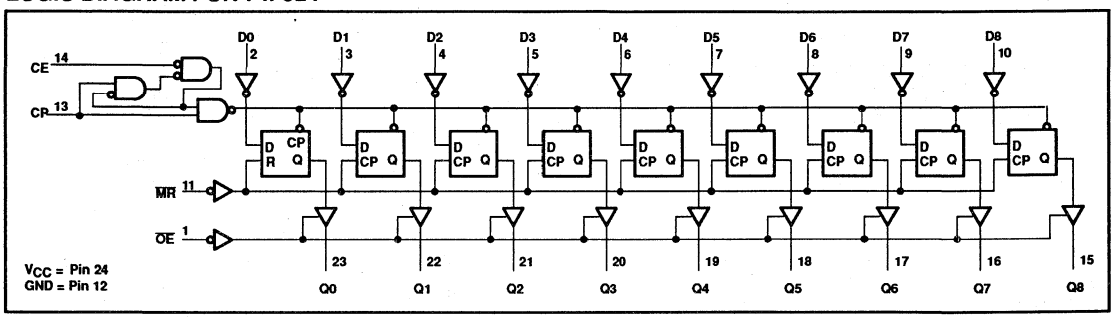
INPUTS			OUTPUTS		OPERATING MODE
			74F821	74F822	
$\overline{OE}$	CP	Dn	Q	$\overline{Q}$	
L	↑	l	L	H	Load and read data
L	↑	h	H	L	
L	↥	X	NC	NC	Hold
H	X	X	Z	Z	High impedance

NOTES:
1. H = High–voltage level
2. h = High state must be present one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low state must be present one setup time before the low–to–high clock transition
5. NC= No change
6. X = Don't care
7. Z = High impedance "off" state
8. ↑ = Low–to–high clock transition
9. ↥ = Not low–to–high clock transition

LOGIC DIAGRAM FOR 74F823



LOGIC DIAGRAM FOR 74F824

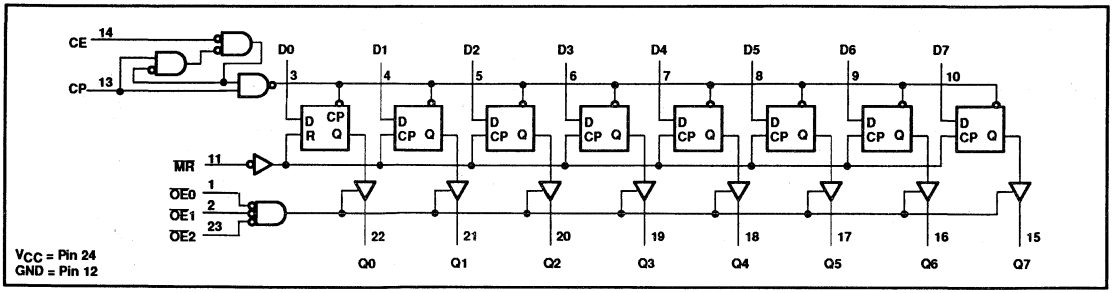


FUNCTION TABLE for 74F823 and 74F824

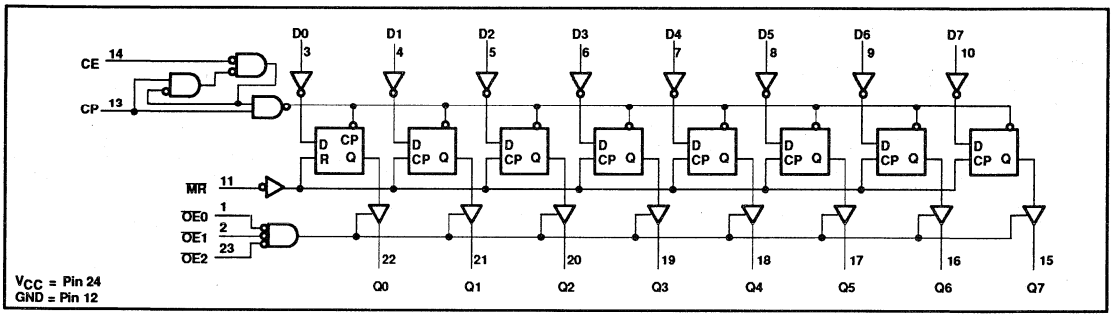
INPUTS					OUTPUTS		OPERATING MODE
					74F823	74F824	
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$*	CP	Dn	Q	$\overline{Q}$	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	X	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

NOTES:
1. H = High–voltage level
2. h = High state must be present one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low state must be present one setup time before the low–to–high clock transition
5. NC= No change
6. X = Don't care
7. Z = High impedance "off" state
8. * = Since $\overline{CE}$ input is sensitive to very short (<3ns) high–to–low–to–high going spikes while CP is high, users should avoid the use of decoders or other potentially glitch prone device on the $\overline{CE}$ input.
9. ↑ = Low–to–high clock transition

LOGIC DIAGRAM FOR 74F825



LOGIC DIAGRAM FOR 74F826



FUNCTION TABLE for 74F825 and 74F826

INPUTS					OUTPUTS		OPERATING MODE
					74F825	74F826	
$\overline{OE}n$	$\overline{MR}$	$\overline{CE}$*	CP	Dn	Q	$\overline{Q}$	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	X	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

NOTES:

1. H = High–voltage level
2. h = High state must be present one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low state must be present one setup time before the low–to–high clock transition
5. NC = No change
6. X = Don't care
7. Z = High impedance "off" state
8. * = Since $\overline{CE}$ input is sensitive to very short (<3ns) high–to–low–to–high going spikes while CP is high, users should avoid the use of decoders or other potentially glitch prone device on the $\overline{CE}$ input.
9. ↑ = Low–to–high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		128	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current				–24	mA
I_{OL}	Low–level output current				64	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} =	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.4			V
					I_{OH} = –24mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High–level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current			V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}	Off–state output current, high–level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied			V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short–circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F821, 74F822	I_{CCH}	V_{CC} = MAX				75	105	mA
			I_{CCL}					75	105	mA
			I_{CCZ}					75	115	mA
		74F823, 74F824	I_{CCH}	V_{CC} = MAX				65	100	mA
			I_{CCL}					70	105	mA
			I_{CCZ}					75	110	mA
		74F825, 74F826	I_{CCH}	V_{CC} = MAX				60	85	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F821/74F822/74F824/74F825/74F826

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency		Waveform 1	150	180		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Q}$n	74F821, 74F825, 74F826	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}$n	74F822, 74F824	Waveform 1	4.5 4.5	6.5 6.5	9.0 9.0	4.5 4.5	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn or $\overline{Q}$n	74F824 74F825, 74F826	Waveform 2	3.0	5.0	8.0	3.0	8.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$n to Qn or $\overline{Q}$n		Waveform 4 Waveform 5	2.0 3.0	4.5 5.0	8.0 8.0	2.0 2.5	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$n to Qn or $\overline{Q}$n		Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS FOR 74F821/74F822/74F824/74F825/74F826

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L= 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to CP		Waveform 3	1.0 1.0			1.0 1.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
t_w (H) t_w (L)	CP Pulse width, high or low		Waveform 1	3.5 3.5			4.0 4.0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low, $\overline{CE}$ to CP	74F824, 74F825, 74F826	Waveform 3	0.0 2.0			0.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{CE}$ to CP		Waveform 3	0.0 3.0			0.0 3.5		ns
t_w (L)	$\overline{MR}$ Pulse width, low		Waveform 2	4.5			4.5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP		Waveform 2	2.5			2.5		ns

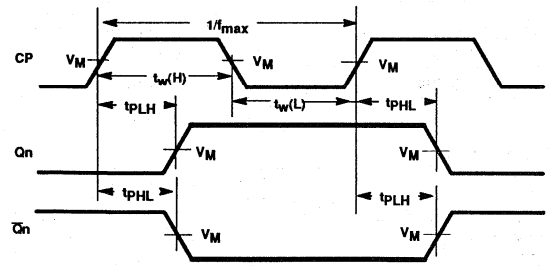
AC ELECTRICAL CHARACTERISTICS FOR 74F823

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to 85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	150	180		140		130		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Qn}$	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	4.0 3.5	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn or $\overline{Qn}$	Waveform 2	3.0	5.0	8.0	3.0	8.0	3.0	8.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$n to Qn or $\overline{Qn}$	Waveform 4 Waveform 5	2.0 3.0	4.5 5.0	8.0 8.0	2.0 2.5	9.0 9.0	2.0 2.5	11.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$n to Qn or $\overline{Qn}$	Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns

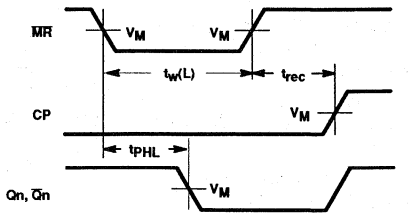
AC SETUP REQUIREMENTS FOR 74F823

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L= 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L= 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to CP	Waveform 3	1.0 1.0			1.0 1.0		2.0 1.5		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CP	Waveform 3	2.0 2.0			2.0 2.0		2.5 2.0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	Waveform 1	3.5 3.5			4.0 4.0		4.0 4.0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low, $\overline{CE}$ to CP	Waveform 3	0.0 2.0			0.0 2.0		0.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{CE}$ to CP	Waveform 3	0.0 3.0			0.0 3.5		1.5 4.0		ns
t_w (L)	$\overline{MR}$ Pulse width, low	Waveform 2	4.5			4.5		4.5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	2.5			2.5		2.5		ns

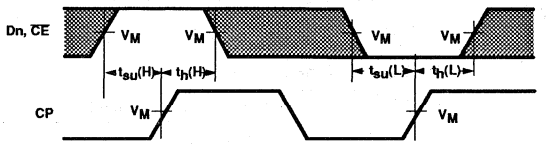
AC WAVEFORMS



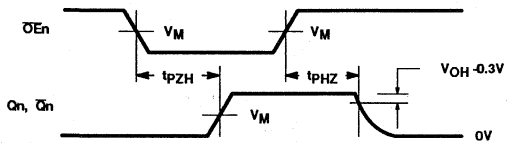
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



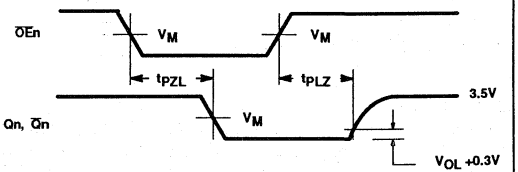
Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time



Waveform 3. Data setup time and hold times



Waveform 4. 3-state output enable time to high level and output disable time from high level



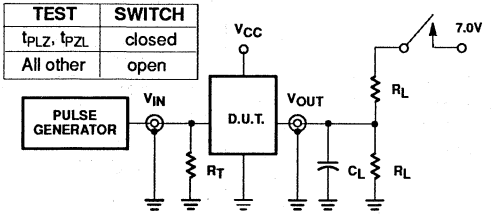
Waveform 5. 3-state output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



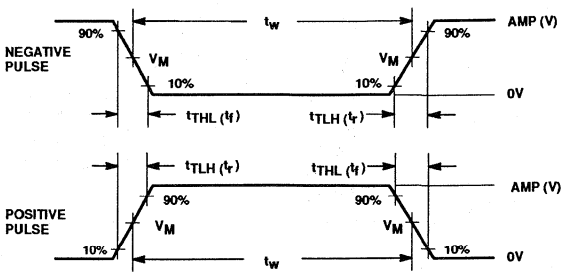
Test circuit for 3–state outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0880
ECN No.	97929
Date of issue	October 23, 1989
Status	Product Specification
FAST Products	

FAST 74F827, 74F828 Buffers

74F827 10-Bit Buffer/Line Driver, Non-Inverting (3-State)
74F828 10-Bit Buffer/Line Driver, Inverting (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F827	6.0ns	60mA
74F828	6.0ns	55mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **I_{IL} is 20μA vs FAST family spec of 600μA and 1000μA for AMD 29827/29828 series**
- **Ideal where high speed, light bus loading and increased fan-in are required**
- **Controlled rise and fall times to minimize ground bounce**
- **Glitch free power up in 3-state**
- **Flow through pinout architecture for microprocessor oriented applications**
- **Outputs sink 64mA**
- **Slim 300 mil-wide plastic 24-pin package**
- **Pinout and function compatible with AMD 29827/29828 series**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic DIP (300 mil)	N74F827N, N74F828N
24-Pin Plastic SOL	N74F827D, N74F828D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_9	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$ $\overline{OE}_1$	Output enable inputs (active Low)	1.0/0.033	20μA/20μA
Q_0- Q_9	Data outputs ('F827)	1200/106.7	24mA/64mA
$\overline{Q}_0$- $\overline{Q}_9$	Data outputs ('F828)	1200/106.7	24mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

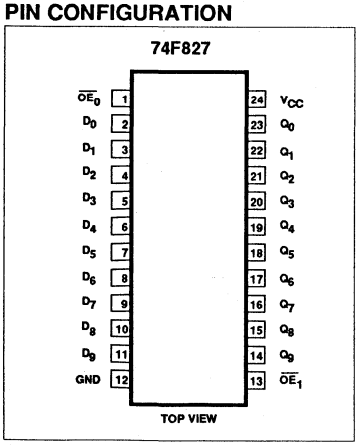
DESCRIPTION

The 74F827 and 74F828 10-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

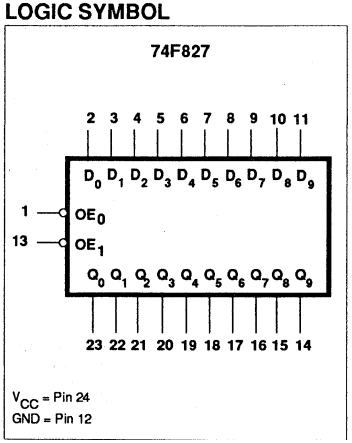
The 'F827 and 'F828 are functionally and pin compatible to AMD AM29827 and AM 29828.

The 'F828 is an inverting version of 'F827.

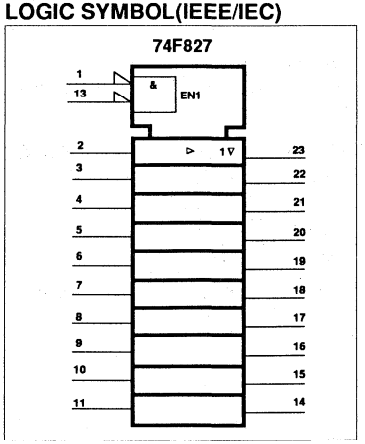
PIN CONFIGURATION



LOGIC SYMBOL

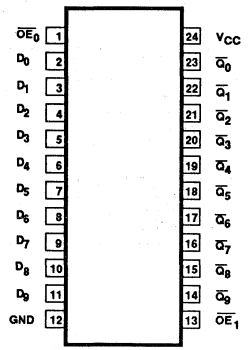


LOGIC SYMBOL(IEEE/IEC)



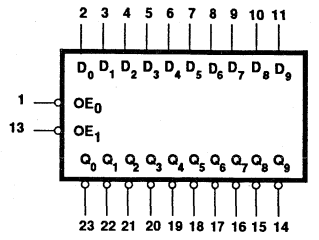
PIN CONFIGURATION

74F828



LOGIC SYMBOL

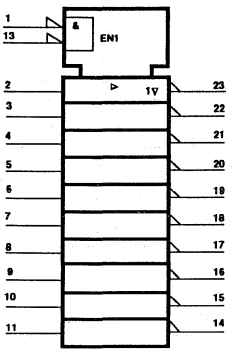
74F828



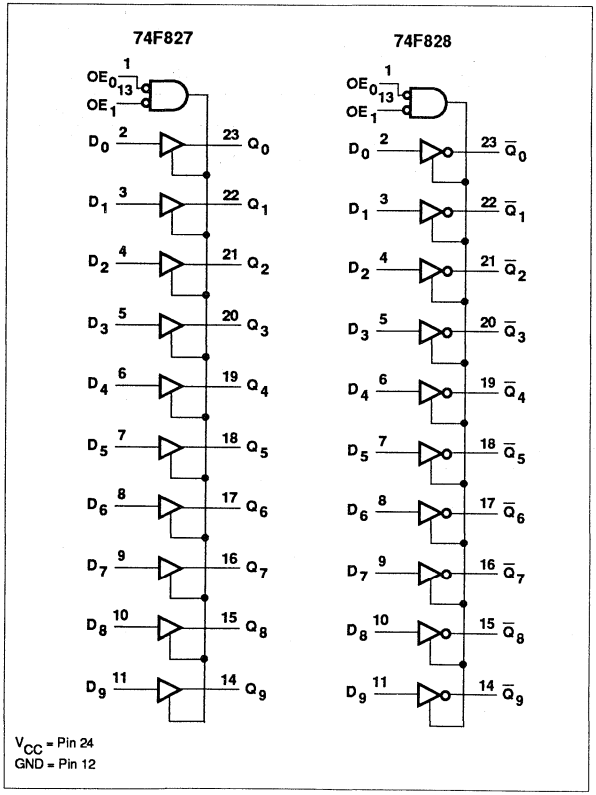
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

74F828



LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
		'F827	'F828	
$\overline{OE}_n$	D_n	Q_n	$\overline{Q}_n$	
L	L	L	H	Transparent
L	H	H	L	Transparent
H	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.4	3.3		V
					I_{OH} = -24mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, HIgh voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F827	I_{CCH}	V_{CC} = MAX				50	70	mA
			I_{CCL}					70	100	mA
			I_{CCZ}					60	90	mA
		'F828	I_{CCH}	V_{CC} = MAX				30	45	mA
			I_{CCL}					65	85	mA
			I_{CCZ}					55	70	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1	2.0 2.0	5.5 4.5	8.5 8.5	2.0 2.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4	5.0 4.0	8.0 6.0	12.0 10.5	4.5 4.0	14.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4	2.5 2.5	5.0 5.0	8.0 8.0	2.0 2.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2	2.0 1.0	6.0 3.0	8.5 7.0	2.0 1.0	9.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4	6.0 5.0	8.0 7.0	11.5 10.5	5.5 4.5	14.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4	2.5 1.5	5.0 4.0	8.5 7.0	2.0 1.5	9.0 8.0	ns

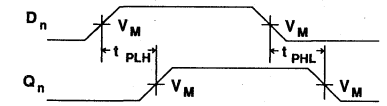
AC ELECTRICAL CHARACTERISTICS for 1 Output switching with C_L=300pF and R_L =500Ω load

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L =300pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1		9.5 7.5	13.0 10.0		14.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 9.5	20.0 13.0		21.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 9.5	19.0 13.5		20.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2		10.0 6.0	13.0 9.0		14.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		15.5 10.5	19.0 13.0		21.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		15.0 10.0	18.0 13.0		20.0 14.5	ns

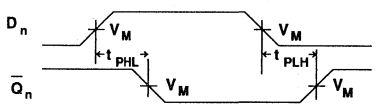
AC ELECTRICAL CHARACTERISTICS for 10 Outputs switching with C_L=300pF and R_L =500Ω load

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L =300pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1		12.0 14.0	16.0 17.0		17.0 18.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 17.0	20.0 21.0		21.0 21.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 12.5	19.0 15.5		20.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2		10.0 10.0	17.0 13.5		18.0 14.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		18.0 15.0	21.0 18.0		23.0 19.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		16.5 11.5	19.5 14.5		22.5 15.0	ns

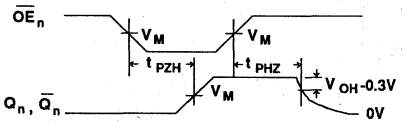
AC WAVEFORMS



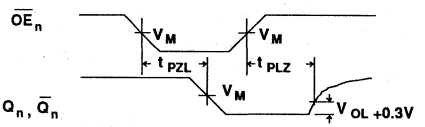
Waveform 1. Propagation Delay For Non-Inverting Output



Waveform 2. Propagation Delay For Inverting Output



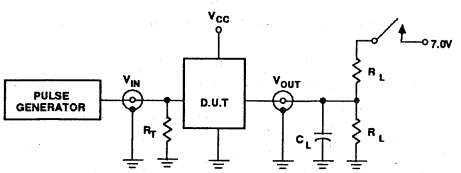
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

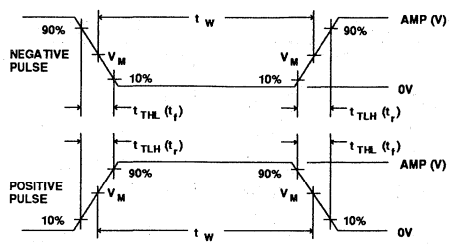
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Hex 2-input OR drivers

74F832/74F1832

FEATURES

- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND – 74F832
  Center V_{CC} and GND – 74F1832
- Typical propagation delay of 3.5ns
- Superior ground noise characteristics (implemented using ouput edge rate control)
- Increased source and sink current (64mA)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F832	3.5ns	26mA
74F1832	3.5ns	26mA

ORDERING INFORMATION

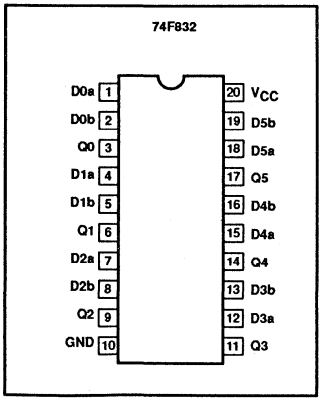
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20–pin plastic DIP	N74F832N, N74F1832N
20–pin plastic SOL	N74F832D, N74F1832D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

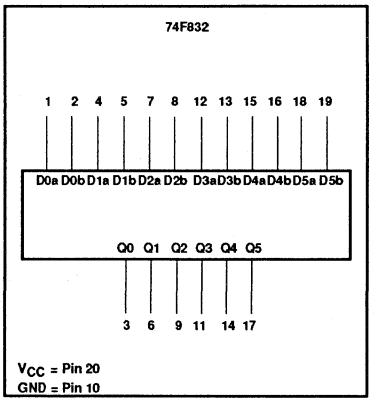
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna – Dnb	Data inputs	1.0/0.033	20µA/20µA
Q0 – Q5	Data outputs	3200/106.7	64mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

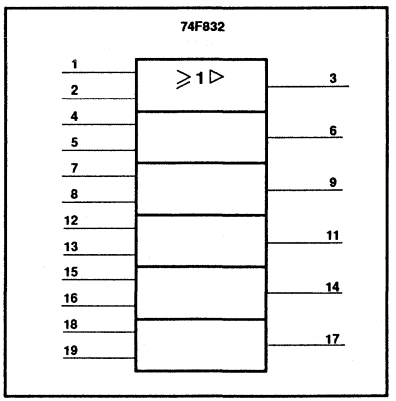
PIN CONFIGURATION



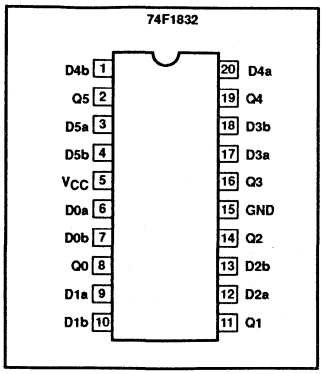
LOGIC SYMBOL



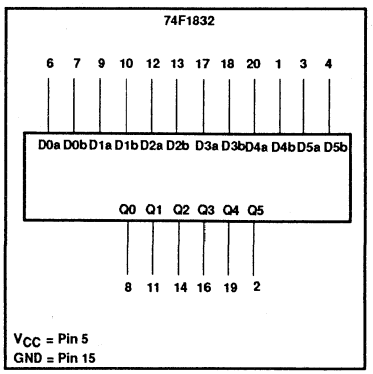
IEC/IEEE SYMBOL



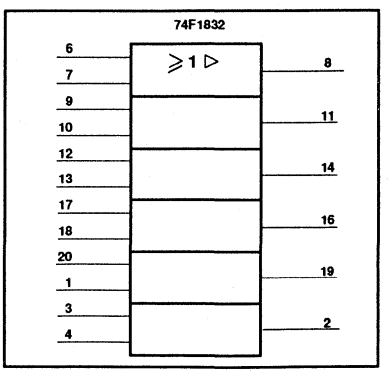
PIN CONFIGURATION



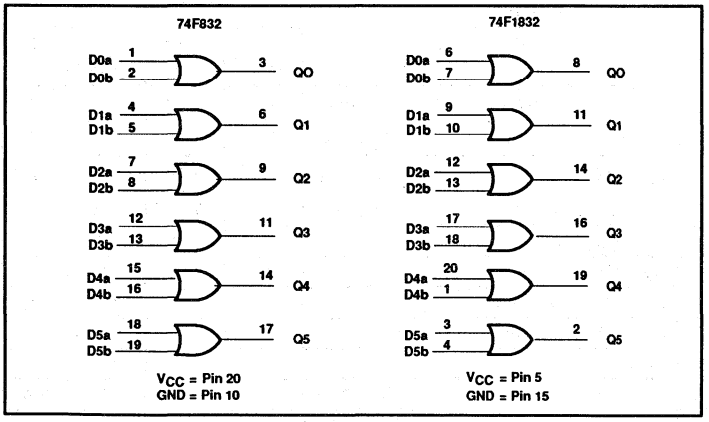
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	Qn
H	X	H
X	H	H
L	L	L

NOTES:
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free–air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High–level output current			–64	mA
I_{OL}	Low–level output current			64	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX		-60		-180	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		21	30	mA
		I_{CCL}		V_{IN} = 4.5V		31	44	mA

NOTES:

6. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
7. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
8. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.

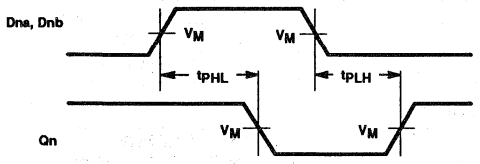
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	Waveform 1	2.0 2.0	4.0 3.5	6.0 6.0	2.0 1.5	6.5 6.5	ns
$t_{sk(o)}$	Output skew[1,2]	Waveform 2			2.0		2.5	ns

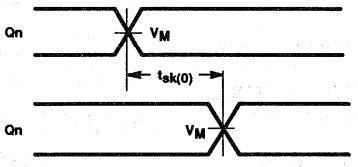
NOTES:

1. $|t_{PN}$ actual – t_{PM} actual| for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



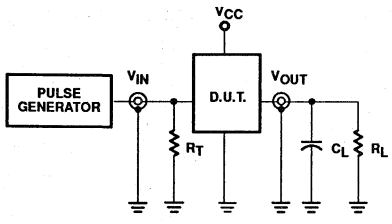
Waveform 1. Propagation delay for inverting output



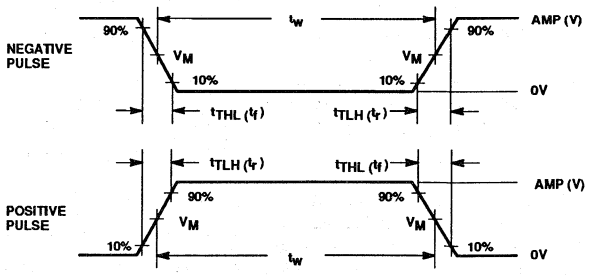
Waveform 2. Output skew

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

Document No.	853-0615
ECN No.	99490
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F835
Shift Register

8-Bit Shift Register with 2:1 Mux-in, Latched "B" inputs, and Serial Out

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F835	150MHz	45mA

FEATURES

- **Specifically designed for Video applications**
- **Combines the 'F373, two 'F157s, and the 'F166 functions in one package**
- **Interleaved loading with 2:1 mux**
- **Dual 8-bit Parallel inputs**
- **Transparent Latch on all "B" inputs**
- **Guaranteed Serial Shift Frequency to 100MHz**
- **Expandable to 16-bits or more with serial input**

DESCRIPTION

The 74F835 is a high speed 8-bit parallel/serial-in, serial-out shift register whose parallel inputs have been connected to an internal octal two-to-one multiplexer with all the 'B' inputs connected to an octal latch.

This 24 pin part is specifically designed for video bit shifting, where interleaved loading is desired and parts count is critical. However, and It is useful in any design where a 2:1 mux input with a transparent latch is needed.

ORDERING INFORMATION

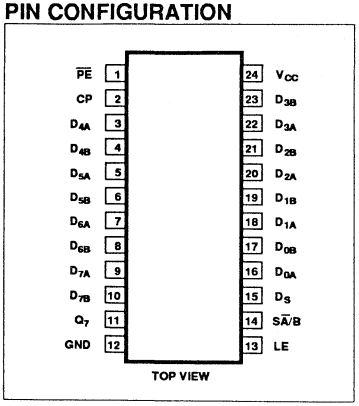
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F835N
24-Pin Plastic SOL	N74F835D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

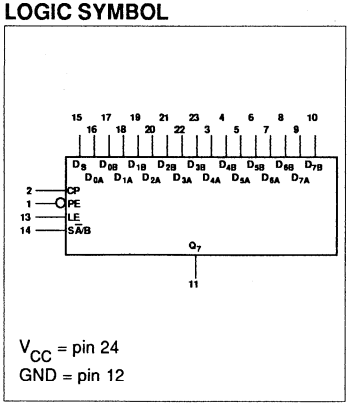
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{0A} - D_{7A}	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{0B} - D_{7B}	Latched Parallel data inputs	1.0/1.0	20µA/0.6mA
D_S	Serial data input	1.0/1.0	20µA/0.6mA
CP	Shift Register Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$S\overline{A}/B$	Mux Select	1.0/1.0	20µA/0.6mA
LE	Latch Enable input (for B inputs)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input	1.0/1.0	20µA/0.6mA
Q_7	Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

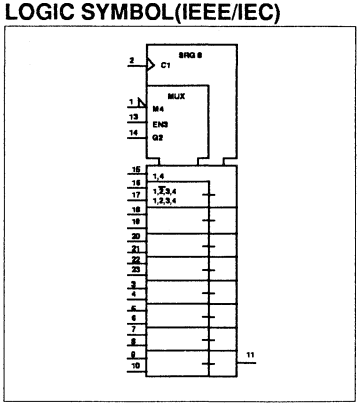
PIN CONFIGURATION



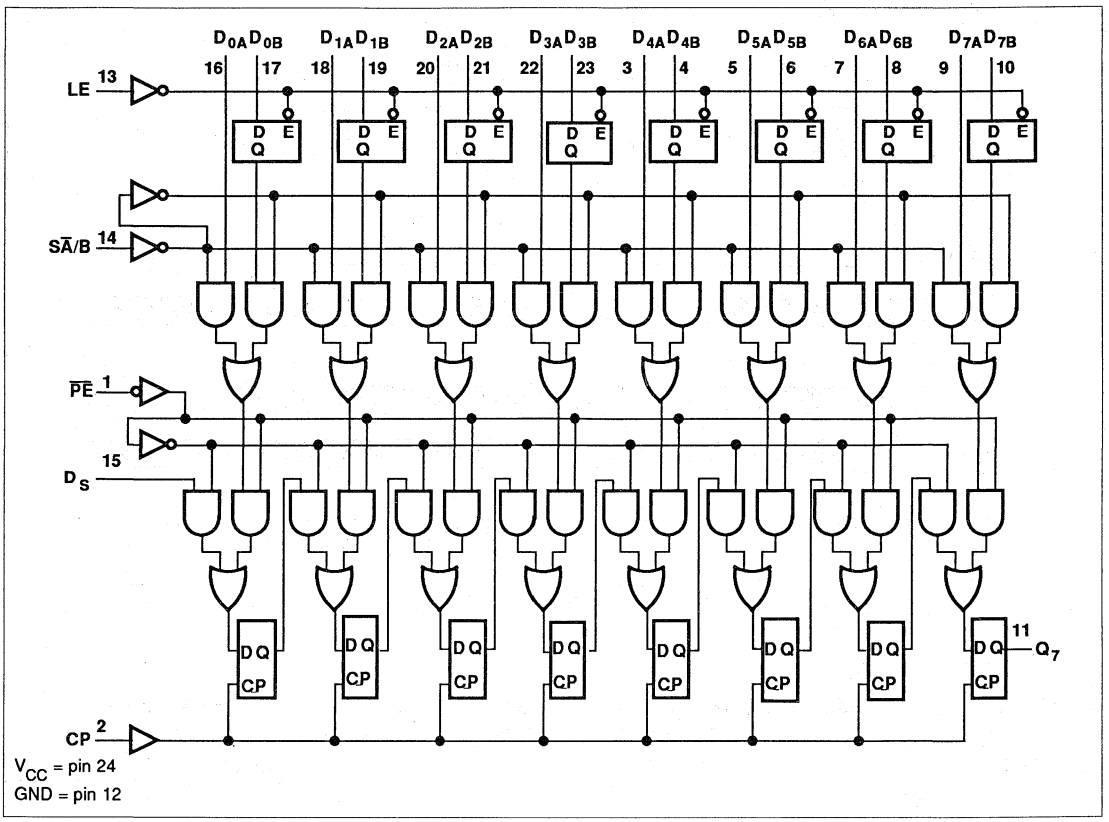
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM

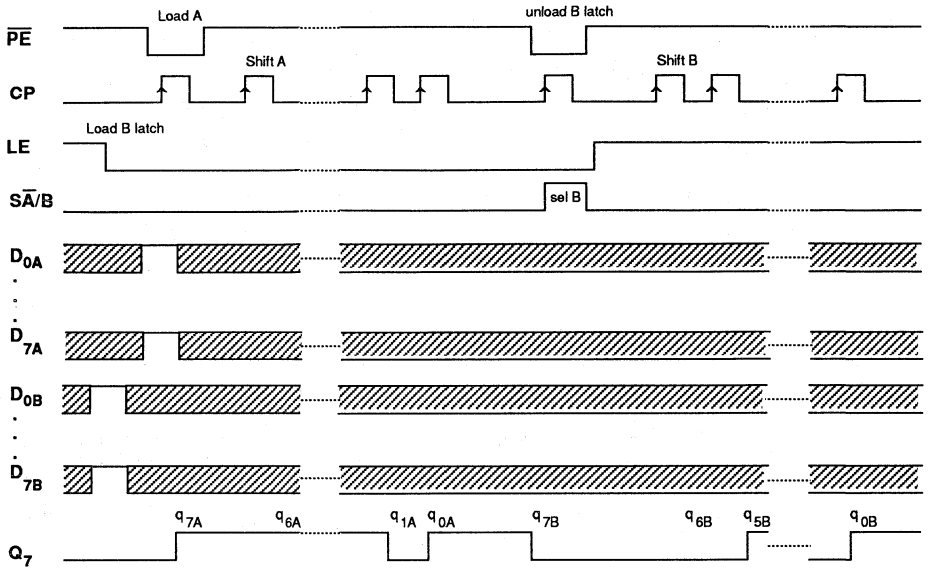


FUNCTION TABLE

OPERATING MODE	INPUTS							INTERNAL			OUTPUT
								B Latch	Serial Reg		
	$\overline{PE}$	CP	LE	$S\overline{A}/B$	D_{nA}	D_{nB}	D_S		Q_0	Q_{1-6}	Q_7
Parallel load A data	L	↑	X	L	h	X	X	X	H	H	H
					l	X	X	X	L	L	L
Latch B data	X	X	L	X	X	h	X	H	X	X	X
					X	l	X	L	X	X	X
Parallel load B data (from Latch)	L	↑	L	H	X	X	X	h	H	H	H
					X	X	X	l	L	L	L
Parallel load B data (Transparent Mode)	L	↑	H	H	X	h	X	h	H	H	H
					X	l	X	l	L	L	L
Serial Shift	H	↑	X	X	X	X	h	X	H	q_{n-1}	q_6
					X	X	l	X	L	q_{n-1}	q_6

H = High voltage level
L = Low voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
q_n = Lower case letters indicate the state of the referenced flop cell one cycle prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

TYPICAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximun input voltage	V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} =MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} =MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} =MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} =MAX			45	65	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

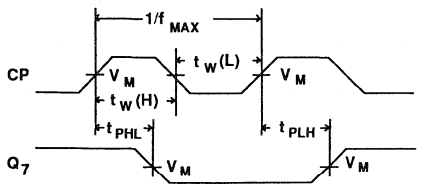
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	130	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_7 (Load)	Waveform 1	5.0 5.0	7.0 7.0	9.5 9.5	5.0 5.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_7 (Shift)	Waveform 1	5.0 5.0	7.0 7.0	9.5 9.5	5.0 5.0	10.0 10.0	ns

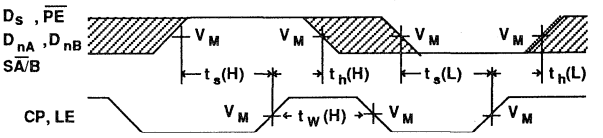
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_{nA} or D_{nB} to CP	Waveform 2	3.5 3.5			3.5 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_{nA} or D_{nB} to CP	Waveform 2	1.0 1.0			1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup time D_S to CP	Waveform 2	1.0 1.0			1.5 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_S to CP	Waveform 2	2.0 2.0			2.5 2.5		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{PE}$ to CP	Waveform 2	3.5 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{PE}$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_{nB} to LE	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_{nB} to LE	Waveform 2	3.0 3.0			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time $S\overline{A}/B$ to CP	Waveform 2	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time $S\overline{A}/B$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	4.5 4.5			5.5 5.0		ns
$t_w(H)$	Latch Enable pulse width, High	Waveform 1	4.5			5.0		ns

AC WAVEFORMS



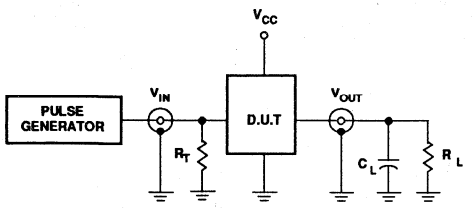
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data and Select Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



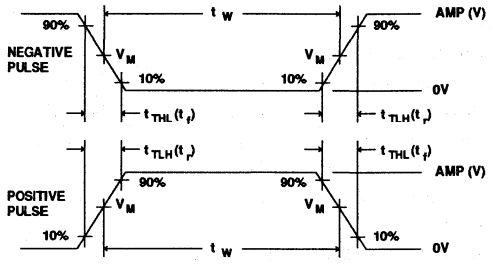
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Bus Interface Latches — FAST 74F841/842/843/844/845/846

'F841/'F842 10-bit bus interface latches, NINV/INV (3-State); 'F843/'F844 9-bit bus interface latches, NINV/INV (3-State); 'F845/'F846 8-bit bus interface latches, NINV/INV (3-State)

FEATURES

- High speed parallel latches
- Extra data width for wide address/ data paths or busses carrying parity
- High impedance NPN base input structure minimizes bus loading
- I_{IL} is 20µA vs 1000µA for AM29841 series
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- 48mA sink current
- Slim Dip 300 mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29841-846 series

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	5.5ns	60mA
74F843, 74F845	5.5ns	75mA
74F844, 74F846	6.2ns	60mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C
24-pin plastic Slim DIP (300mil)	N74F841N, N74F842N, N74F843N, N74F844N, N74F845N, N74F846N
24-pin plastic SOL	N74F841D, N74F842D, N74F843D, N74F844D, N74F845D, N74F846D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/0.033	20µA/20µA
LE	Latch Enable input	1.0/0.033	20µA/20µA
$\overline{OE}$, $\overline{OE}$n	Output Enable input (active Low)	1.0/0.033	20µA/20µA
$\overline{MR}$	Master Reset input (active Low)	1.0/0.033	20µA/20µA
$\overline{PRE}$	Preset input (active Low)	1.0/0.033	20µA/20µA
Qn	Data outputs	1200/80	24mA/48mA
$\overline{Q}$n	Data outputs	1200/80	24mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

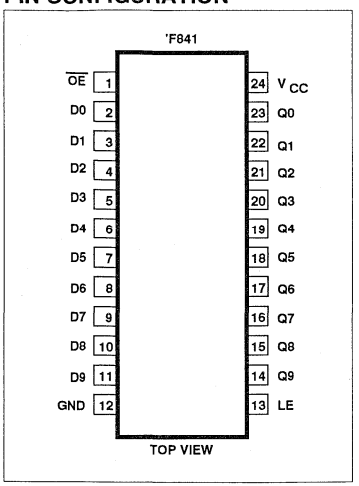
The 'F841-'846 bus interface latch series are designed to provide extra data width for wider address/data paths of busses carrying parity.

The 'F841-'F846 series are functionally and pin compatible to the AMD AM29841-AM29846 series.

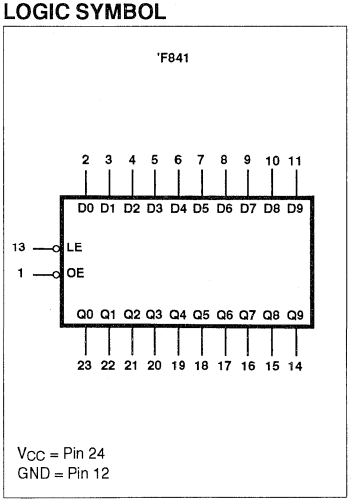
The 'F841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

(continued)

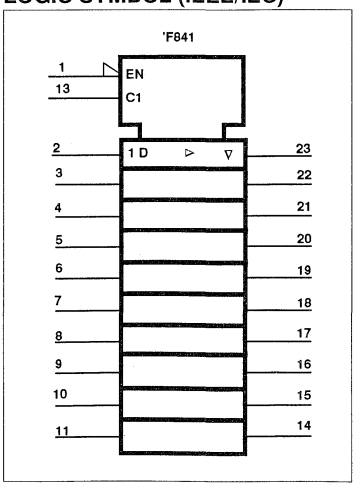
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Data appears on the bus when the Output Enable (OE) is Low. When OE is High the output is in the High-impedance state.

The 'F842 is the inverted output version of the 'F841.

The 'F843 consists of nine D-type latches with 3-State outputs. In addition to the LE and OE pins, the 'F843 has a Master Reset (MR) pin and Preset (PRE) pin. These pins are ideal for parity bus interfacing in high performance systems. When MR is Low, the outputs are Low if OE is Low. When MR is High, data can be entered into the latch. When PRE is Low, the outputs are High, if OE is Low. PRE overrides MR.

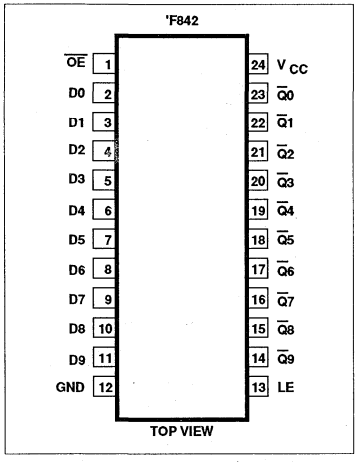
The 'F844 is the inverted output version of the 'F843.

The 'F845 consists of eight D-type latches with 3-State outputs. In addition to the LE, OE, MR and PRE pins, the 'F845 has two additional OE pins making a total of three Output Enables (OE0, OE1, OE2) pins.

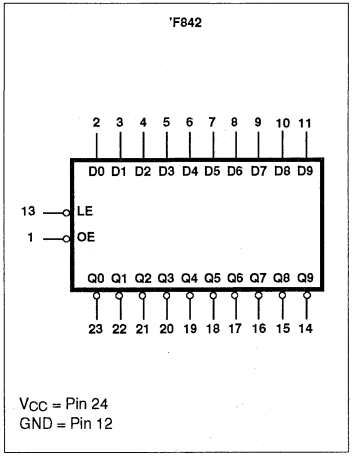
The multiple Output Enables (OE0, OE1, OE2) allow multi-user control of the interface, e.g., CS, DMA, and RD/WR.

The 'F846 is the inverted output version of the 'F845.

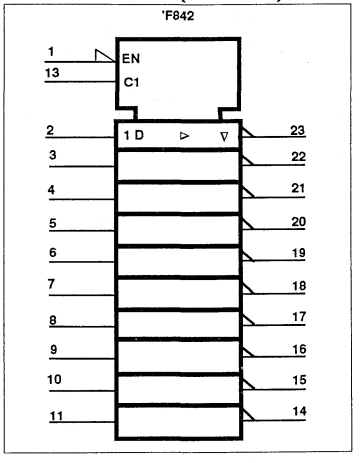
PIN CONFIGURATION



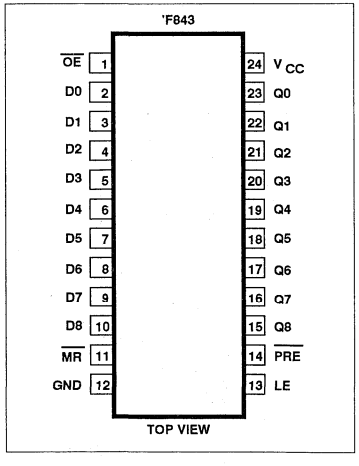
LOGIC SYMBOL



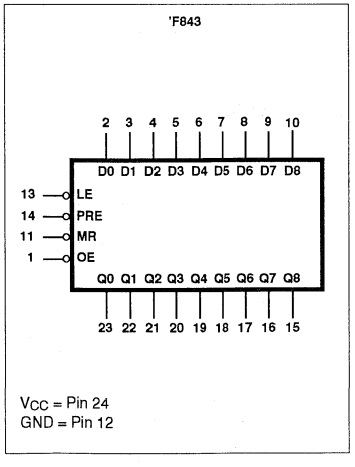
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



LOGIC SYMBOL



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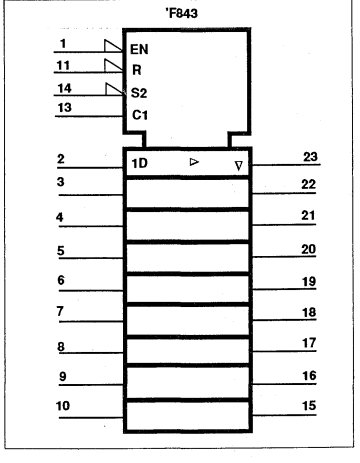
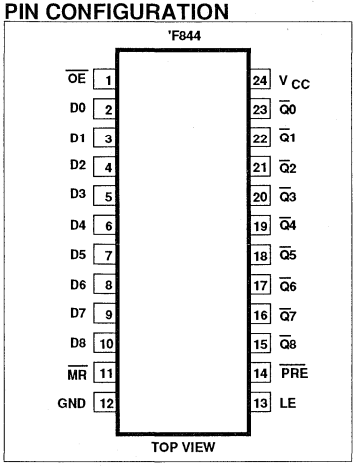
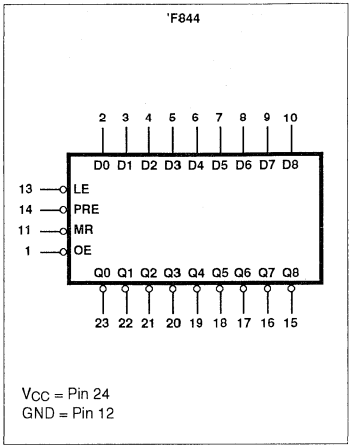


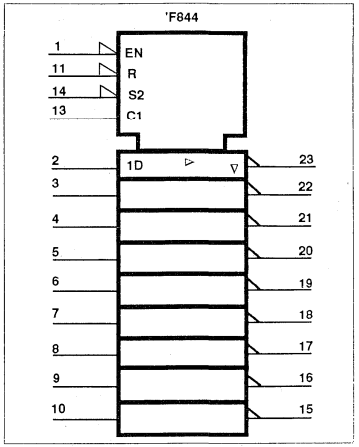
PIN CONFIGURATION



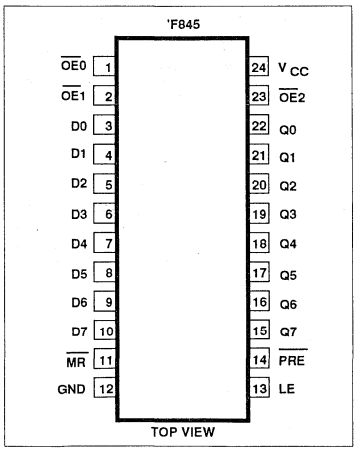
LOGIC SYMBOL



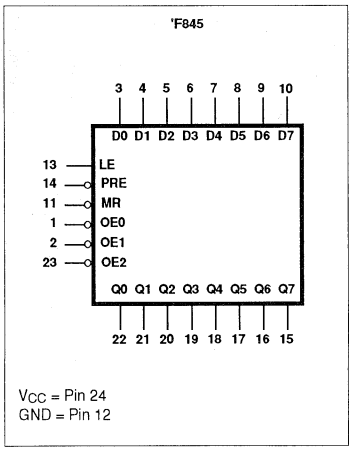
LOGIC SYMBOL (IEEE/IEC)



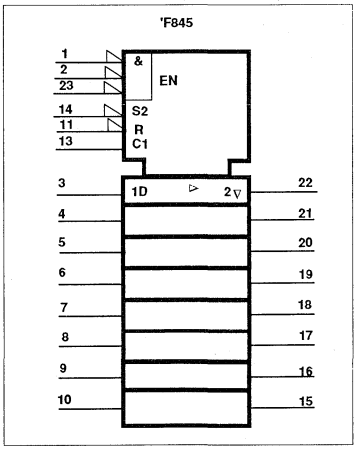
PIN CONFIGURATION



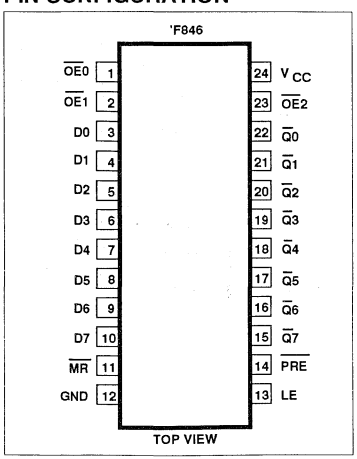
LOGIC SYMBOL



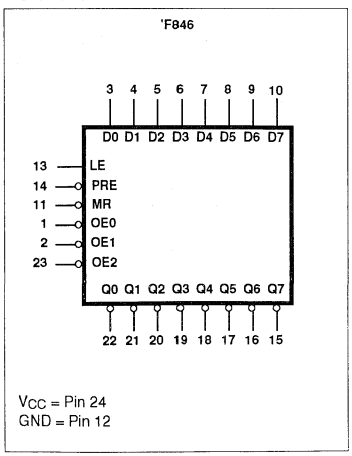
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



LOGIC SYMBOL



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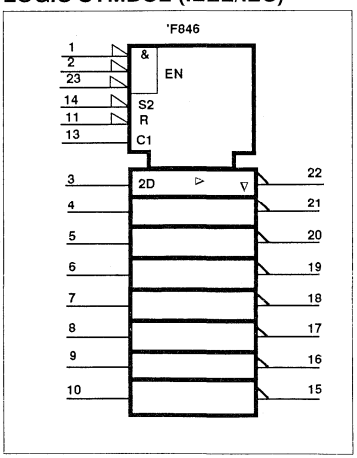
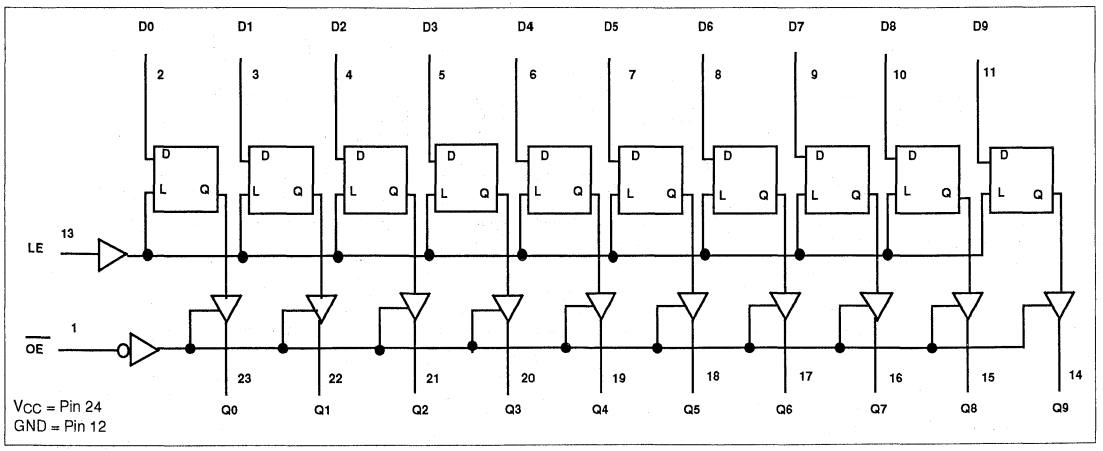
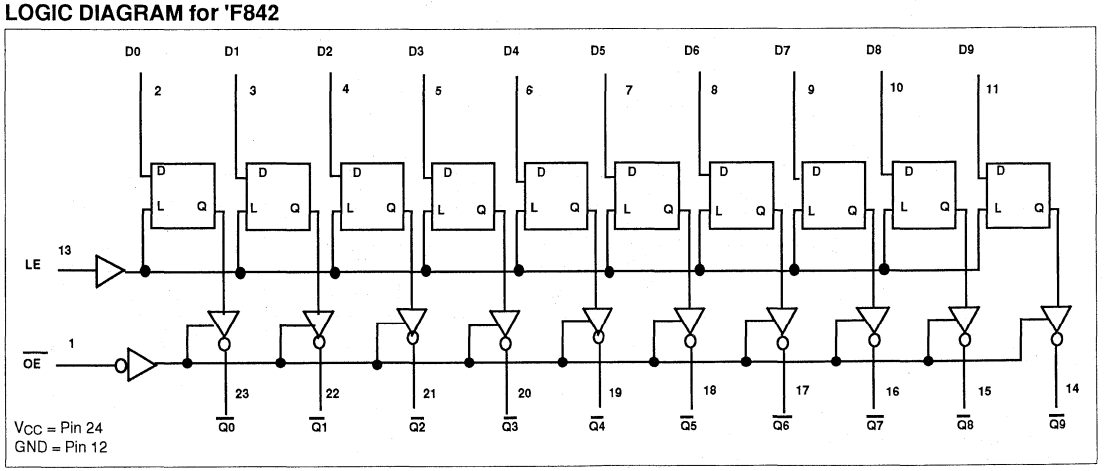


LOGIC DIAGRAM for 'F841



LOGIC DIAGRAM for 'F842

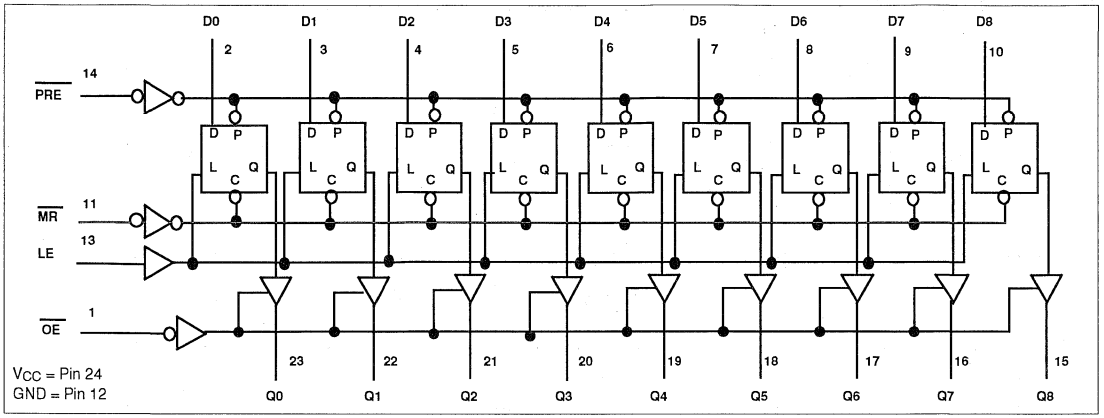


FUNCTION TABLE for 'F841 and 'F842

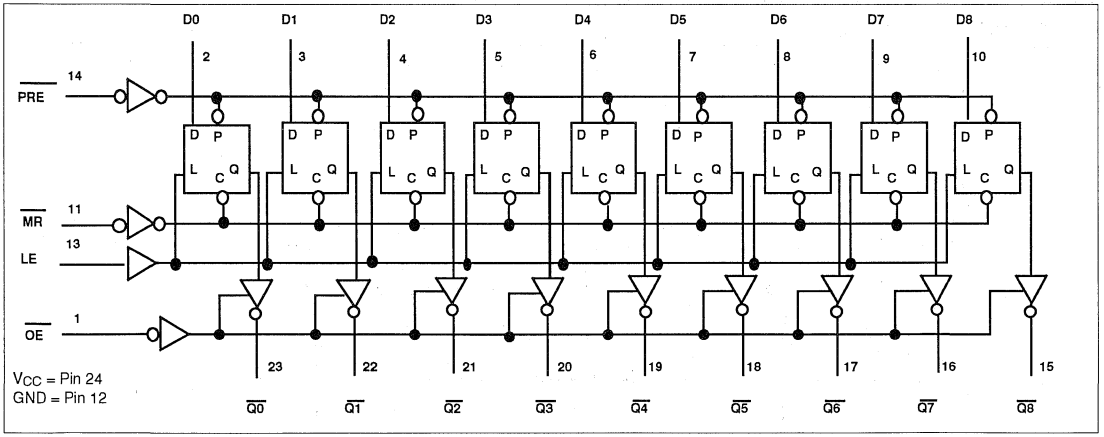
INPUTS			OUTPUTS		OPERATING MODE
			'F841	'F842	
OE	LE	Dn	Q	Qn	
L	H	L	L	H	Transparent
L	H	H	H	L	
L	↓	l	L	H	Latched
L	↓	h	H	L	
H	X	X	Z	Z	High impedance
L	L	X	NC	NC	Hold

H = High voltage level
L = Low voltage level
h = High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓ = High-to-Low transition
X = Don't care
NC = No change
Z = High impedance "off" state

LOGIC DIAGRAM for 'F843



LOGIC DIAGRAM for 'F844

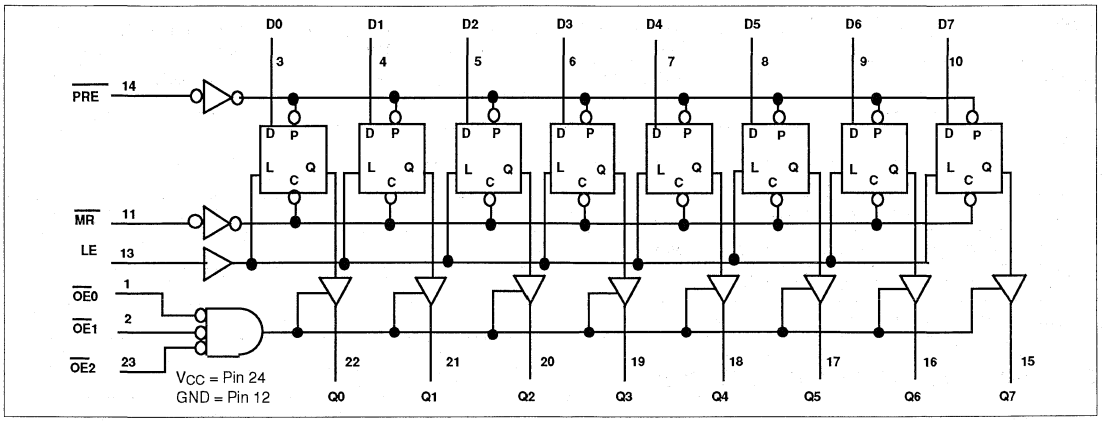


FUNCTION TABLE for 'F843 and 'F844

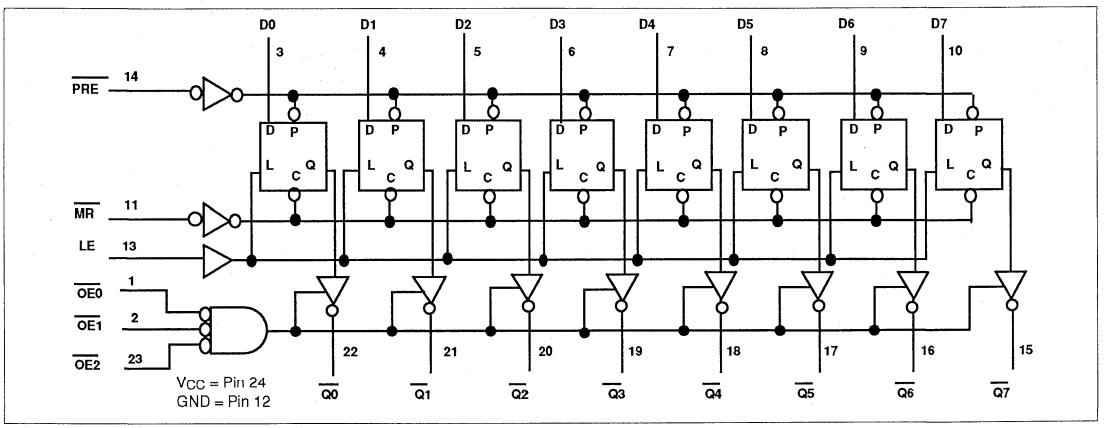
INPUTS					OUTPUTS		OPERATING MODE
					'F843	'F844	
OE	PRE	MR	LE	Dn	Q	Qn	
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L L	H H	H H	H H	L H	L H	H L	Transparent
L L	H H	H H	↓ ↓	l h	L H		Latched
H	X	X	X	X	Z	Z	High impedance
L	H	H	L	X	NC	NC	Hold

H = High voltage level
L = Low voltage level
h = High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓ = High-to-Low transition
X = Don't care
NC = No change
Z = High impedance "off" state

LOGIC DIAGRAM for 'F845



LOGIC DIAGRAM for 'F846



FUNCTION TABLE for 'F845 and 'F846

INPUTS					OUTPUTS		OPERATING MODE
					'F845	'F846	
OEn	PRE	MR	LE	Dn	Q	Qn	
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L L	H H	H H	H H	L H	L H	H L	Transparent
L L	H H	H H	↓ ↓	l h	L H	H L	Latched
H	X	X	X	X	Z	Z	High impedance
L	H	H	L	X	NC	NC	Hold

H = High voltage level
L = Low voltage level
h = High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓ = High-to-Low transition
X = Don't care
NC = No change
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	84	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output voltage			-24	mA
I_{OL}	Low-level output voltage			48	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS [1]			LIMITS			UNIT
					Min	Typ [2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.2			V
				±5%V_{CC}	2.2	3.3		
			I_{OH} = -24mA	±10%V_{CC}	2.0			
				±5%V_{CC}	2.0			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 32mA	±10%V_{CC}		0.38	0.55	V
			I_{OL} = 48mA	±5%V_{CC}		0.38	0.55	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current [3]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F841	I_{CCH}	V_{CC} = MAX		50	65	mA
			I_{CCL}			60	80	
			I_{CCZ}			70	92	
		'F842	I_{CCH}	V_{CC} = MAX		40	60	
			I_{CCL}			65	90	
			I_{CCZ}			60	90	
		'F843 'F845	I_{CCH}	V_{CC} = MAX		65	90	
			I_{CCL}			75	100	
			I_{CCZ}			85	115	
		'F844 'F846	I_{CCH}	V_{CC} = MAX		50	70	
			I_{CCL}			70	95	
			I_{CCZ}			70	95	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F841/74F842

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn or $\overline{Qn}$	'F841	Waveform 1, 2	2.0 2.5	4.0 4.5	7.5 7.5	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn or $\overline{Qn}$	'F841	Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 9.0	4.0 3.5	10.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay Dn to Qn or $\overline{Qn}$	'F842	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	4.5 4.0	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn or $\overline{Qn}$	'F842	Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	3.0 3.0	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time High or Low-level $\overline{OE}$n to Qn or $\overline{Qn}$		Waveform 5 Waveform 6	2.5 4.0	4.5 6.0	8.0 9.5	2.0 3.0	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time High or Low-level $\overline{OE}$n to Qn or $\overline{Qn}$		Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC ELECTRICAL CHARACTERISTICS FOR 74F841/74F842

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to LE		Waveform 4	0.0 0.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to LE	'F841	Waveform 4	2.5 3.0			3.0 4.0		ns
$t_w(H)$	LE Pulse width, High	'F841	Waveform 4	3.5			4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to LE	'F842	Waveform 4	3.0 3.5			3.5 4.5		ns
$t_w(H)$	LE Pulse width, High	'F842	Waveform 4	3.0			3.0		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F843/74F845

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn or $\overline{Qn}$	Waveform 1, 2	2.0 2.5	4.5 4.5	7.5 8.0	2.0 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn or $\overline{Qn}$	Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 8.5	4.5 4.0	10.0 8.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to Qn or $\overline{Qn}$	Waveform 3	3.5	5.5	8.5	3.0	9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn or $\overline{Qn}$	Waveform 3	2.0	4.5	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output enable time High or Low-level $\overline{OE}$n to Qn or $\overline{Qn}$	Waveform 5 Waveform 6	2.5 4.0	4.5 6.0	7.5 9.5	2.0 3.0	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time High or Low-level $\overline{OE}$n to Qn or $\overline{Qn}$	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC ELECTRICAL CHARACTERISTICS FOR 74F843/74F845

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low Dn to LE	Waveform 4						ns
t_h(H) t_h(L)	Hold time, High or Low Dn to LE	Waveform 4						ns
t_w(H)	LE Pulse width, High	Waveform 4						ns
t_w(L)	$\overline{PRE}$ Pulse width, Low	Waveform 3						ns
t_w(H)	$\overline{MR}$ Pulse width, Low	Waveform 3						ns
t_{REC}	$\overline{PRE}$ recovery time	Waveform 3						ns
t_{REC}	$\overline{MR}$ recovery time	Waveform 3						ns

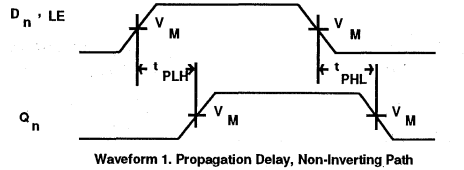
AC ELECTRICAL CHARACTERISTICS FOR 74F844/74F846

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn or $\overline{Qn}$	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 3.0	9.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn or $\overline{Qn}$	Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	5.0 4.5	10.5 9.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to Qn or $\overline{Qn}$	Waveform 3	3.5	5.5	8.5	3.0	9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn or $\overline{Qn}$	Waveform 3	5.0	7.0	10.0	4.5	10.5	ns
t_{PZH} t_{PZL}	Output enable time High or Low-level $\overline{OE}$n to Qn or $\overline{Qn}$	Waveform 5 Waveform 6	2.5 4.0	5.0 6.0	7.5 9.5	2.0 3.0	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time High or Low-level $\overline{OE}$n to Qn or $\overline{Qn}$	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

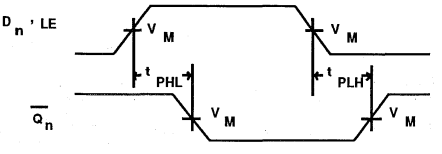
AC ELECTRICAL CHARACTERISTICS FOR 74F844/74F846

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to LE	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to LE	Waveform 4	3.0 4.0			3.0 4.0		ns
$t_w(H)$	LE Pulse width, High	Waveform 4	3.0			3.0		ns
$t_w(L)$	$\overline{PRE}$ Pulse width, Low	Waveform 3	4.0			5.0		ns
$t_w(H)$	$\overline{MR}$ Pulse width, Low	Waveform 3	4.0			5.0		ns
t_{REC}	$\overline{PRE}$ recovery time	Waveform 3	0.0			0.0		ns
t_{REC}	$\overline{MR}$ recovery time	Waveform 3	3.5			4.5		ns

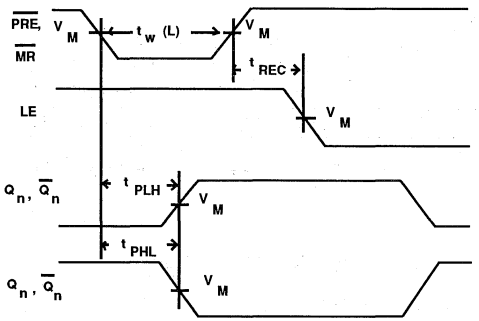
AC WAVEFORMS



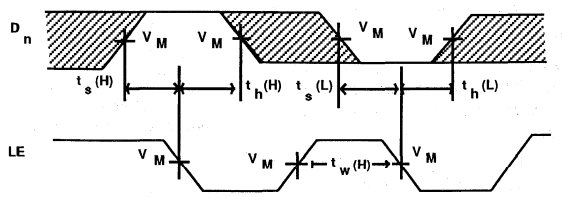
Waveform 1. Propagation Delay, Non-Inverting Path



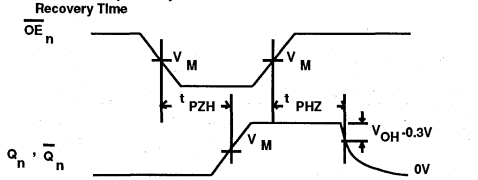
Waveform 2. Propagation Delay, Inverting Path



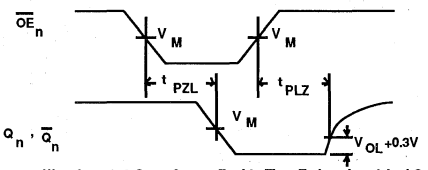
Waveform 3. Master Reset and Preset Pulse Width, Master Reset and Preset to Output Delay and Master Reset and Preset to Latch Enable Recovery Time



Waveform 4. Data Setup And Hold Times

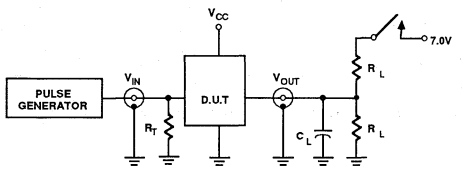


Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

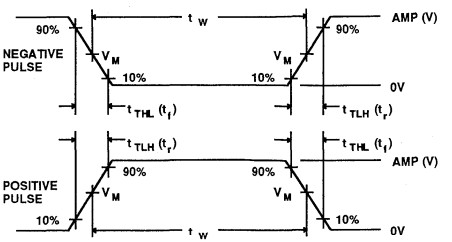
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0881
ECN No.	95975
Date of issue	March 7, 1989
Status	Product Specification
FAST Products	

FAST 74F861, 74F862, 74F863, 74F864 Bus Transceivers

'F861/'F862 10-Bit Bus Transceivers, NINV/INV (3-State)
'F863/'F864 9-Bit Bus Transceivers, NINV/INV (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F861, 74F862	6.0ns	150mA
74F863, 74F864	6.0ns	115mA

FEATURES

- **Provide high performance bus interface buffering for wide data/address paths or busses carrying parity**
- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **I_{IL} is 20μA vs 1000μA for AM29861 series**
- **Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-state outputs glitch free during power-up and power-down**
- **Slim Dip 300 mil package**
- **Broadside pinout compatible with AMD AM 29861-29864 series**
- **Outputs sink 64mA**

DESCRIPTION

The 74F861 series Bus Transceivers provide high performance bus interface buffering for wide data/address paths of busses carrying parity. The 'F863/'F864 9-bit Bus Transceivers have NOR-ed transmit and receive output enables for

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F861N, N74862N, 74F863N, N74F864N
24-Pin Plastic SOL[1]	N74F861D, N74F862D, 74F863D, N74F864D

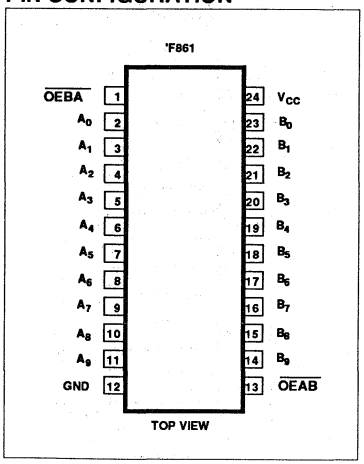
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

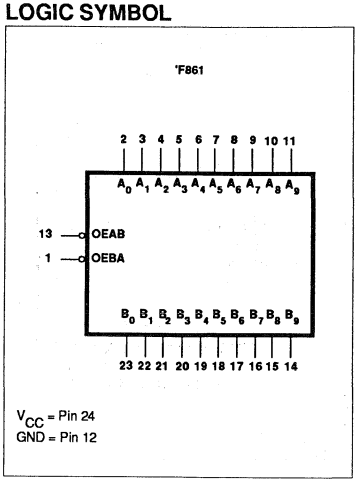
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F861 'F862	A_0 - A_9	Data transmit inputs	3.5/0.117	70μA/70μA
	B_0 - B_9	Data receive inputs	3.5/0.117	70μA/70μA
	$\overline{OEBA}$	Transmit output enable input	1.0/0.033	20μA/20μA
	$\overline{OEAB}$	Receive output enable input	1.0/0.033	20μA/20μA
	A_0 - A_9	Data transmit outputs	1200/106.7	24mA/64mA
	B_0 - B_9	Data receive outputs	1200/106.7	24mA/64mA
'F863 'F864	A_0 - A_9	Data transmit inputs	3.5/0.117	70μA/70μA
	B_0 - B_9	Data receive inputs	3.5/0.117	70μA/70μA
	$\overline{OEBA}_n$	Transmit output enable inputs	1.0/0.033	20μA/20μA
	$\overline{OEAB}_n$	Receive output enable inputs	1.0/0.033	20μA/20μA
	A_0 - A_8	Data transmit outputs	1200/106.7	24mA/64mA
	B_0 - B_8	Data receive outputs	1200/106.7	24mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

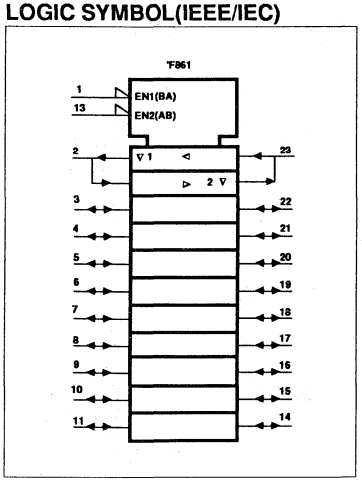
PIN CONFIGURATION



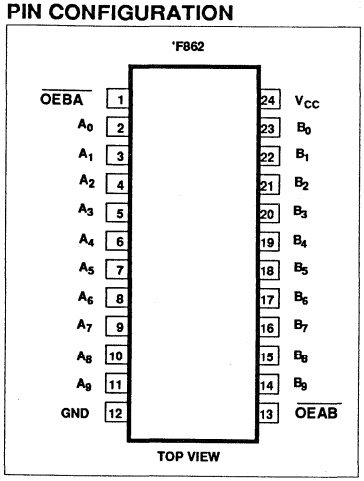
LOGIC SYMBOL



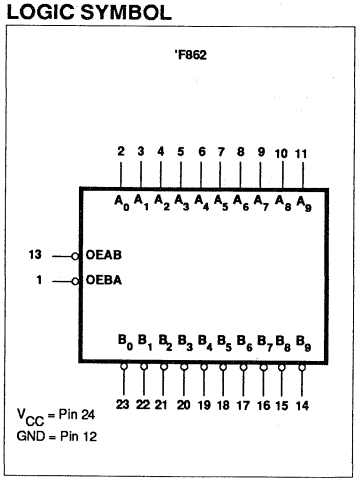
LOGIC SYMBOL(IEEE/IEC)



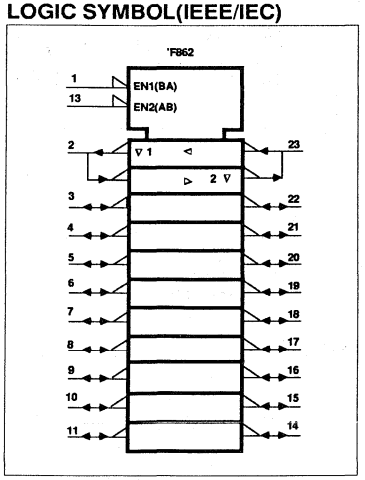
PIN CONFIGURATION



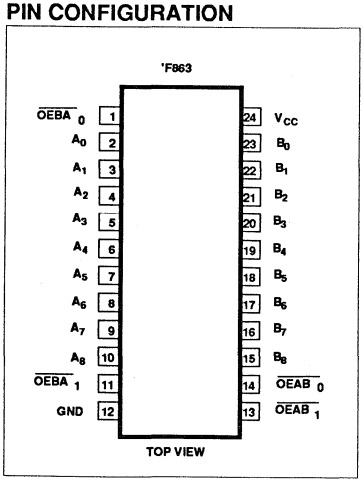
LOGIC SYMBOL



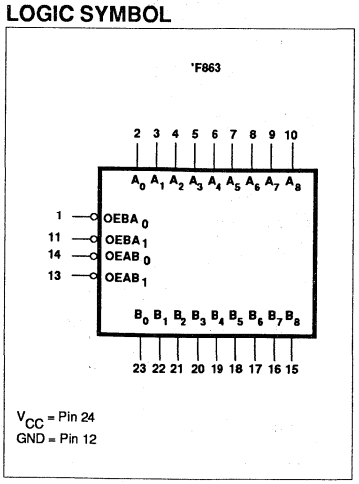
LOGIC SYMBOL(IEEE/IEC)



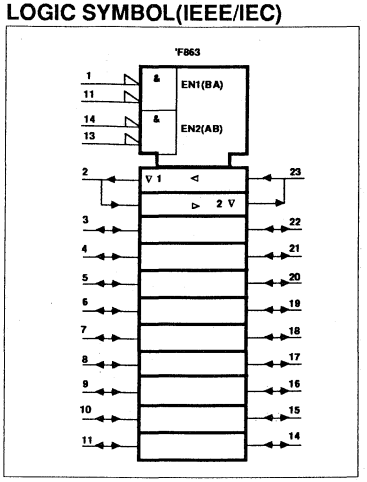
PIN CONFIGURATION



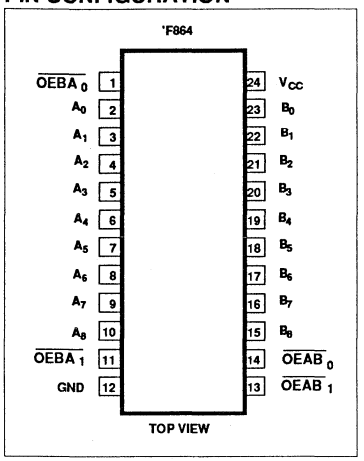
LOGIC SYMBOL



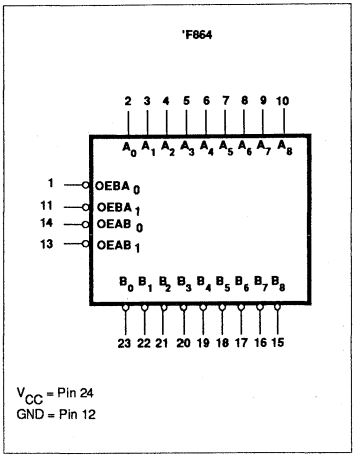
LOGIC SYMBOL(IEEE/IEC)



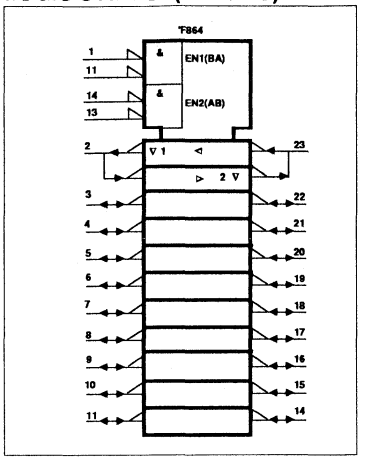
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

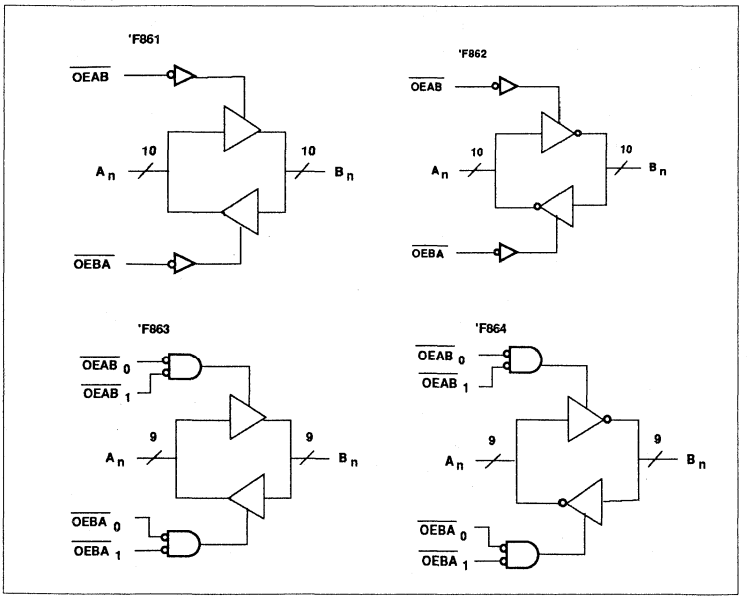


FUNCTION TABLE for 'F861 and 'F862

INPUTS		OPERATING MODES	
$\overline{OEAB}$	$\overline{OEBA}$	'F861	'F862
L	H	A data to B bus	A data to B bus
H	L	B bus to A data	B bus to A data
H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

LOGIC DIAGRAM



FUNCTION TABLE for 'F863 and 'F864

INPUTS				OPERATING MODES	
$\overline{OEAB}_0$	$\overline{OEAB}_1$	$\overline{OEBA}_0$	$\overline{OEBA}_1$	'F863	'F864
L	L	H	X	A data to B bus	A data to B bus
L	L	X	H		
H	X	L	L	B bus to A data	B bus to A data
X	H	L	L		
H	H	H	H	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.4	3.3		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-24mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} =MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$ $\overline{OEAB_n}$, $\overline{OEBA_n}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	A_n, B_n	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	A_n, B_n 'F861 'F863	I_{CCH}	V_{CC} = MAX			145	195	mA
			I_{CCL}				140	195	mA
			I_{CCZ}				165	220	mA
		'F862 'F864	I_{CCH}	V_{CC} = MAX			90	130	mA
			I_{CCL}				120	170	mA
			I_{CCZ}				130	160	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

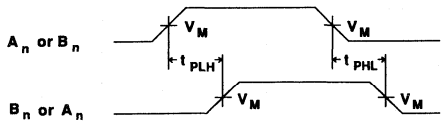
AC ELECTRICAL CHARACTERISTICS for 74F861 and 74F863

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n	Waveform 1	4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n or A_n	Waveform 1	4.0 2.5	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.0 4.5	8.0 7.0	11.5 10.5	5.0 4.5	13.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.0 5.5	8.0 7.5	11.0 11.0	5.0 4.5	13.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.5 2.5	5.5 5.0	9.0 8.5	3.0 2.0	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.5 2.5	5.5 4.5	8.5 8.5	3.0 2.0	9.5 9.5	ns

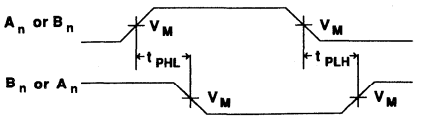
AC ELECTRICAL CHARACTERISTICS for 74F862 and 74F864

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n or A_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.5 7.0	8.5 9.5	12.0 13.5	5.5 6.0	13.5 15.5	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.5 7.5	8.0 9.5	11.5 13.5	5.5 6.5	13.5 15.5	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns

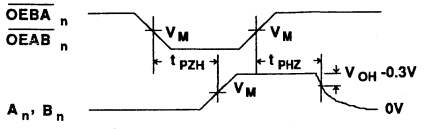
AC WAVEFORMS



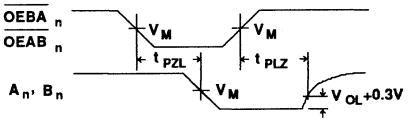
Waveform 1. Propagation Delay For Non-Inverting Output



Waveform 2. Propagation Delay For Inverting Output



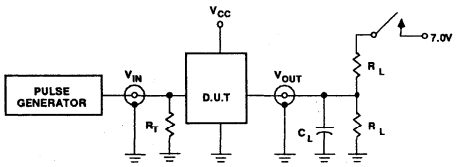
Waveform 3 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

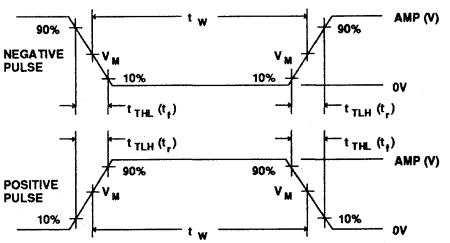
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0039
ECN No.	96220
Date of issue	April 4, 1989
Status	Product Specification
FAST Products	

FAST 74F1240, 74F1241 Buffers

74F1240 Octal Inverter Buffer (3-State)
74F1241 Octal Buffer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1240	3.5ns	40mA
74F1241	4.5ns	46mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Low power, light loading**
- **Functional pin for pin equivalent of 'F240 and 'F241**
- **1/30th the bus loading of 'F240 and 'F241**
- **Provides ideal interface and increase fan-out of MOS Microprocessors**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION

The 74F1240 and 74F1241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_n$, each controlling four of the 3-state outputs.

ORDERING INFORMATION

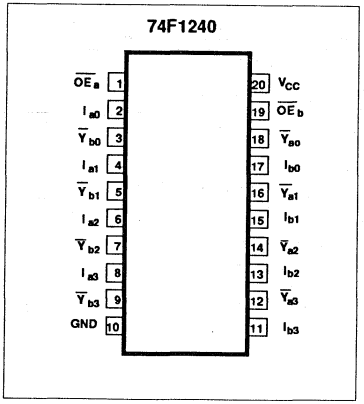
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F1240N, N74F1241N
20-Pin Plastic SOL	N74F1240D, N74F1241D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

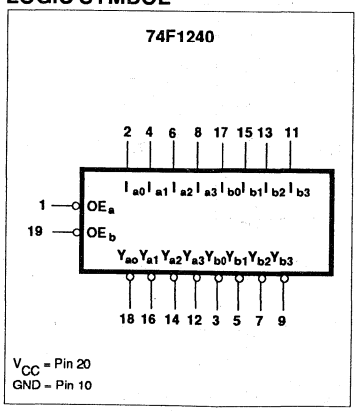
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/0.033	20μA/20μA
I_{an}, I_{bn}	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_a$, $\overline{OE}_b$	Output enable input (active Low)	1.0/0.033	20μA/20μA
OE_b	Output enable input (active High, 'F1241)	1.0/0.033	20μA/20μA
Y_{an}, Y_{bn}	Data outputs ('F1241)	750/106.7	15mA/64mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs ('F1240)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

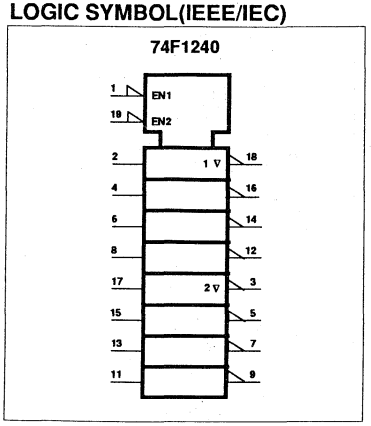
PIN CONFIGURATION



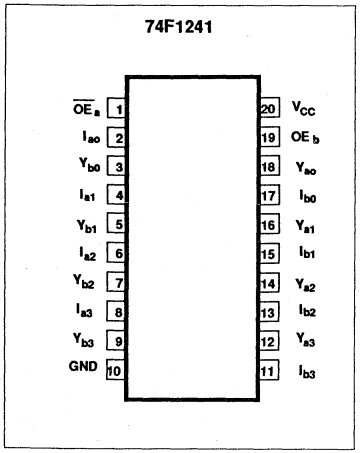
LOGIC SYMBOL



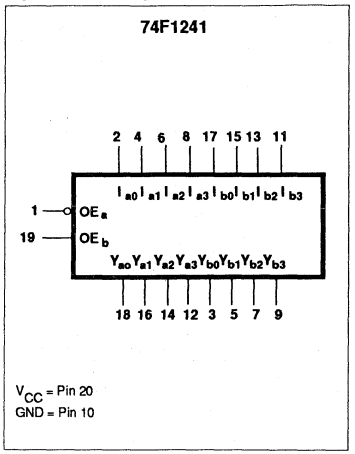
LOGIC SYMBOL(IEEE/IEC)



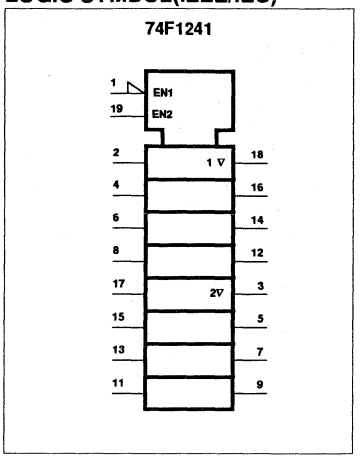
PIN CONFIGURATION



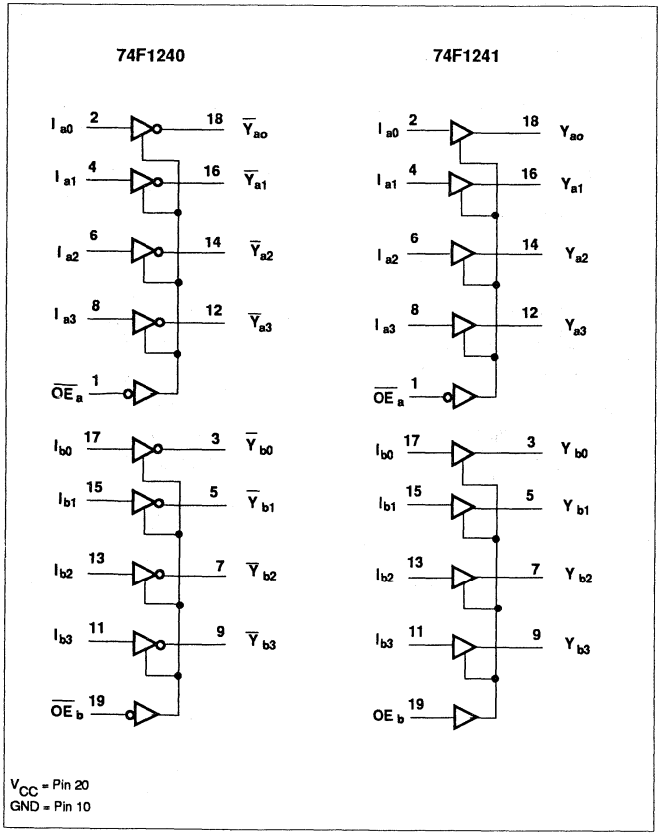
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM,



FUNCTION TABLE, 74F1240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

FUNCTION TABLE, 74F1241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10% V_{CC}	2.4			V
						±5% V_{CC}	2.7	3.3		V
					I_{OH} = -15mA	±10% V_{CC}	2.0			V
						±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
					I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5 V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F1240	I_{CCH}	V_{CC} = MAX				22	30	mA
			I_{CCL}					58	75	mA
			I_{CCZ}					44	58	mA
		74F1241	I_{CCH}	V_{CC} = MAX				33	44	mA
			I_{CCL}					62	80	mA
			I_{CCZ}					45	60	mA

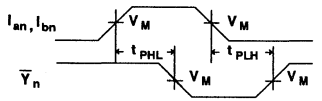
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

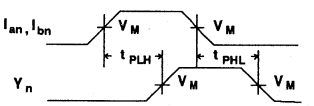
AC CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to $\overline{Y}_n$	74F1240	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	7.5 9.0	3.0 4.0	8.0 9.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F1241	Waveform 2	2.5 2.5	4.0 5.0	5.5 6.5	2.5 2.5	6.0 7.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.0 8.0	3.0 3.0	7.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	3.0 3.0	5.5 6.0	7.5 8.0	3.0 3.0	8.5 8.5	ns ns

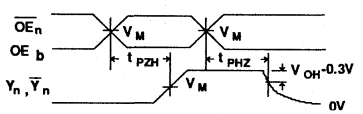
AC WAVEFORMS



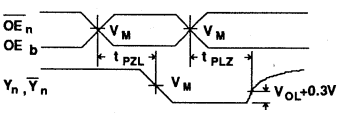
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



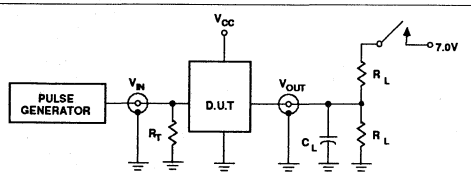
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

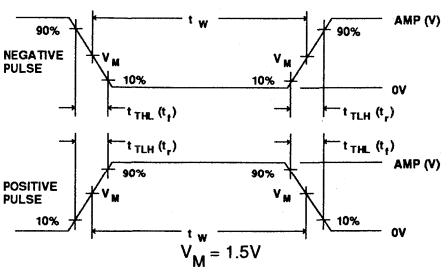
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0040
ECN No.	94761
Date of issue	October 7, 1988
Status	Product Specification
FAST Products	

FAST 74F1242, 74F1243 Transceivers

74F1242 Quad Transceiver, Inverting (3-State)
74F1243 Quad Transceiver (3-State)

FEATURES

- **High impedance NPN base inputs for reduced loading (70µA in High and Low states)**
- **Low power, light-bus loading**
- **Functional pin for pin equivalent of 'F242 and 'F243**
- **1/30th the bus loading of 'F242 and 'F243**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **3-State buffer outputs sink 64mA and source 15mA**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1242	3.5ns	43mA
74F1243	4.5ns	44mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F1242N, N74F1243N
14-Pin Plastic SO	N74F1242D, N74F1243D

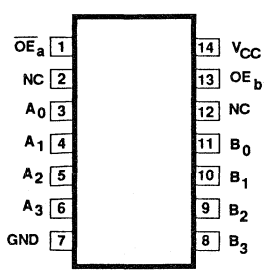
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs	3.5/0.117	70µA/70µA
$\overline{OE}_a$	Output Enable input (active Low)	1.0/0.033	20µA/20µA
OE_b	Output Enable input	1.0/0.033	20µA/20µA
A_n, B_n	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

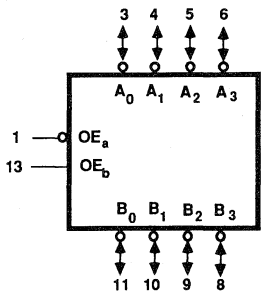
'F1242



TOP VIEW

LOGIC SYMBOL

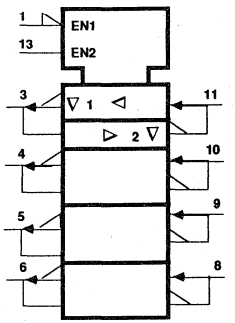
'F1242



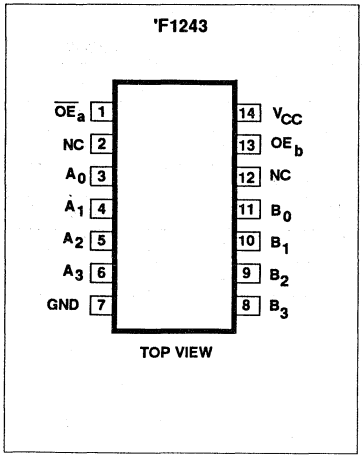
V_{CC} = Pin 14
GND = Pin 7
NC = Pin 2, 12

LOGIC SYMBOL(IEEE/IEC)

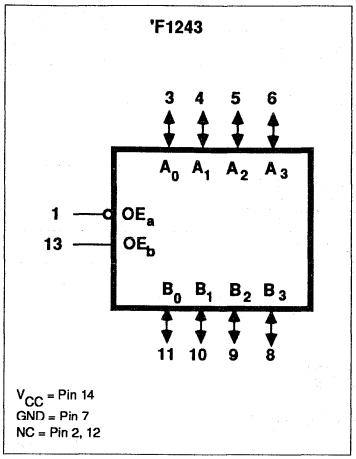
'F1242



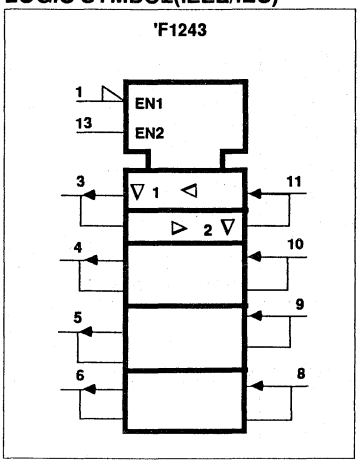
PIN CONFIGURATION



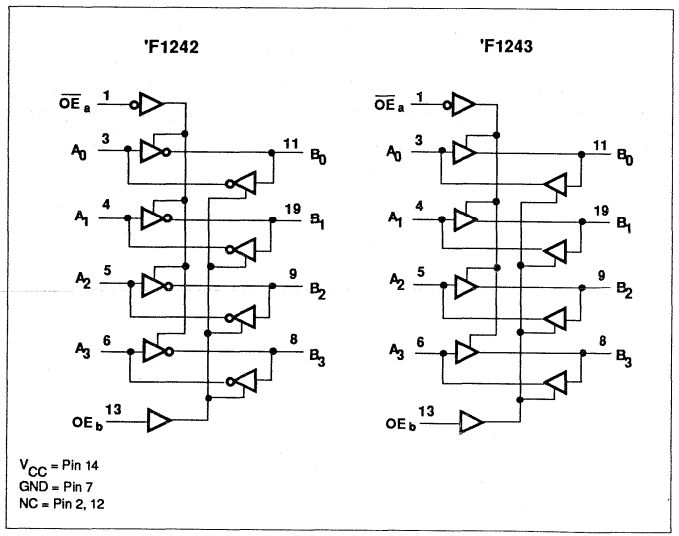
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE, 'F1242

INPUTS		OUTPUTS	
$\overline{OE}_a$	OE_b	A_n	B_n
L	L	INPUT	$B=\overline{A}$
H	L	Z	Z
L	H	a	a
H	H	$A=\overline{B}$	INPUT

FUNCTION TABLE, 'F1243

INPUTS		OUTPUTS	
$\overline{OE}_a$	OE_b	A_n	B_n
L	L	INPUT	B=A
H	L	Z	Z
L	H	a	a
H	H	A=B	INPUT

H = High voltage level
L = Low voltage level
Z = High impedance "off" state
a = This condition is not allowed due to excessive currents

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	A_0-A_3, B_0-B_3	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
		$\overline{OE}_a$, OE_b	V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	$\overline{OE}_a$, OE_b only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{IH}+I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F1242	I_{CCH}	V_{CC} = MAX			35	46	mA
			I_{CCL}				50	72	mA
			I_{CCZ}				45	60	mA
		'F1243	I_{CCH}	V_{CC} = MAX			40	50	mA
			I_{CCL}				52	65	mA
			I_{CCZ}				44	60	mA

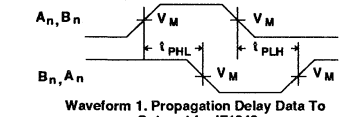
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

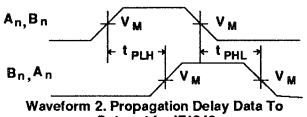
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	'F1242	Waveform 1	3.0 1.5	4.5 2.5	6.0 4.0	3.0 1.5	6.5 4.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F1242	Waveform 3 Waveform 4	3.5 3.0	5.5 5.5	7.5 7.5	3.0 3.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	'F1242	Waveform 3 Waveform 4	3.5 3.0	6.0 5.0	8.0 7.5	3.5 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	'F1243	Waveform 2	2.0 3.0	4.0 5.0	5.5 6.5	2.0 3.0	6.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F1243	Waveform 3 Waveform 4	2.5 2.5	5.5 5.0	8.0 7.5	2.5 2.5	8.5 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	'F1243	Waveform 3 Waveform 4	3.5 2.0	6.5 5.0	8.5 7.5	3.0 2.0	9.0 8.0	ns

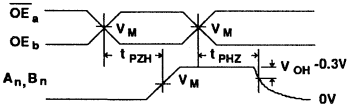
AC WAVEFORMS



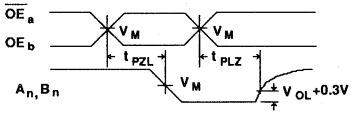
Waveform 1. Propagation Delay Data To Outpout for 'F1242



Waveform 2. Propagation Delay Data To Outpout for 'F1243



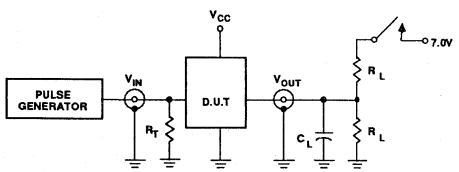
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

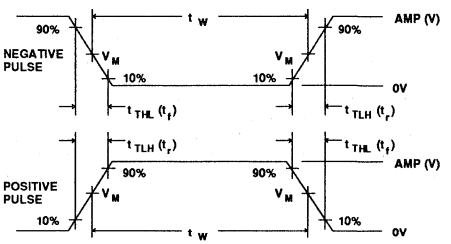
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0041
ECN No.	96221
Date of issue	April 4, 1989
Status	Product Specification
FAST Products	

FAST 74F1244
Buffer

74F1244 Octal Buffer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1244	4.5ns	43mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Low power, light loading**
- **Functional pin for pin equivalent of 'F244**
- **1/30th the bus loading of 'F244**
- **Provides ideal interface and increase fan-out of MOS Microprocessors**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA and source 15mA**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F1244N
20-Pin Plastic SOL	N74F1244D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_a$, $\overline{OE}_b$	Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
Y_{an}, Y_{bn}	Data outputs	750/106.7	15mA/64mA

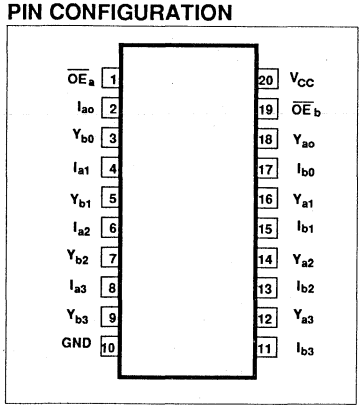
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

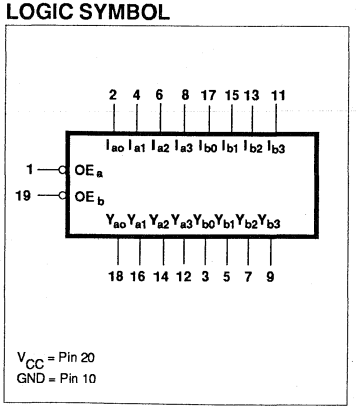
The 74F1244 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_a$ and $\overline{OE}_b$, each controlling four of the 3-state outputs.

The 'F1244 is pin and functional compatible with the 'F244. The lower power and light bus loading features make it an ideal part to interface directly with MOS Microprocessors.

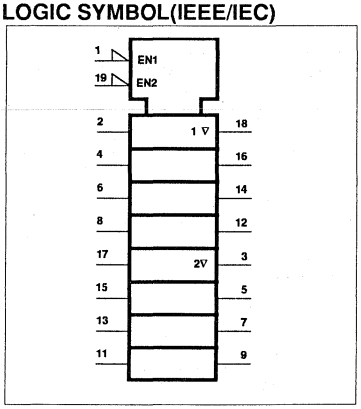
PIN CONFIGURATION



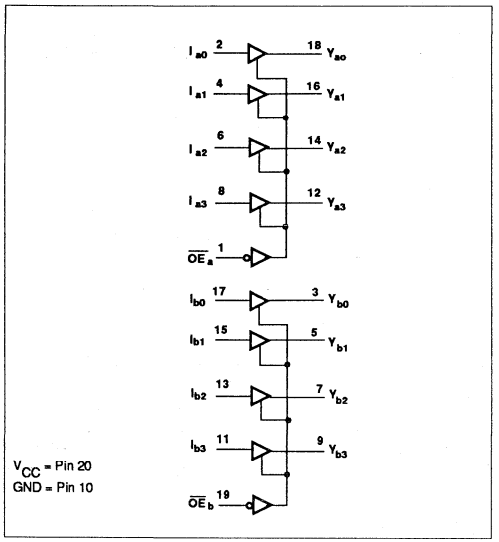
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

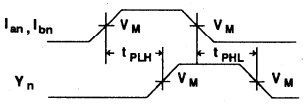
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				30	40	mA
		I_{CCL}					57	75	mA
		I_{CCZ}					43	58	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

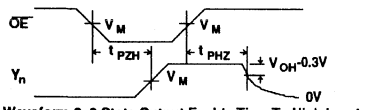
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	Waveform 1	2.5 2.0	4.0 5.0	5.5 7.0	2.5 2.0	6.0 7.5	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	3.0 3.0	6.0 6.5	7.5 8.0	3.0 3.0	8.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	2.0 2.0	4.0 4.0	5.5 5.5	2.0 2.0	6.0 6.0	ns ns

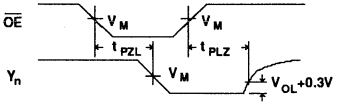
AC WAVEFORMS



Waveform 1. For Non-Inverting Outputs



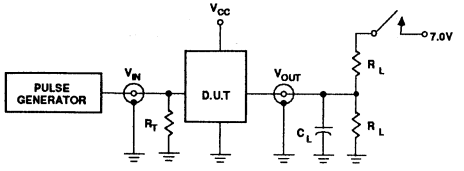
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

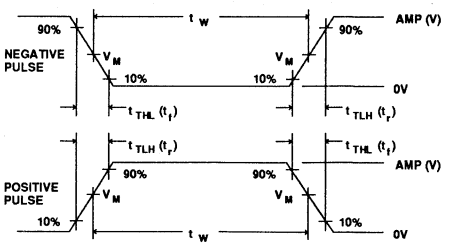
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

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Date of issue	April 4, 1989
Status	Product Specification
FAST Products	

FAST 74F1245 Transceiver

Octal Transceiver (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1245	5.0ns	115mA

FEATURES

- **Same function and pinout as 74F245**
- **High impedance NPN base inputs for reduced loading (70μA in Low and High states)**
- **Useful in applications where light loading bus loading or direct interface with output of a MOS microprocessor is desired**
- **Octal bidirectional bus interface**
- **Glitch free during 3-state power up and power down**
- **3-state buffer outputs sink 64mA and source 15mA**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F1245N
20-Pin Plastic SOL[1]	N74F1245D

NOTE:
1.Thermal mounting technique are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

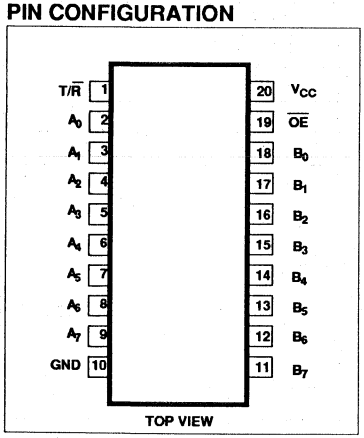
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	A and B port inputs	3.5/0.117	70μA/70μA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.033	40μA/20μA
T/$\overline{R}$	Transmit/Receive input	2.0/0.033	40μA/20μA
A_0- A_7	A port outputs	150/40	3.0mA/24mA
B_0- B_7	B Port outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

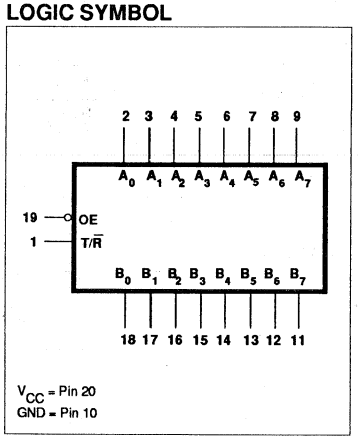
DESCRIPTION

The 74F1245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics.The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive(T/$\overline{R}$) input for direction control. The 3-state outputs, B_0- B_7, have been designed to prevent output bus loading if the power is removed from the device.

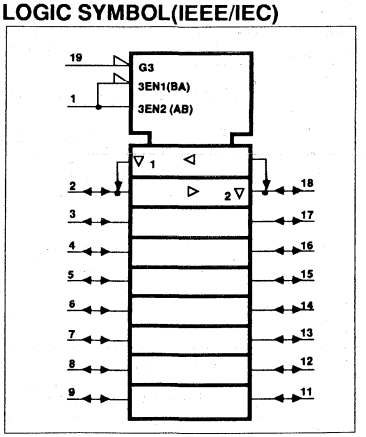
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

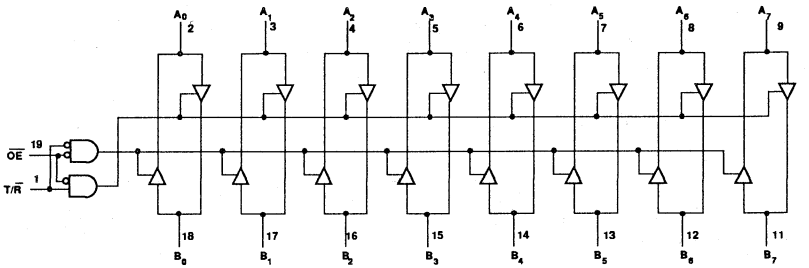


FUNCTION TABLE

INTPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A=B	INPUTS
L	H	INPUTS	B=A
H	X	Z	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



V_{CC}=pin 20
GND=pin 10

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.30	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				120	155	mA
		I_{CCL}					116	150	mA
		I_{CCZ}					110	165	mA

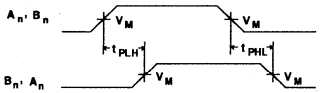
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

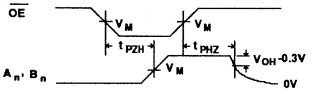
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.0 2.5	4.0 5.0	6.5 7.5	1.5 2.0	7.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 2 Waveform 3	3.0 4.0	6.0 7.5	8.0 10.0	2.5 3.5	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 2 Waveform 3	2.0 4.0	5.0 7.0	8.0 10.0	1.5 4.0	9.0 11.0	ns

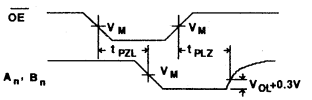
AC WAVEFORMS



Waveform 1. Propagation Delay For Non-Inverting Output



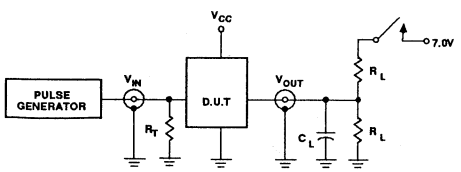
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

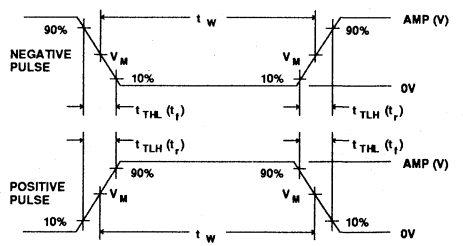
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Latch — FAST 74F1604

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in high and low state)
- Stores 16–bit wide data inputs, multiplexed 8–bit outputs
- Propagation delay 7.0ns typical
- Power supply current 70mA typical

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F1604	7.0ns	70mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
28–pin plastic DIP	N74F1604N
28–pin plastic SOL	N74F1604D

DESCRIPTION

The 74F1604 is a dual octal transparent latch. Organized as 8–bit A and B latches, the latch outputs are connected by pairs to eight 2–input multiplexers. A select (SELECT A/$\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight outputs. Data from the B inputs are selected when SELECT A/$\overline{B}$ is low; data from the A inputs are selected when SELECT A/$\overline{B}$ is high. Data enters the latch on the falling edge of the latch enable ($\overline{LE}$) input. The latch remains transparent to the data inputs while $\overline{LE}$ is low, and stores the data that is present one setup time before the low–to–high latch enable transition.

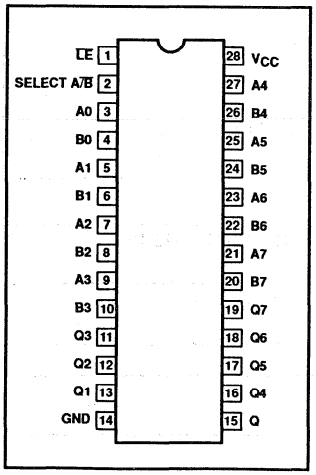
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	Data inputs	1.0/0.033	20μA/20μA
B0 – B7	Data inputs	1.0/0.033	20μA/20μA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20μA/20μA
$\overline{LE}$	Latch enable input (active low)	1.0/0.033	20μA/20μA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

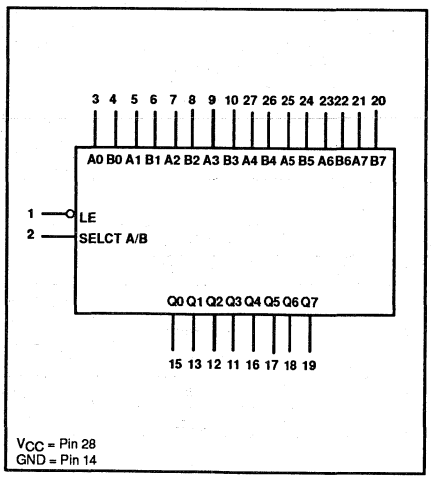
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

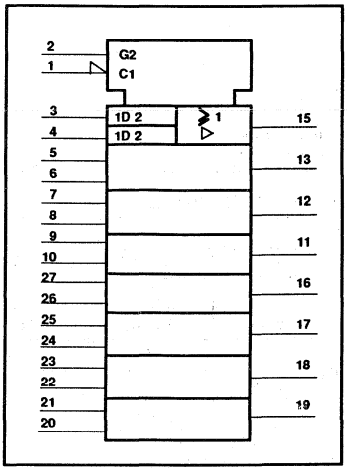
PIN CONFIGURATION



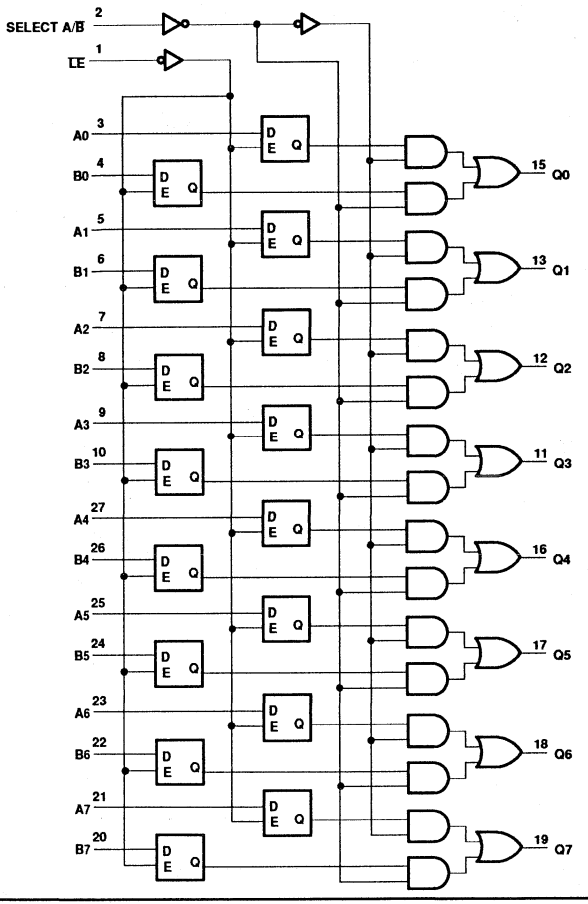
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS19				OUTPUTS	OPERATING MODE
A0 – A7	B0 –B7	SELECT A/B	$\overline{LE}$	Q0 – Q7	
A data	B data	L	L	B data	Enable and read register
A data	B data	H	L	A data	
X	X	X	H	NC	Hold
A data	B data	l	↑	B data	Latch and read register
A data	B data	h	↑	A data	

Notes to function table

1. H = High–voltage level
2. h = High–voltage level one setup time before the low–to–high latch enable transition
3. L = Low–voltage level
4. l = Low–voltage level one setup time before the low–to–high latch enable transition
5. NC= No change (If SELECT A/B is toggled and the A latched data is different from B latched data then the output will change accordingly.)
6. X = Don't care
7. ↑ = Low–to–high latch enable transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				60	80	mA
		I_{CCL}					75	100	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

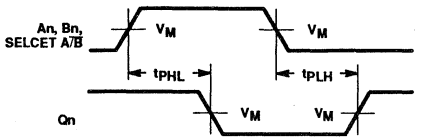
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Qn (non–inverting)	Waveform 2	3.0 3.5	5.5 6.5	8.5 10.0	2.5 3.0	9.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Qn (inverting)	Waveform 1	4.0 2.5	7.0 4.5	10.5 7.5	3.5 2.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to Qn	Waveform 3	6.5 6.0	9.5 9.0	13.0 12.5	5.5 5.0	15.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Qn	Waveform 1, 2	4.0 4.0	6.5 7.0	9.5 10.5	3.5 3.5	10.5 12.5	ns

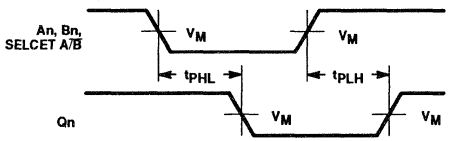
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_D = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_D= 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An, Bn to $\overline{CE}$	Waveform 4	0.0 1.0			0.0 3.5		ns
t_h (H) t_h (L)	Hold time, high or low An, Bn to $\overline{CE}$	Waveform 4	1.5 3.0			2.0 3.5		ns
t_w (L)	$\overline{CE}$ Pulse width, low	Waveform 4	6.5			7.5		ns

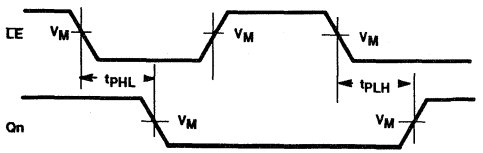
AC WAVEFORMS



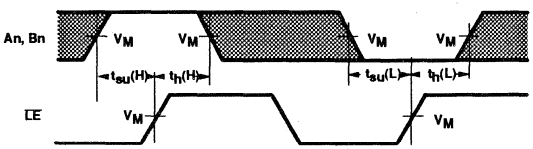
Waveform 1. Propagation delay for SELECT A/$\overline{B}$ to output (A register stored data = low) or An. Bn to output



Waveform 2. Propagation delay for SELECT A/$\overline{B}$ to output (A register stored data = low) or An. Bn to output



Waveform 3. Propagation delay for latch enable to output

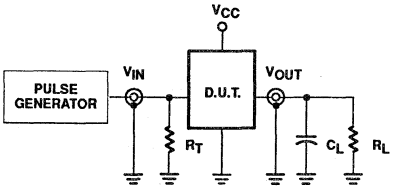


Waveform 4. Setup time and hold times and $\overline{CE}$ pulse width

Note to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



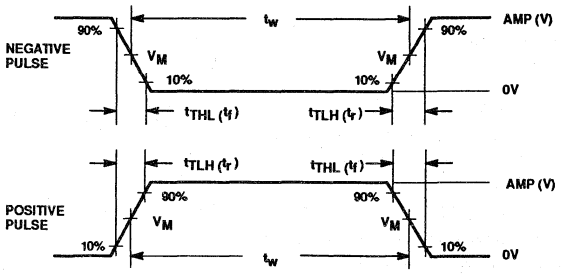
Test circuit for totem-pole outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	v_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

FAST 74F1762
Memory Address Multiplexer

Product Specification

Fast Products

FEATURES

- **Provides refresh and multiplexed row and column addresses for DRAMs**
- **Addressing up to 4MBit DRAMs**
- **Compatible with 74F1761 DIVC and other DRAM controllers**
- **High-performance outputs**
- **High-speed address multiplexing**
- **On-chip 11-bit refresh counter**

TYPE	TYPICAL DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F1762	5.3ns	90mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
Plastic DIP	N74F1762N
PLCC 44	N74F1762A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
RA_0 - RA_{10}	Row address inputs	1.0/1.0	20µA/0.6mA
CA_0 - CA_{10}	Column address inputs	1.0/1.0	20µA/0.6mA
$\overline{MA}_0$ - $\overline{MA}_{10}$	DRAM address outputs	N/A	15mA/20mA
$\overline{REFEN}$	Refresh enable input	1.0/1.0	20µA/0.6mA
MUX	Row/column select input	1.0/1.0	20µA/0.6mA
COUNT	Refresh address count input	1.0/1.0	20µA/0.6mA
MR	Refresh counter reset input	1.0/1.0	20µA/0.6mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state. FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

PRODUCT DESCRIPTION:

The Signetics Memory Address Multiplexer is designed for use in very high performance dynamic RAM applications. In addition to multiplexing row and column addresses, the device also generates and multiplexes refresh addresses. Though specifically designed to be used with the 74F1761, DRAM and Interrupt Vector Controller, it may be used with any other custom or standard DRAM timing controller chip.

The 'F1762 contains 22 address inputs (RA_0 - RA_{10}) and (CA_0 - CA_{10}), an 11-bit refresh counter, and eleven 3-to-1 multiplexers. The multiplexed row, column or refresh address is output on the eleven high-performance outputs ($\overline{MA}_0$ - $\overline{MA}_{10}$). This enables direct addressing of up to 4MBit dynamic RAMs. Combined with the 'F1761, the 'F1762 provides a complete 4MBit DRAM and interrupt control solution. This solution can control dynamic RAMs with access times down to 40ns.

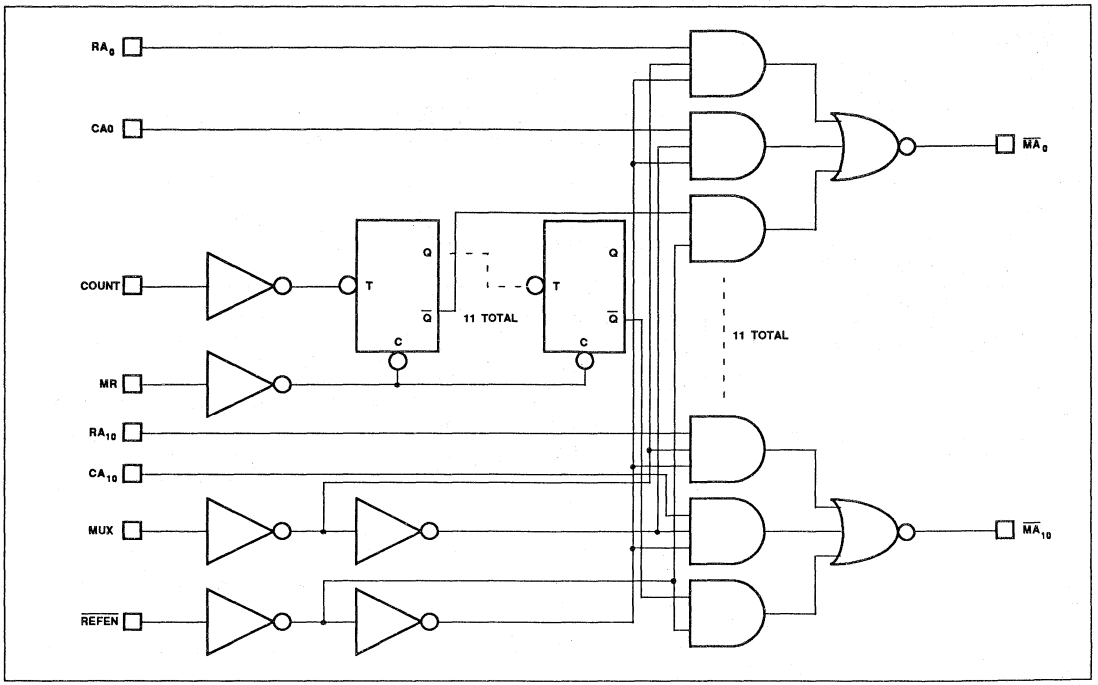
FUNCTIONAL DESCRIPTION:

Functionally, the 'F1762 Memory Address Multiplexer is quite simple. Referring to the logic diagram, the 11-bit Refresh Counter is controlled by the COUNT input, which increments the value stored in the refresh counter on every Low to High transition. When the 'F1762 is used with the 'F1761, this pin is usually connected to the $\overline{REFEN}$ input, so that at the end of every refresh cycle, the refresh counter will be incremented. The Master Reset (MR) input clears the contents of the refresh counter, and may be used for diagnostic testing or initializing after power-up. The eleven 3-to-1 multiplexers are controlled by the MUX and $\overline{REFEN}$ inputs. When $\overline{REFEN}$ is asserted, regardless of the state of the MUX signal, the contents of the internal refresh counter are inverted and asserted at the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs. When $\overline{REFEN}$ is negated, the MUX signal controls which set of address inputs will be propagated to the outputs. With MUX Low, the Row Address inputs (RA_0 - RA_{10}) will be inverted and asserted at the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs. When MUX is High, the Column Addresses (CA_0 - CA_{10}) will be correspondingly asserted.

The $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs have specialized drivers to switch 70 ohm transmission lines (typical of DRAM arrays) on the incident edge, thus improving overall system performance. For more information on the driving characteristics, please refer to the DC electrical characteristics and also Signetics application note number AN218.

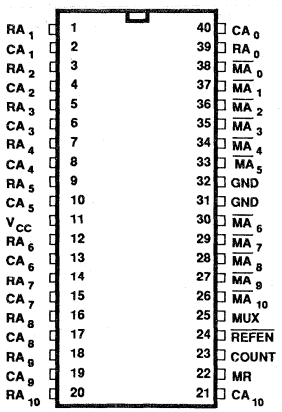
Memory Address Multiplexer FAST 74F1762

LOGIC DIAGRAM

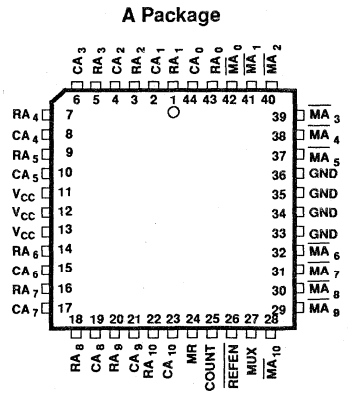


PIN CONFIGURATION

N Package



A Package



Memory Address Multiplexer | FAST 74F1762

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
RA_0 - RA_{10}	39, 1, 3, 5, 7, 9, 12, 14, 16, 18, 20	43, 1, 3, 5, 7, 9, 14, 16, 18, 20, 22	I	Row Address Inputs. When $\overline{REFEN}$ is negated and MUX is Low, these inputs are inverted and propogated to the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
CA_0 - CA_{10}	40, 2, 4, 6, 8, 10, 13, 15, 17, 19, 21	44, 2, 4, 6, 8, 10, 15, 17, 19, 21, 23	I	Column Address Inputs. When $\overline{REFEN}$ is negated and MUX is High, these inputs are inverted and propogated to the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
$\overline{MA}_0$ - $\overline{MA}_{10}$	38, 37, 36, 35, 34, 33, 30, 29, 28, 27, 26	42, 41, 40, 39, 38, 37, 32, 31, 30, 29, 28	O	Active Low Memory Address Outputs. These outputs contain the address from either the internal refresh counter, the Row Address inputs, or the Column Address inputs depending on the state of the $\overline{REFEN}$ and MUX signal inputs.
$\overline{REFEN}$	24	26	I	Active Low Refresh Enable Input. When asserted, the address contained in the internal refresh counter is asserted on the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
MUX	25	27	I	Row / Column Address Multiplex Input. If $\overline{REFEN}$ is High, this signal will multiplex the inverted Row or Column address inputs on the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs when it is asserted Low or High respectively.
COUNT	23	25	I	Refresh Counter Count Clock Input. A Low to High transition on this input will increment the internal refresh counter by one regardless of the state of $\overline{REFEN}$ input.
MR	22	24	I	Active High Refresh Counter Master Reset Input. A High level on this input will reset the internal refresh counter to all zeros.
V_{CC}	11	11, 12, 13		+5V ± 10% Supply input.
GND	31, 32	33, 34, 35, 36		Ground.

FUNCTION TABLE

INPUTS						OUTPUTS	COUNTER
MR	COUNT	MUX	$\overline{REFEN}$	RA_n	CA_n	$\overline{MA}_n$	COUNTER CONTENTS
H	X	X	X	X	X	UN*	Reset to 0
L	↑	X	X	X	X	UN*	Increment by 1
H	X	X	L	X	X	L	Reset to 0
L	X	X	L	X	X	COUNTER CONTENTS	Unchanged
L	X	L	H	L	X	H	Unchanged
L	X	L	H	H	X	L	Unchanged
L	X	H	H	X	L	H	Unchanged
L	X	H	H	X	H	L	Unchanged

*The state of the outputs is dependant on the state of the MUX and $\overline{REFEN}$ inputs. The Counter is reset any time MR is High, and if MR is Low, it is incremented on every low to high transistion of COUNT.

UN = Unspecified
H = High level voltage
L = Low level voltage
X = Don't care
↑ = Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage[3]		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5	3.2		V
					±5%V_{CC}	2.7	3.4		V
				I_{OH2} = -35mA	±5%V_{CC}	2.4			V
V_{OL}	Low-level output voltage[4]		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.5	V
					±5%V_{CC}		0.35	0.5	V
				I_{OL2} = 60mA	±5%V_{CC}		0.45	0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Low-level output voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{IO}[5]	Output current		V_{CC} = MAX, V_{OUT} = 2.25V			-30		-120	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	80	mA
		I_{CCL}					90	120	mA

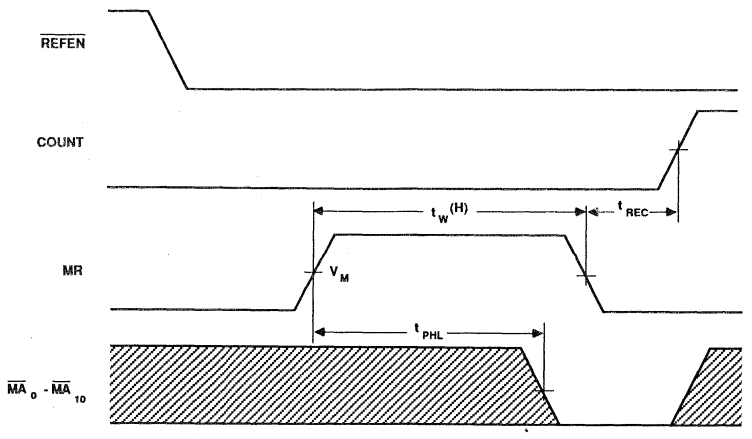
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a Low-to-High transition in a 70Ω transmission line.
4. I_{OL2} is the current necessary to guarntee a High-to-Low transition in a 70Ω transmission line.
5. The output conditions have been chosen to produce a current that closely approximates one-half of the short circuit current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, MUX(↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$, (column address) valid	Waveform 1	2.0 2.5	4.5 5.0	7.5 8.0	2.0 2.5	8.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay, MUX(↓) to $\overline{MA}_0$ - $\overline{MA}_{10}$, (row address) valid	Waveform 3	4.0 2.0	6.5 4.5	9.5 7.5	3.0 2.0	10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{REFEN}$ (↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$		2.0 2.0	4.3 4.5	7.5 8.0	2.0 2.0	8.5 11.0	ns
t_{PLH} t_{PHL}	$\overline{REFEN}$ (↓) to $\overline{MA}_0$ - $\overline{MA}_{10}$ (refresh address) valid	Waveform 2	4.0 2.0	6.9 4.7	10.5 7.5	3.5 2.0	11.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay, RA_0 - RA_{10} to $\overline{MA}_0$ - $\overline{MA}_{10}$	Waveform 4	1.0 0.5	3.0 2.2	6.0 5.0	1.0 0.5	6.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay, CA_0 - CA_{10} to $\overline{MA}_0$ - $\overline{MA}_{10}$	Waveform 5	1.0 0.5	3.0 2.2	6.0 5.0	1.0 0.5	6.5 5.5	ns
t_{PLH} t_{PHL}	COUNT (↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$ (refresh address) valid	Waveform 2	2.0	15.0	35.0	2.0	40.0	ns
t_{PHL}	Propagation delay, MR(↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$	Waveform 1	3.0	5.8	10.5	2.5	11.0	ns
t_w(H)	COUNT pulse width, High	Waveform 2	5.0			5.0		ns
t_w(L)	COUNT pulse width, Low	Waveform 2	5.0			5.0		ns
t_w(H)	MR Pulse width	Waveform 1	5.0			5.0		ns
t_{rec}	Recovery time, MR (↓) to COUNT (↑)	Waveform 1	5.0			5.0		ns

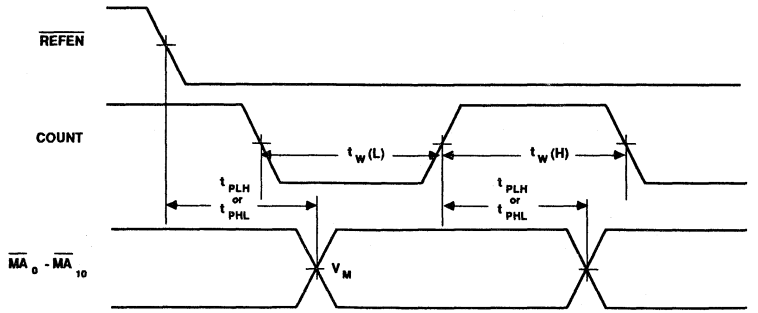
AC WAVEFORMS



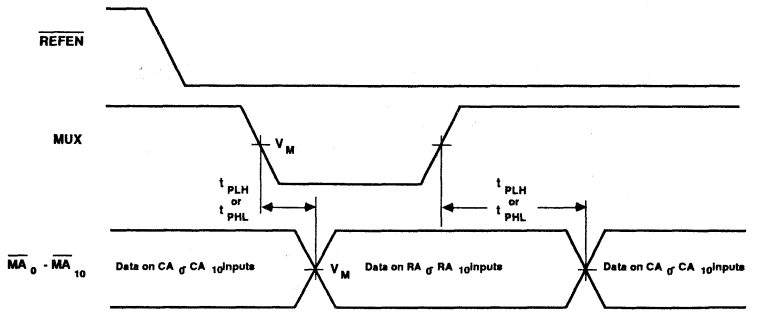
Waveform 1. Waveforms Showing Master Reset Timing

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

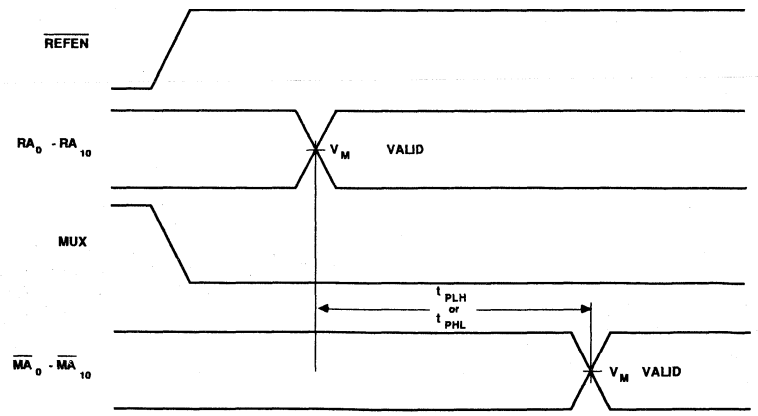
AC WAVEFORMS



Waveform 2. Waveforms Showing Refresh Timing



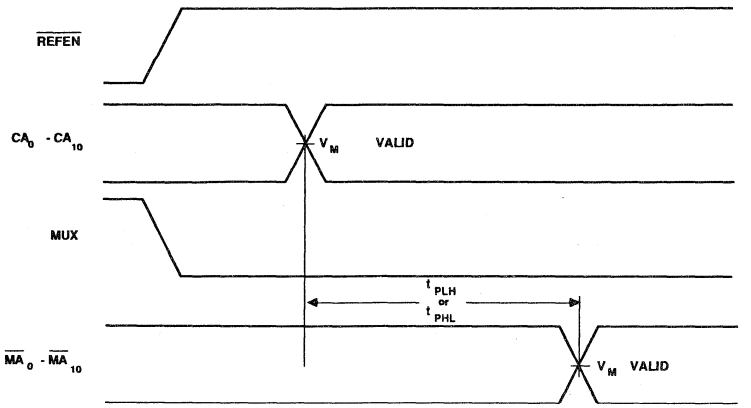
Waveform 3. Waveforms Showing Address Multiplexing Timing



Waveform 4. Waveforms Showing RA_0 - RA_{10} to $\underline{MA}_0$ - to $\underline{MA}_{10}$ Propagation Delay

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

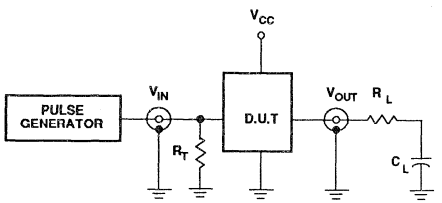
AC WAVEFORMS



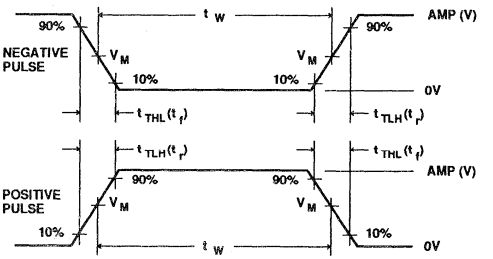
Waveform 5. Waveforms Showing CA_0 - CA_{10} to $\overline{MA}_0$ - $\overline{MA}_{10}$ Propagation Delay

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

Document No.	853-1406
ECN No.	98150
Date of issue	November 17, 1989
Status	Product Specification`
FAST Products	

FAST 74F1763 Intelligent DRAM Controller (IDC)

TYPE	f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1763	100 MHz	150 mA

FEATURES

- **DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Selectable row address hold and $\overline{RAS}$ precharge times**
- **Facilitates page mode accesses**
- **Controls 1 MBit DRAMs**
- **Intelligent burst-mode refresh after page-mode access cycles**

PRODUCT DESCRIPTION

The Signetics Intelligent Dynamic RAM Controller is a 1 MBit, single-port version of the 74F1764 Dual Port Dynamic RAM Controller. It contains automatic signal timing, address multiplexing and refresh control required for interfacing with dynamic RAMs. Additional features have been added to this device to take advantage of technological advances in Dynamic RAMs. A Page-Mode access pin allows the user to assert $\overline{RAS}$ for the entire access cycle rather than the predefined four-clock-cycle pulse width used for normal random access cycles. In addition, the user has the ability to select the $\overline{RAS}$ precharge time and Row-Address Hold time to fit the particular DRAMs being used. $\overline{DTACK}$ has been modified from previous family parts to become a negative true, tri-stated output. The options for latched or unlatched address are contained on a single device by the addition of an Address Latch Enable ($\overline{ALE}$) input. Finally, a burst refresh monitor has been added to ensure complete refreshing after lengthy page-mode access cycles. With a maximum clock frequency of 100 MHz, the F1763 is capable of controlling DRAM arrays with access times down to 40 nsec.

ORDERING INFORMATION

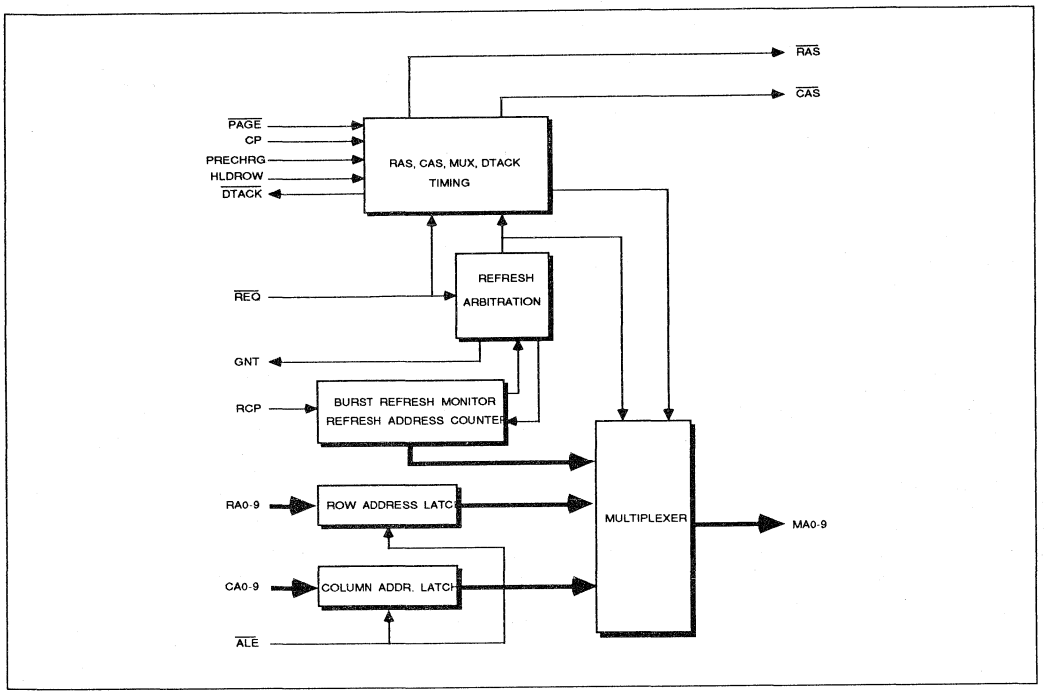
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A=0°C to 70°C
48-Pin Plastic DIP	N74F1763N
44-Pin PLCC	N74F1763A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

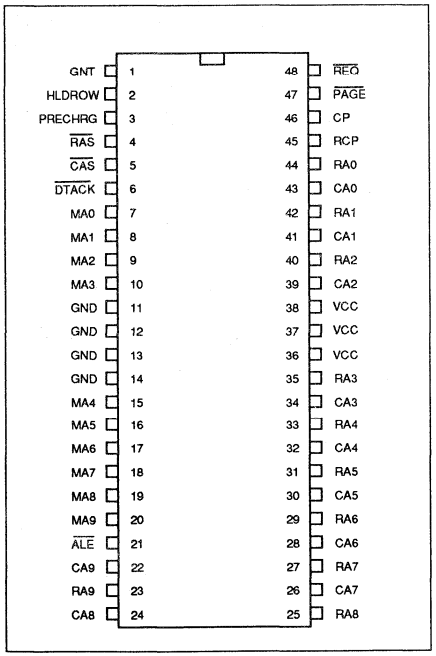
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ}$	DRAM Request Input	1.0/1.0	20 µA/0.6 mA
CP	Clock Input	1.0/1.0	20 µA/0.6 mA
$\overline{PAGE}$	Page Mode Select Input	1.0/1.0	20 µA/0.6 mA
PRECHRG	$\overline{RAS}$ Precharge Select Input	1.0/1.0	20 µA/0.6 mA
HLDROW	Row Hold Select Input	1.0/1.0	20 µA/0.6 mA
$\overline{DTACK}$	Data Transfer Ack. Output	50/80	35 mA/60 mA
GNT	Access Grant Output	50/80	35 mA/60 mA
RCP	Refresh Clock Input	1.0/1.0	20 µA/0.6 mA
RA0-9	Row Address Inputs	1.0/1.0	20 µA/0.6 mA
CA0-9	Column Address Inputs	1.0/1.0	20 µA/0.6 mA
$\overline{ALE}$	Address Latch Enable Input	1.0/1.0	20 µA/0.6 mA
$\overline{RAS}$	Row Address Strobe Output	N/A*	35 mA/60 mA
$\overline{CAS}$	Column Address Strobe Output	N/A*	35 mA/60 mA
MA0-9	DRAM Address Outputs	N/A*	35 mA/60 mA

NOTE:
One (1.0) FAST Unit Load is defined as 20 uA in the HIGH state and 0.6 mA in the LOW state.
* FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

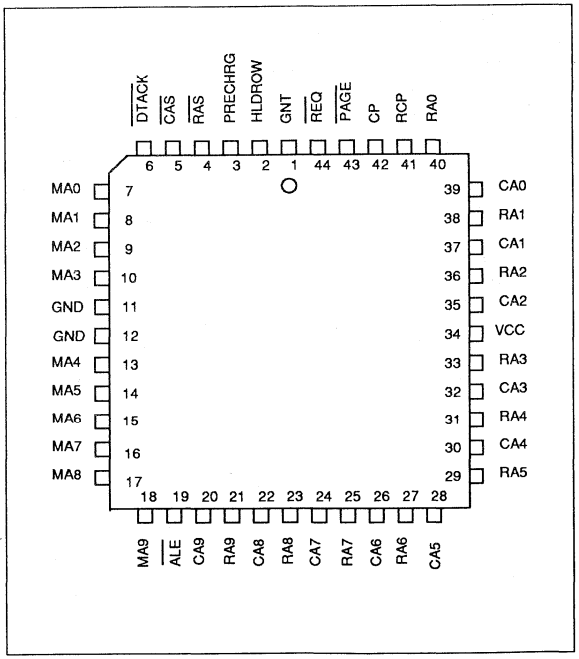
BLOCK DIAGRAM



DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
$\overline{REQ}$	48	44	Input	Active Low Memory Access Request input, must be asserted for the entire DRAM access cycle. $\overline{REQ}$ is sampled on the rising edge of the CP clock.
GNT	1	1	Input	Active High Grant output. When High indicates that a DRAM access (inactive during refresh) cycle has begun. Asserted from the rising edge of the CP clock.
$\overline{PAGE}$	47	43	Input	Active Low Page-Mode Access input. Forces the IDC to keep $\overline{RAS}$ asserted for as long as the $\overline{PAGE}$ input is Low and $\overline{REQ}$ is asserted Low.
HLDROW	2	2	Input	Row Address Hold input. If Low will configure the IDC to maintain the row addresses for a full CP clock cycle after $\overline{RAS}$ is asserted. If High will program the IDC to maintain row addresses for a 1/2 CP clock cycle after $\overline{RAS}$ is asserted.
PRECHRG	3	3	Input	$\overline{RAS}$ Precharge input. A Low will program the IDC to guarantee a minimum of 4 CP clock cycles of precharge. A High will guarantee 3 clock cycles of precharge.
CP	46	42	Input	Clock input. Used by the Controller for all timing and arbitration functions.
RCP	45	41	Input	Refresh Clock input. Divided internally by 64 to produce an internal Refresh Request.
$\overline{DTACK}$	6	6	Output	Active Low, 3-state Data Transfer Acknowledge output. Enabled by the $\overline{REQ}$ input and asserted four clock cycles after the assertion of $\overline{RAS}$. 3-stated when $\overline{REQ}$ goes High.
RA0-9	44,42, 40,35, 33,31, 29,27, 25,23	40, 38, 36, 33, 31, 29, 27, 25, 23, 21	Inputs	Row Address inputs.
CA0-9	43,41, 39,34, 32,30, 28,26, 24,22	39, 37, 35, 32, 30, 28, 26, 24, 22, 20	Inputs	Column Address inputs. Propagated to the MA0-9 outputs 1 CP clock cycle after $\overline{RAS}$ is asserted, if HLDROW=0 or 1/2 clock cycle later if HLDROW is 1.
$\overline{RAS}$	4	4	Output	Active Low Row Address Strobe. Asserted for four clock cycles during each refresh cycle regardless of the $\overline{PAGE}$ input. Also asserted for four clock cycles during processor access if the $\overline{PAGE}$ input is High. If $\overline{PAGE}$ is Low, $\overline{RAS}$ is negated upon negation of $\overline{PAGE}$ or $\overline{REQ}$, whichever occurs first.
$\overline{CAS}$	5	5	Output	Active Low Column Address Strobe. Always asserted 1.5 CP clock cycles after the assertion of $\overline{RAS}$. Negated upon negation of $\overline{REQ}$. HLDROW input pin does not affect $\overline{RAS}$ to $\overline{CAS}$ timing.
MA0-9	7-10, 15-20	7-10, 13-18	Output	DRAM multiplexed address outputs. Row and column addresses asserted on these pins during an access cycle. Refresh counter addresses presented on these outputs during refresh cycles.
$\overline{ALE}$	21	19	Input	Active Low Address Latch Enable input. A Low on this pin will cause the address latches to be transparent. A High level will latch the RA0-9 & CA0-9 inputs.
V_{CC}	36-38	34		+5 V ± 10% Supply voltage.
GND	11-14	11, 12		Ground

FUNCTIONAL DESCRIPTION

The 74F1763 1 Megabit Intelligent DRAM Controller (IDC) is a synchronous device with most signal timing being a function of the CP input clock.

Arbitration:

Once the DRAM's $\overline{RAS}$ precharge time has been satisfied, the $\overline{REQ}$ input is sampled on each rising edge of the CP clock and an internally generated refresh request is sampled on each falling edge of the same clock. When only one of these requests is sampled as active the appropriate memory cycle will begin immediately. For a memory access cycle this will be indicated by GNT and $\overline{RAS}$ outputs both being asserted and for a refresh cycle by multiplexing refresh address to the MA0-9 outputs and subsequent assertion of $\overline{RAS}$ after 1/2CP clock cycle. If both memory access and refresh requests are active at a given time the request sampled first will begin immediately and the other request (if still asserted) will be serviced upon completion of the current cycle and it's associated $\overline{RAS}$ precharge time.

Memory access:

The row (RA0-9) and column (CA0-9) address inputs are latched when $\overline{ALE}$ input is High. When $\overline{ALE}$ is Low the input addresses propagate directly to the outputs. When GNT and RAS are asserted , after a $\overline{REQ}$ has been sampled the RA0-9 address inputs will have already propagated to the MA0-9 outputs for the row address. One or one-half CP clock cycles later (depending on the state of the HLDROW input) the column address (CA0-9) inputs are propagated to the MA0-9 outputs. $\overline{CAS}$ is always asserted one and one-half CP clock cycles after $\overline{RAS}$ is asserted. If the $\overline{PAGE}$ input is High, $\overline{RAS}$ will be negated approximately four CP clock cycles after its initial assertion. At this time the $\overline{DTACK}$ output becomes valid indicating the completion of a memory access cycle. The IDC will maintain the state of all its outputs untill the $\overline{REQ}$ input is negated (see timing waveforms).

Row address hold times:

If the HLDROW input of the IDC is High the row address outputs will remain valid 1/2 CP clock cycle after $\overline{RAS}$ is asserted. If the HLDROW input is Low the row address outputs will remain valid one CP clock cycle after $\overline{RAS}$ is asserted.

$\overline{RAS}$ precharge timing:

In order to meet the $\overline{RAS}$ precharge requirement of dynamic RAMs, the controller will hold-off a subsequent $\overline{RAS}$ signal assertion due to a processor access request or a refresh cycle for four or three full CP clock cycles from the previous negation of $\overline{RAS}$, depending on the state of the PRECHRG input. If the PRECHRG input is Low, $\overline{RAS}$ remains High for at least 4 CP clock cycles. If the PRECHRG input is High $\overline{RAS}$ remains High for at least 3 CP clock cycles.

Refresh timing:

The refresh address counter wakes-up in an all 1's state and is an up counter. The refresh clock (RCP) is internally divided down by 64 to produce an internal refresh request. This refresh request is recognized either immediately or at the end of a running memory access cycle. Due to the possibility that page mode access cycles may be lengthy, the controller keeps track of how many refresh requests have been missed by logging them internally (up to 128) and servicing any pending refresh requests at the end of the memory access cycle. The controller performs $\overline{RAS}$-only refresh cycles until all pending refresh requests are depleted.

Page-mode access:

Fast accesses to consecutive locations of DRAM can be realized by asserting the $\overline{PAGE}$ input as shown in the timing waveforms. In this mode, the controller does not automatically negate $\overline{RAS}$ after four CP clock cycles, but keeps it asserted throughout the access cycle. By using external gates, the $\overline{CAS}$ output can be gated on and off while changing the column address inputs to the controller, which will propogate to the MA_0- MA_9 address outputs and provide a new column address. This is only useful if the $\overline{ALE}$ input is Low, enabling the user to change addresses. This mode can be used with DRAMs that support page or nibble mode addressing.

Output driving characteristics:

Considering the transmission line characteristic of the DRAM arrays, the outputs of the IDC have been designed to provide incident-edge switching (in Dual-Inline-Packaged memory arrays), needed in high performance systems. For more information on the driving characteristics, please refer to Signetics application note number AN218. The driving characteristics of the 74F1763 are the same as those of the 74F765 shown in the application note.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current[1]			-15	mA
I_{OL}	Low-level output current[1]			24	mA
T_A	Operating free-air temperature range	0		70	°C

NOTE:
1. Transient currents will exceed these values in actual operation.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH2}[3] = -35mA	±5%V_{CC}	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
			I_{OL2}[4] = 60mA	±5%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage	V_{CC}= MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Output current[5]	V_{CC} = MAX, V_O= 2.25V			-100		-225	mA
I_{CC}	Supply current (total)	V_{CC}= MAX					220	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{cc} = 5V, T_A = 25°C.
3. I_{OH2} is transient current necessary to guarantee a Low to High transition in a 70Ω transmission line.
4. I_{OL2} is transient current necessary to guarantee a High to Low transition in a 70Ω transmission line.
5. Not more than one output should be shorted at a time. For testing I_{os}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=25°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
1	CP clock period (tcp)		10			10		ns
2	CP clock low time		5			5		ns
3	CP clock high time		5			5		ns
4	RCP clock period		100			100		ns
5	RCP clock low time		10			10		ns
6	RCP clock high time		10			10		ns
7	Setup time $\overline{REQ}$(↓) to CP(↑)		4	2		4		ns
8	$\overline{REQ}$ High hold time after CP(↑) **(Note 1)**		0			0		ns
9	$\overline{REQ}$ High pulse width **(Note 2)**		1/2tcp+5	1/2tcp+5	1/2tcp+5	1/2tcp+5	1/2tcp+5	ns
10	Propagation delay CP(↑) to GNT High		8.5	11	13.5	8.5	15.5	ns
11	Propagation delay $\overline{REQ}$(↑) to GNT Low		8.5	10.5	13	8.5	14	ns
12	$\overline{ALE}$ pulse width Low		4	1		4		ns
13	RA0-9,CA0-9 High or Low setup to $\overline{ALE}$(↑)		2	0		2		ns
14	$\overline{ALE}$(↑) to RA0-9,CA0-9 High or Low hold		1	0		1		ns
15	Propagation delay RA0-9,CA0-9 High or Low to MA0-9 **(Note 3)**	$\overline{ALE}$ Low	4	7.5	11	4	14	ns
16	Propagation delay $\overline{ALE}$(↓) to MA0-9		5.5	8.5	13	5.5	15	ns
17	Propagation delay CP(↑) to $\overline{RAS}$(↓)		8.5	10.5	12.5	8.5	14	ns
18	$\overline{RAS}$(↓) to MA0-9 (colum address) skew	HLDROW = 1	1/2tcp-2	1/2tcp+2	1/2tcp+5.5	1/2tcp-2.5	1/2tcp+7	ns
19	$\overline{RAS}$(↓) to MA0-9 (column address) skew	HLDROW = 0	1tcp-2	1tcp+2	1tcp+5.5	1tcp-2.5	1tcp+7	ns
20	$\overline{RAS}$(↓) to $\overline{RAS}$(↑) skew	PAGE = 1	4tcp+1.5	4tcp+3.5	4tcp+6	4tcp+1	4tcp+6.5	ns
21	Propagation delay CP(↑) to $\overline{RAS}$(↑)		12	14	16.5	12	18.5	ns
22	Propagation delay $\overline{REQ}$(↑) to $\overline{RAS}$(↑) **(Note 4)**		14.5	17.5	20	14	24	ns
23	Propagation delay CP(↓) to $\overline{CAS}$(↓)		6	8	10	6	11	ns
24	Propagation delay $\overline{PAGE}$(↑) to $\overline{RAS}$(↑) **(Note 4)**		10	12.5	15	10	17	ns
25	$\overline{RAS}$(↓) to $\overline{CAS}$(↓) skew		1.5tcp-4.5	1.5tcp-2.5	1.5tcp-o.5	1.5tcp-5.5	1.5tcp	ns
26	Propagation delay $\overline{REQ}$(↑) to $\overline{CAS}$(↑)		10	12	15	10	17	ns
27	MA0-9 (column address) to $\overline{CAS}$(↓) skew		1tcp-8	1tcp-4	1tcp-0.5	1tcp-9	1tcp-0.5	ns

AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=25°C V_{cc}=+5.0V±10% C_L=300pF RL=70Ω			T_A=0°C to +70°C V_{cc}=+5.0V±10% C_L=300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
28	MA0-9 (column address) to $\overline{CAS}$(↓) skew	HLDROW = 0	1/2tcp-8	1/2tcp-4	1/2tcp-0.5	1/2tcp-9	1/2tcp-0.5	ns
29	Set-up time $\overline{PAGE}$(↓) to CP(↑)		2			2		ns
30	Propagation delay $\overline{REQ}$(↓) to $\overline{DTACK}$(↑)		6	8	11.5	6	12	ns
31	Propagation delay CP(↑) to $\overline{DTACK}$(↓)		7.5	9.5	12	7.5	13	ns
32	Propagation delay $\overline{REQ}$(↑) to $\overline{DTACK}$(3-state)		9	12	13	9	15.5	ns
33	MA0-9 (refresh address) to $\overline{RAS}$(↓) skew		1/2tcp-5			1/2tcp-6.5		ns
34	$\overline{RAS}$(↓) to MA0-9 (refresh addres) skew		1tcp-2			1tcp-2.5		ns
35	$\overline{RAS}$(↑) to RAS(↓) skew (precharge)	PRECHRG = 0	4tcp-6	4tcp-3.5	4tcp-1.5	4tcp-6.5	4tcp-6.5	ns
36	$\overline{RAS}$(↑) to RAS(↓) skew (precharge)	PRECHRG = 1	3tcp-6	3tcp-3.5	3tcp-1.5	3tcp+1	3tcp-6.5	ns

Note1: $\overline{REQ}$ High hold means that, if $\overline{REQ}$ is High at the rising clock edge, it is guaranteed that the $\overline{REQ}$ input was not samples as Low.
Note2: A 50% duty cycle clock is recommended. If the duty cycle of the clock is not 50%, $\overline{REQ}$ should be held high for enough time such that a falling CP clock edge samples $\overline{REQ}$ as High. This is to ensure that refresh cycles don't get locked-up.
Note3: When $\overline{ALE}$ is Low, the address input latches are in the transparant mode and therefore any changes in the address inputs will be propagated to the MA0-9 outputs. Figure 2 illustrates RA0-9 inputs propagating to the MA0-9 outputs, but later in the cycle, if $\overline{ALE}$ is still Low when the CA0-9 inputs are multiplexed to the MA0-9 outputs the CA0-9 inputs will be in the transparant mode.
Note4: If $\overline{PAGE}$ is High and $\overline{REQ}$ is Low, $\overline{RAS}$ is automatically negated after approximately 4 CP clock cycles. If $\overline{PAGE}$ is Low and $\overline{REQ}$ is also Low, $\overline{RAS}$ will be negated when $\overline{PAGE}$ goes High. $\overline{RAS}$ will always be negated when $\overline{REQ}$ goes High regardless of the state of $\overline{PAGE}$ input.

TIMING DIAGRAMS

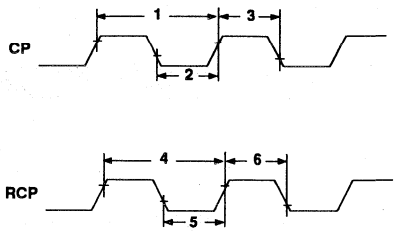


Figure 1: Clock cycle Timing

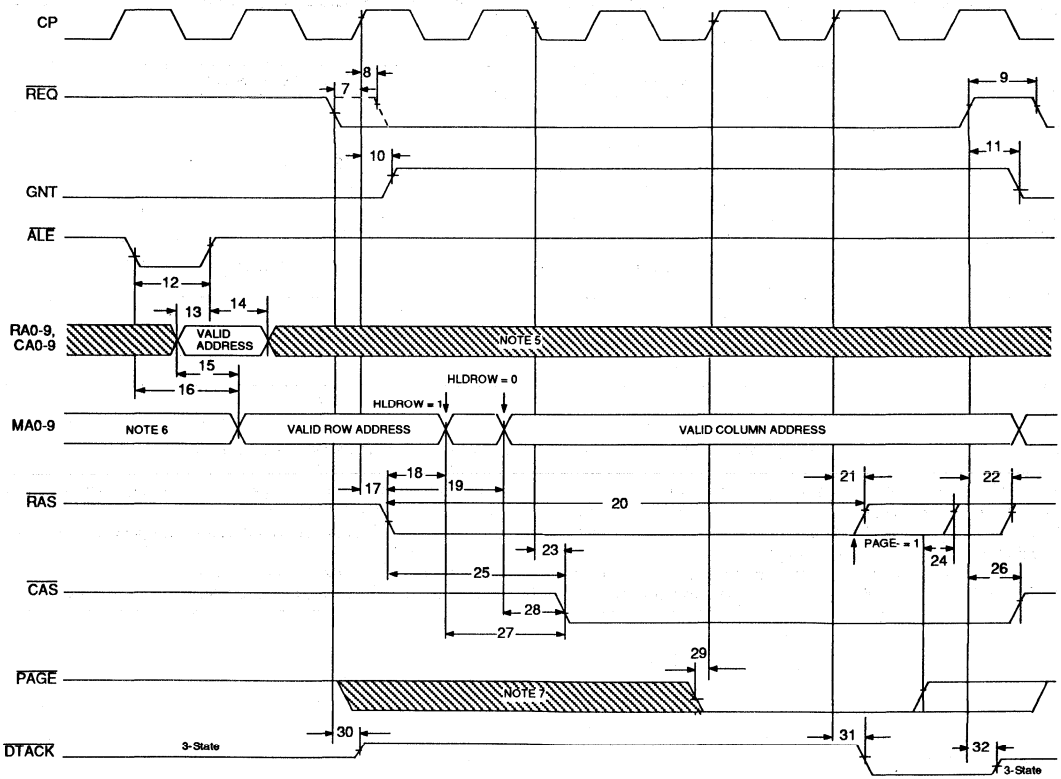


Figure 2: Memory access cycle timing

Note 5: If the RA0-9 & CA0-9 address inputs are not latched,RA0-9 inputs should remain valid until row address hold time is met and CA0-9 inputs should remain valid until column address hold time is met.
Note 6: MA0-9 outputs will contain the present row address on the RA0-RA9 inputs or the last row address latched into the device.
Note 7: $\overline{\text{PAGE}}$ input may be asserted anytime before this rising clock edge inorder to hold $\overline{\text{RAS}}$ Low.

TIMING DIAGRAM

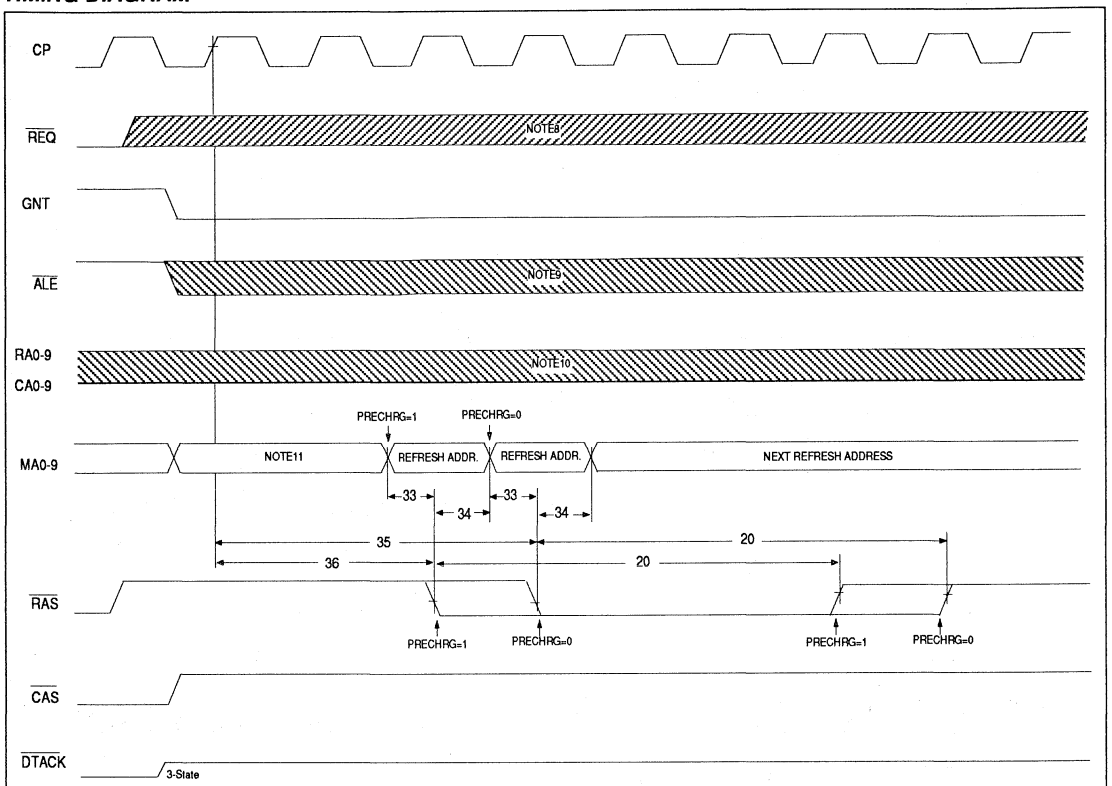


Figure 3: Refresh cycle timing following a memory access cycle

Note 8: $\overline{REQ}$ input is a don't care during a memory refresh cycle. If $\overline{REQ}$ is asserted during a refresh cycle, it will be recognized at the first rising CP clock edge, following the refresh cycle and it's associated $\overline{RAS}$ precharge time (see Figure 4).
Note 9: RA0-9 & CA0-9 address inputs may be latched at anytime during a memory refresh cycle. However, a memory access cycle will not begin until after the completion of the refresh cycle.
Note 10: RA0-9 & CA0-9 if in the transparant mode do not propagate to the MA0-9 outputs during a refresh cycle.
Note 11: MA0-9 outputs will contain the present row address on the RA0-RA9 inputs or the last row address latched into the device.

TIMING DIAGRAM

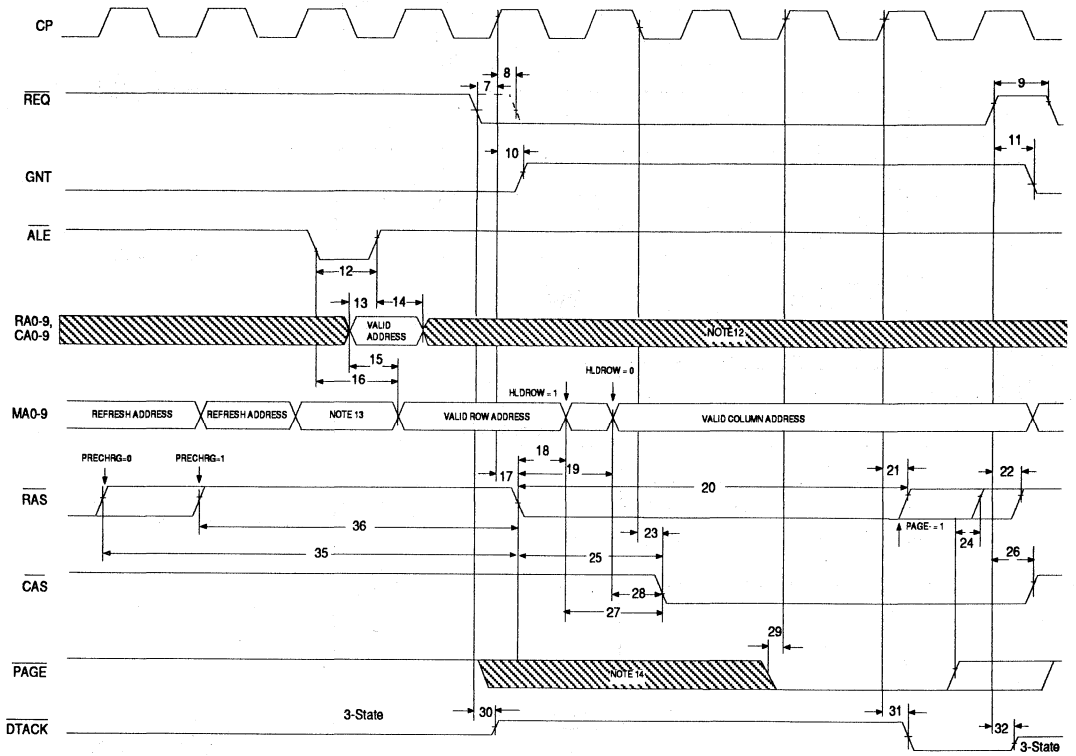


Figure 4: Memory access cycle timing following a refresh cycle

Note 12: If the RA0-9 & CA0-9 address inputs are not latched,RA0-9 inputs should remain valid until row address hold time is met and CA0-9 inputs should remain valid until column address hold time is met.
Note 13: MA0-9 outputs will contain the present row address on the RA0-RA9 inputs or the last row address latched into the device.
Note 14: $\overline{\text{PAGE}}$ input may be asserted anytime before this rising clock edge inorder to hold $\overline{\text{RAS}}$ Low.

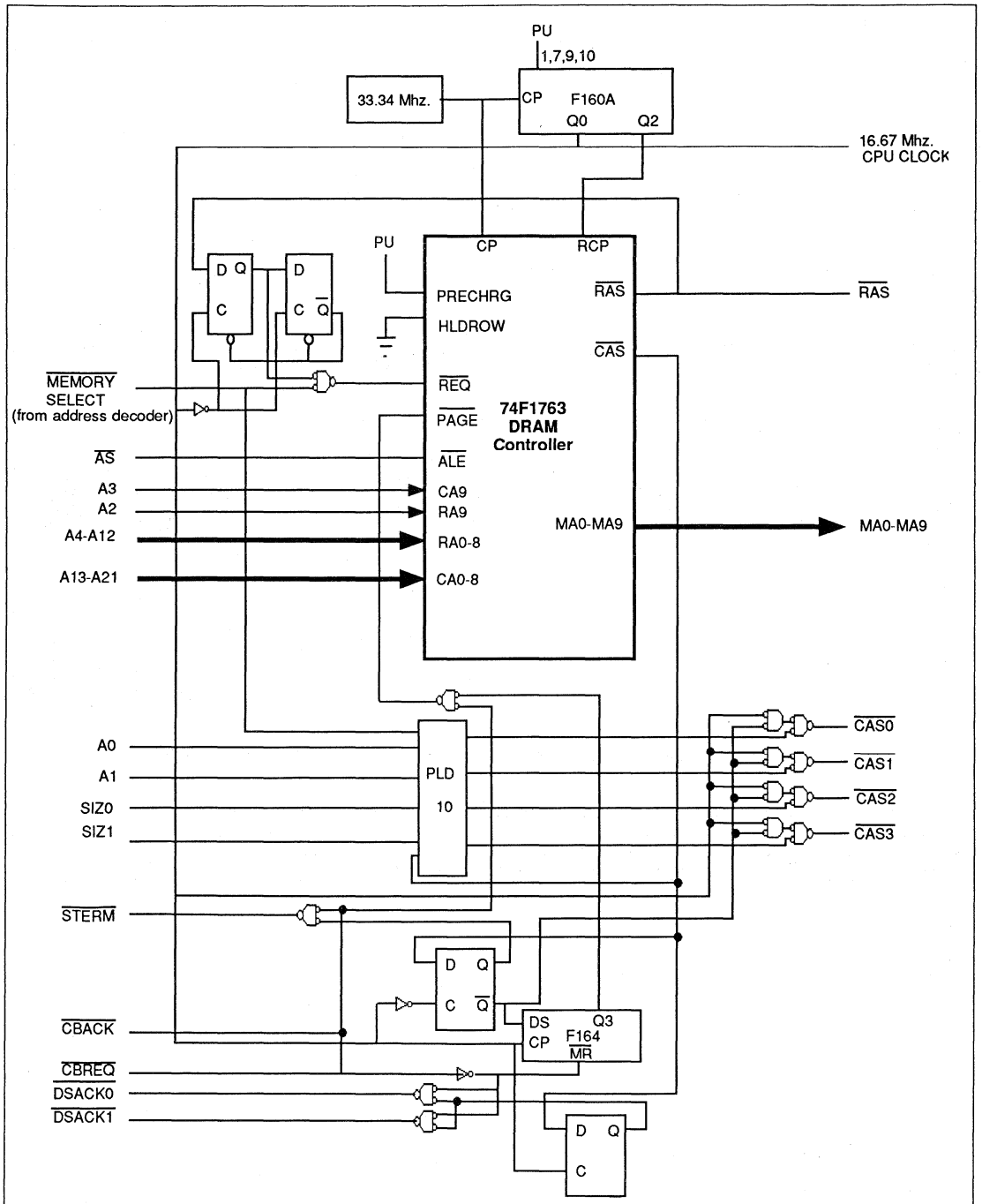
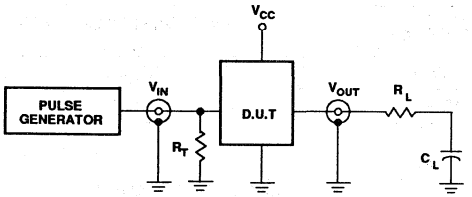


Figure 5: 16.67 MHz 68030 interface with 74F1763 for cache burst mode support using 4Mbytes of 100nsec. nibble-mode DRAMs (Four 32bit words read to or written from cache in only 7 clock cycles).

TEST CIRCUIT AND WAVEFORMS



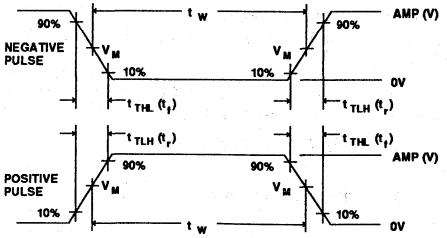
Test Circuit Simulating RAM Boards

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	853-1311
ECN No.	96115
Date of issue	May 11, 1989
Status	Product Specification`
FAST Products	

FAST 74F1764/1765 74F1764-1/1765-1 I Megabit DRAM Dual-Ported Controllers

FEATURES

- **Allows two microprocessors to access the same bank of dynamic RAM**
- **Performs arbitration, signal timing, address multiplexing and refresh**
- **10 address output pins allow direct control of up to 1Mbit dynamic RAMs**
- **External address multiplexing enables control of 4Mbit (or greater) dynamic RAMs**
- **Separate refresh clock allows adjustable refresh timing**
- **74F1764/F1764-1 have on-chip 20-bit address input latch**
- **Allows control of dynamic RAMS with row access times down to 40ns**
- **74F1764/F1765 output drivers designed for incident wave switching**
- **74F1764-1/F1765-1 output drivers designed for first reflected wave switching**

DESCRIPTION

The 74F1764/1765 DRAM Dual-ported Controller is a high speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F1764 vs 74F1765

The 74F1764 though functionally and pin to pin compatible with the 74F1765 differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1764/1765	150MHz	150mA
74F1764-1/1765-1	150MHz	125mA

ORDERING INFORMATION

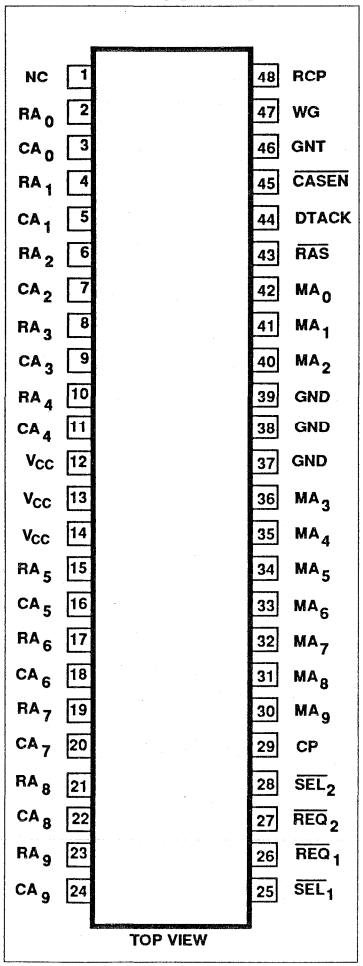
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
48-Pin Plastic DIP	N74F1764N, N74F1765N, N74F1764-1N, N74F1765-1N
44-Pin PLCC	N74F1764A, N74F1765A, N74F1764-1A, N74F1765-1A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

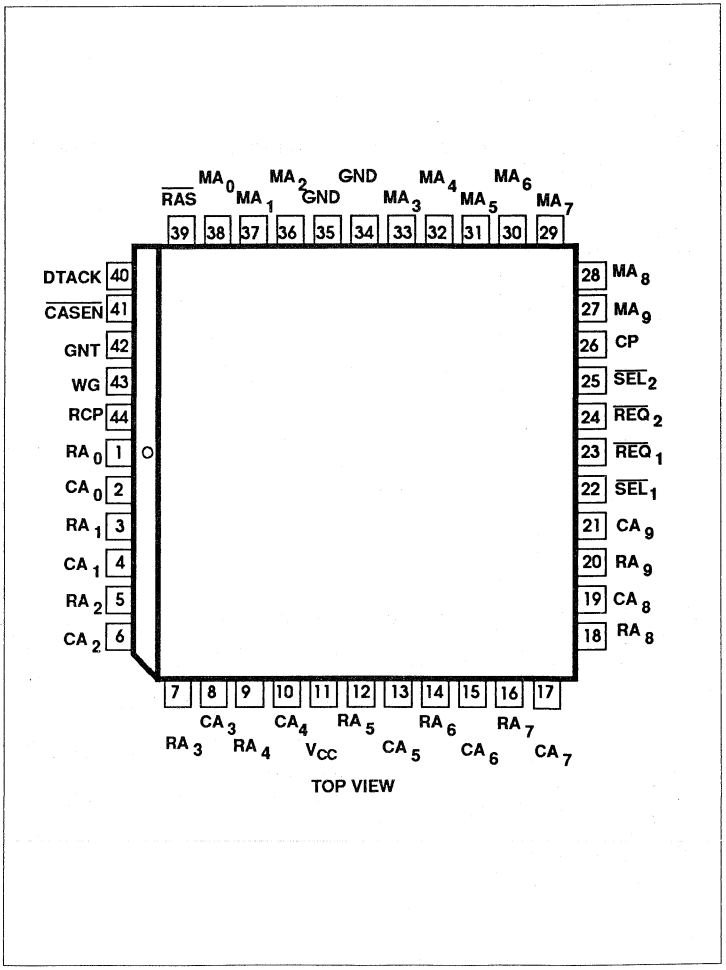
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
RA_0 - RA_9		Row address inputs	1.0/1.0	20µA/0.6mA
CA_0 - CA_9		Column address inputs	1.0/1.0	20µA/0.6mA
$\overline{REQ}_1$, $\overline{REQ}_2$		Memory access request inputs	1.0/1.0	20µA/0.6mA
CP		Clock input	1.0/1.0	20µA/0.6mA
RCP		Refresh clock input	1.0/1.0	20µA/0.6mA
$\overline{SEL}_1$, $\overline{SEL}_2$	'F1764/1765	Select outputs	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
MA_0 - MA_9	'F1764/1765	Memory address outputs	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
GNT	'F1764/1765	Grant output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
$\overline{RAS}$	'F1764/1765	Row address strobe output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
WG	'F1764/1765	Write gate output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
$\overline{CASEN}$	'F1764/1765	Column address strobe enable output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
DTACK	'F1764/1765	Data transfer acknowledge output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA

NOTE:
1.One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state

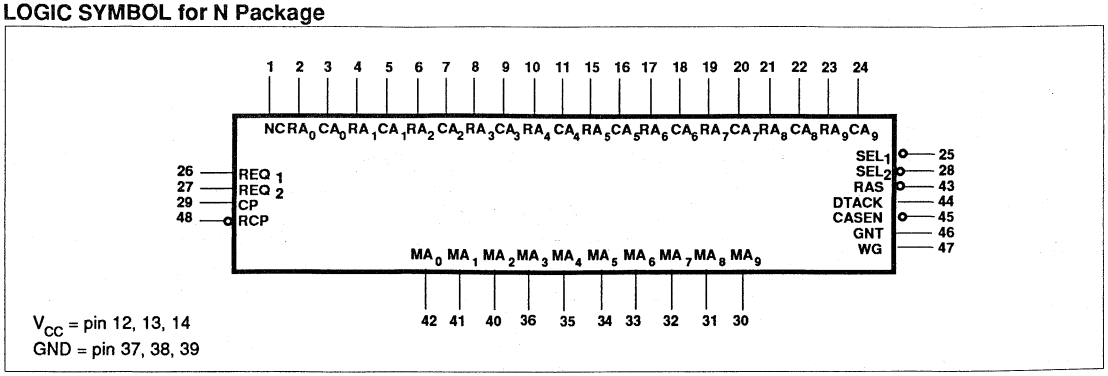
DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



LOGIC SYMBOL for N Package



PIN DESCRIPTION

SYMBOL	PINS DIP	PINS PLCC	TYPE	NAME AND FUNCTION
RA_0	2	1	Inputs	Address inputs used to generate memory row address
RA_1	4	3		
RA_2	6	5		
RA_3	8	7		
RA_4	10	9		
RA_5	15	12		
RA_6	17	14		
RA_7	19	16		
RA_8	21	18		
RA_9	23	20		
CA_0	3	2	Inputs	Address inputs used to generate memory column address
CA_1	5	4		
CA_2	7	6		
CA_3	9	8		
CA_4	11	10		
CA_5	16	13		
CA_6	18	15		
CA_7	20	17		
CA_8	22	19		
CA_9	24	21		
$\overline{REQ}_1$	26	23	Input	Memory access request from Microprocessor 1
$\overline{REQ}_2$	27	24	Input	Memory access request from Microprocessor 2
CP	29	26	Input	Clock input which determines the master timing
RCP	48	44	Input	Refresh clock determines the period of refresh for each row after it is internally divided by 64
$\overline{SEL}_1$	25	22	output	Select signal is activated in response to active $\overline{REQ}_1$ input indicating selection of Microprocessor 1
$\overline{SEL}_2$	28	25	output	Select signal is activated in response to active $\overline{REQ}_2$ input indicating selection of Microprocessor 2
MA_0	42	38	Outputs	Memory address outputs designed to drive address lines of the DRAM
MA_1	41	37		
MA_2	40	36		
MA_3	36	33		
MA_4	35	32		
MA_5	34	31		
MA_6	33	30		
MA_7	32	29		
MA_8	31	28		
MA_9	30	27		
GNT	46	42	Output	Grant output, activated upon start of a memory access cycle
$\overline{RAS}$	43	39	Output	Row address strobe, used to latch the row address into the bank of DRAM (to be connected directly to the RAS inputs of the DRAMs)
WG	47	43	Output	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
$\overline{CASEN}$	45	41	Output	Column address Strobe Address Enable is used to latch the column address into the bank of DRAMs
DTACK	44	40	Output	Data Transfer Acknowledge indicates that the data on the DRAM output lines is valid or the proper access time has been met

ARCHITECTURE

The 74F1764/1765 1 Megabit DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 'F1764/1765 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{REQ}$ inputs will be serviced by activating the corresponding $\overline{SEL}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress The arbitration is accomplished by sampling the $\overline{REQ}_1$ and $\overline{REQ}_2$ inputs on differenrt edges of the CP clock. $\overline{REQ}_1$ is sampled on the rising edge and $\overline{REQ}_2$ on the falling edge (refer to Figure 1 and 2).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated every 64 RCP cycles. The refresh counter is incremented at the end of every refresh cycle, and provides the refresh address.

Since $\overline{SEL}$ outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the $\overline{SEL}$ outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock should be set equal to:
(tras (of the DRAM) + 16-5)/4 plus any system guard-band required.

For the 74F1764-1/1765-1 the CP clock input period should be equal to:
(Tras (of the DRAM) + 22-10)/4 plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate $\overline{REQ}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If however, a refresh cycle is in process, and there is only one active $\overline{REQ}$ input, the $\overline{SEL}$ output corresponding to the active input $\overline{REQ}$ will be asserted but the GNT output will not go High until the completion of the refresh cycle (see Figures 8 and 9).

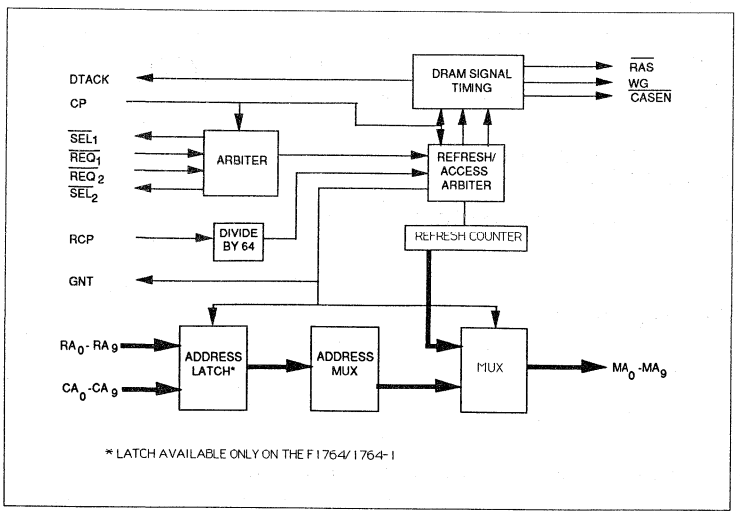
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the $\overline{SEL}$ output for the other processor will not be issued, though GNT is asserted at that time, because the other processor is performing an access cycle. This will insure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the $\overline{SEL}$ output corresponding to the awaiting $\overline{REQ}$ input will be asserted, followed by the GNT output. If ,however, there are any pending refresh requests, assertion of the GNT output will be held OFF until the refresh has been serviced.

When GNT goes High, the RA_0-RA_9 and CA_0-CA_9 address input to the 'F1764/ 'F1764-1 are latched internally and the RA_0-RA_9 signals are propagated to the MA_0-MA_9 outputs. The address inputs are not latched by the 74F1765/F1765-1 and therefore, RA_0-RA_9 inputs propagate directly to the MA_0-MA_9 outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{RAS}$ output is asserted.

BLOCK DIAGRAM



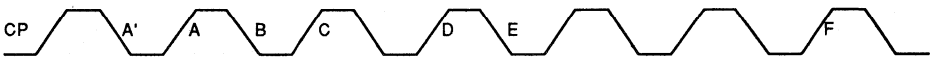
One clock cycle later, the CA_0-CA_9 latch outputs on the 'F1764 and 'F1764-1 or CA_0-CA_9 inputs to the 'F1765 and 'F1765-1 are selected and propagated to the MA_0-MA_9 outputs. The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

A half-clock cycle is again allowed for the CA_0-CA_9 signals to propagate and stabilize. $\overline{CASEN}$ then becomes valid. $\overline{CASEN}$ can be used as $\overline{CAS}$ output or decoded with higher order address signals to produce multiple $\overline{CAS}$ signals. After $\overline{CASEN}$ is valid, the controller will wait for 2 and one-half clock cycles before negating $\overline{RAS}$, making a total $\overline{RAS}$ pulse width of approximately 4 clock cycles. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

All controller output signals are held in this final state until the selected processor withdraws its request by driving its $\overline{REQ}$ input High.
When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

A refresh cycle is serviced by propagating the 10 refresh counter address signals to the MA_0-MA_9 outputs. After a half-clock cycle the $\overline{RAS}$ output is asserted for four cycles and then negated for three clock cycles to meet the $\overline{RAS}$ precharge requirements of the DRAMS (see Figures 3 and 4).

TIMING SEQUENCE

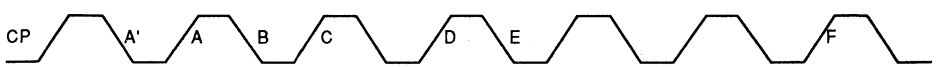


A' $\overline{REQ_2}$ sampled
A $\overline{REQ_1}$ sampled
SEL_1 triggered (SEL_1 triggered by $\overline{REQ_1}$ sample circuitry) ($\overline{REQ_2}$ disabled by SEL_1 circuitry)
B GNT triggered
RA_0-RA_9 and CA_0-CA_9 latched (input address latch triggered by GNT circuitry)*
RA_0-RA_9 propagate to MA_0-MA_9 outputs
C $\overline{RAS}$ triggered
D WG triggered
CA_0-CA_9 selected and propagated to MA_0-MA_9 outputs
E $\overline{CASEN}$ triggered
F $\overline{RAS}$ negated
DTACK triggered

* Only on 'F1764 and 'F1764-1

Figure 1. Sequence of Events for $\overline{REQ_1}$ Memory Access Cycle

TIMING SEQUENCE

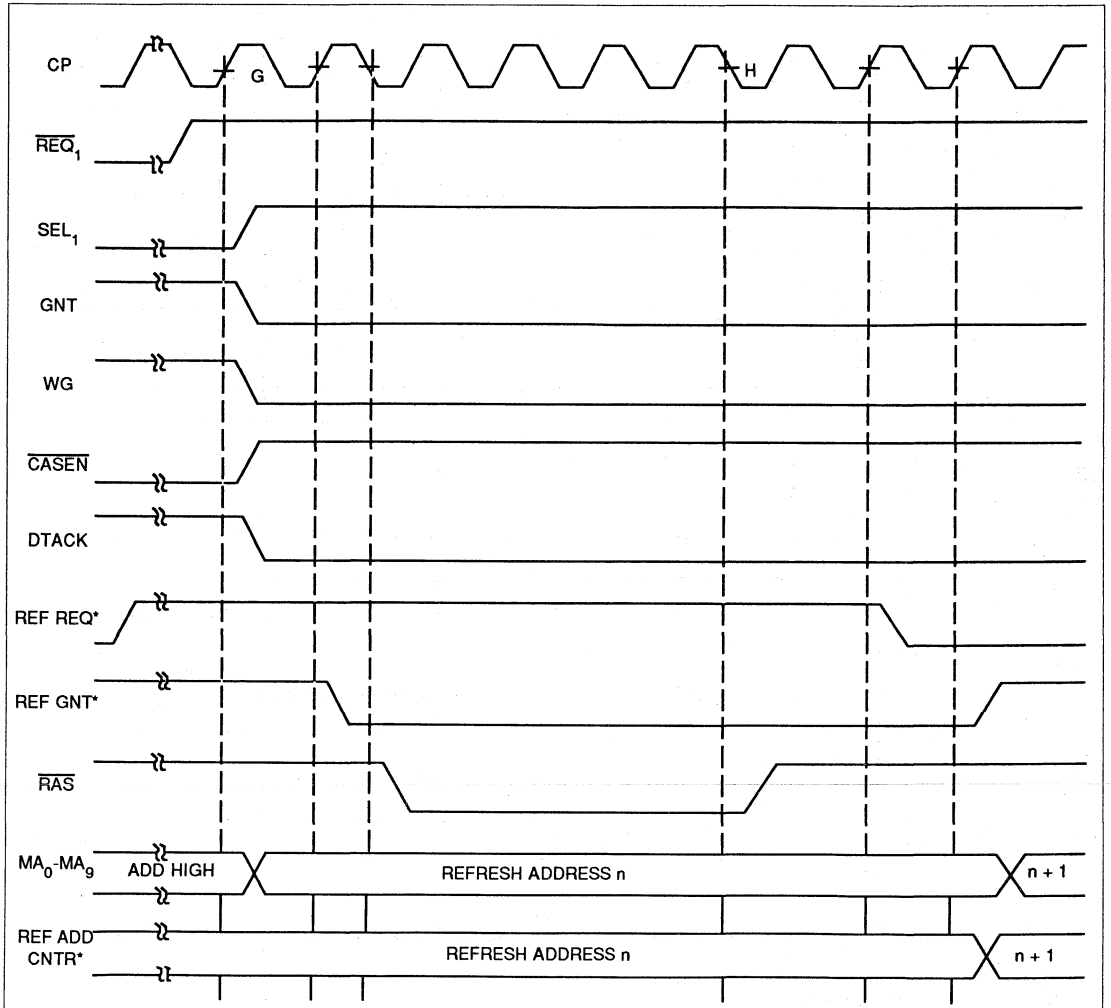


A' $\overline{REQ_2}$ sampled
SEL_2 triggered (SEL_2 triggered by $\overline{REQ_2}$ sampling circuitry)
A $\overline{REQ_1}$ is not sampled(disabled by SEL_2 circuitry)
B GNT triggered
RA_0-RA_9 and CA_0-CA_9 latched (input address latch triggered by GNT circuitry)*
RA_0-RA_9 propagate to MA_0-MA_9 outputs
C $\overline{RAS}$ triggered
D WG triggered
CA_0-CA_9 selected and propagated to MA_0-MA_9 outputs
E $\overline{CASEN}$ triggered
F $\overline{RAS}$ negated
DTACK triggered

* Only on 'F1764 and 'F1764-1

Figure 2. Sequence of Events for $\overline{REQ_2}$ Memory Access Cycle

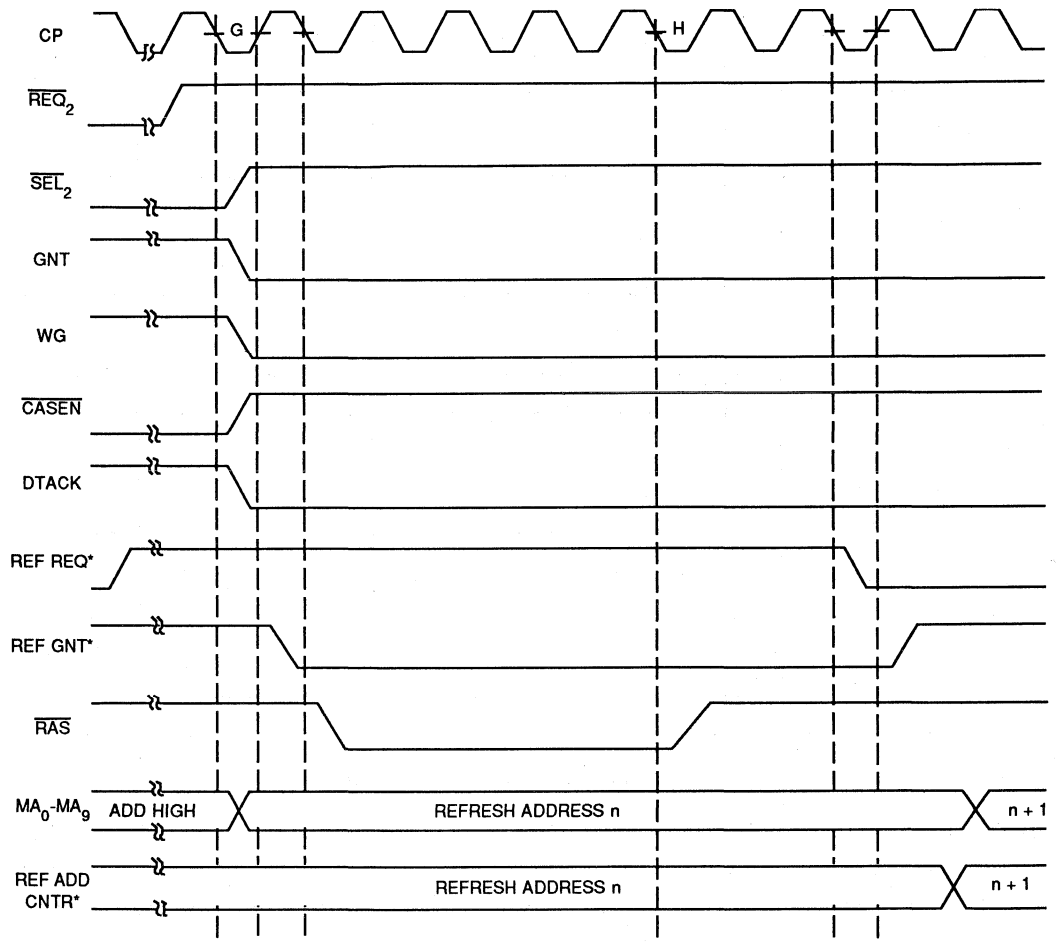
TIMING DIAGRAM



Note: *= These are internal signlas only

Figure 3. Refresh Cycle Timing Following a $\overline{REQ}_1$ Memory Access Cycle

TIMING DIAGRAM



Note: *= These are internal signlas only

Figure 4. Refresh Cycle Timing Following a $\overline{REQ}_2$ Memory Access Cycle

Using 74F1764/1765 AND 74F1764-1/1765-1 TO ADDRESS 4MBIT DRAMS

The addressing capabilities of the 1 Megabit DRAM dual-ported controllers can be extended to address 4Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 5 shows an application, using an external 2-to-1 multiplexer to address 4Mbit dynamic RAMs. The 10-bit internal refresh counter of the controller provides 1024 row addresses which more than meet the refreshing needs for most industry standard 4Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 1024 rows.

Additional address bits (for larger DRAMs) may also be multiplexed externally as long as the DRAM refreshing requirements do not exceed 1024 row addresses.

The WG output of the controller should be used to multiplex between the external row and column addresses. However, it is important that the propagation delay through the external multiplexer does not cause column address setup violations on the dynamic RAM.

APPLICATION

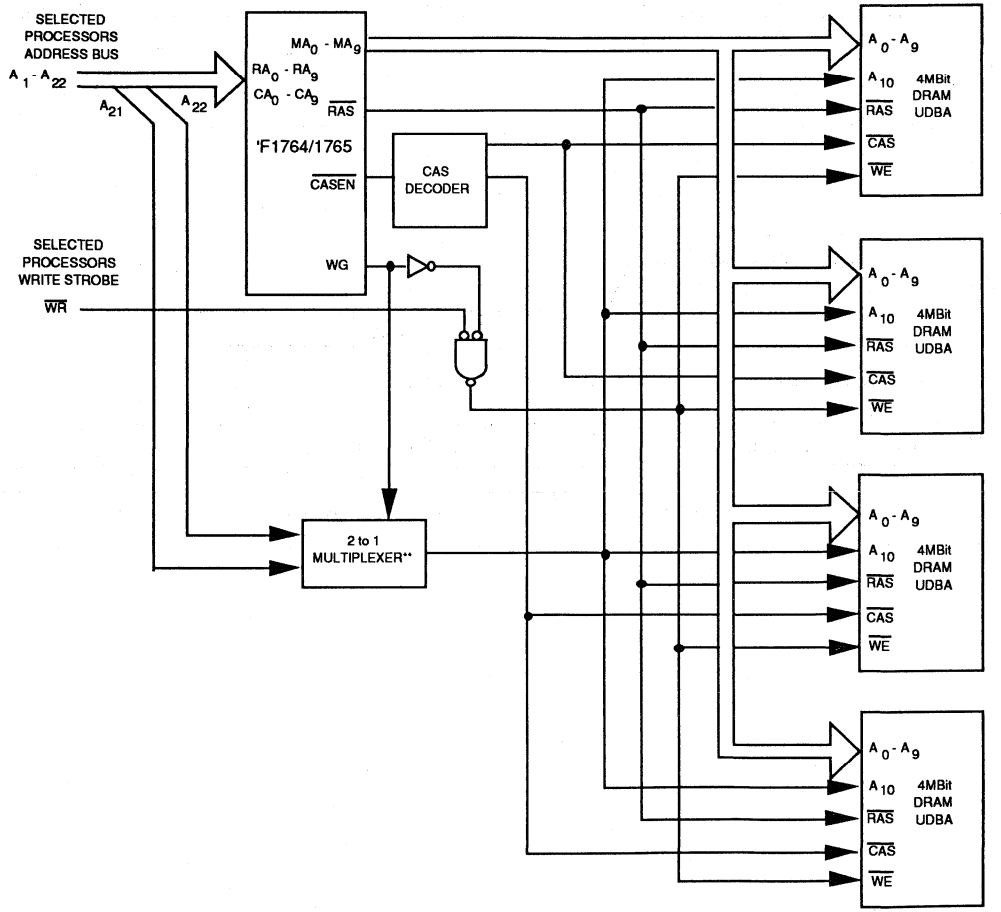


Figure 5. Using the Controller to Address 4Mbit DRAMS

TIMING DIAGRAM

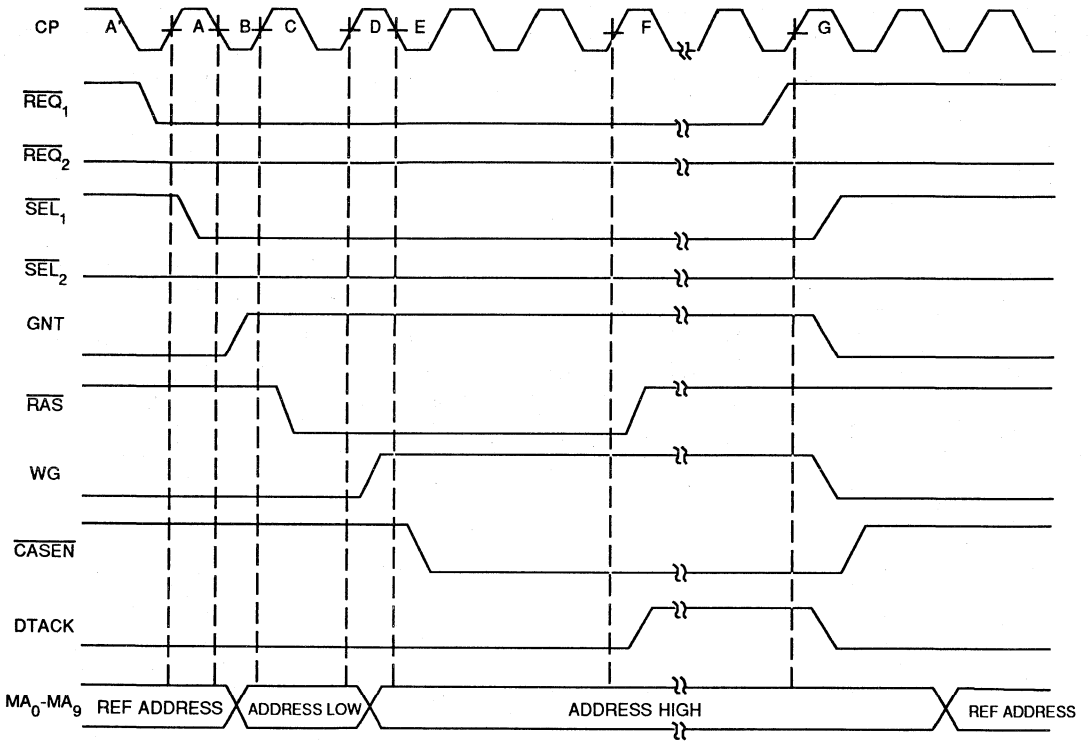


Figure 6. Request 1 ($\overline{REQ_1}$) Memory Access Cycle Timing

TIMING DIAGRAM

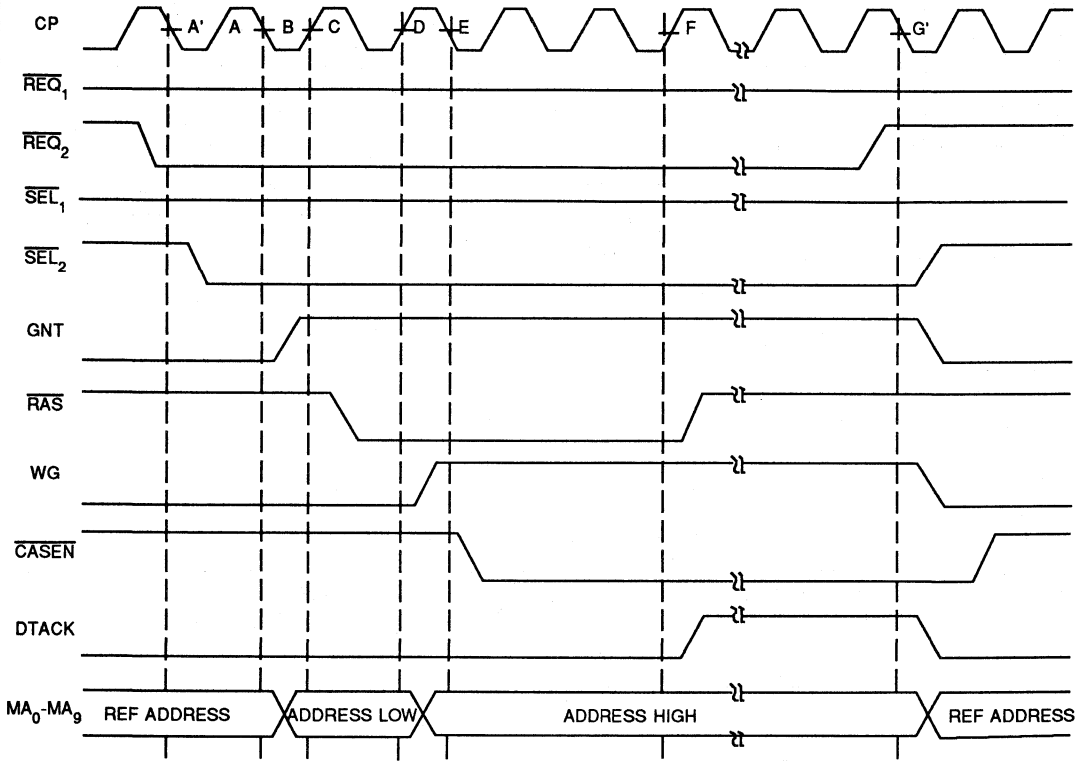


Figure 7. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing

TIMING DIAGRAM

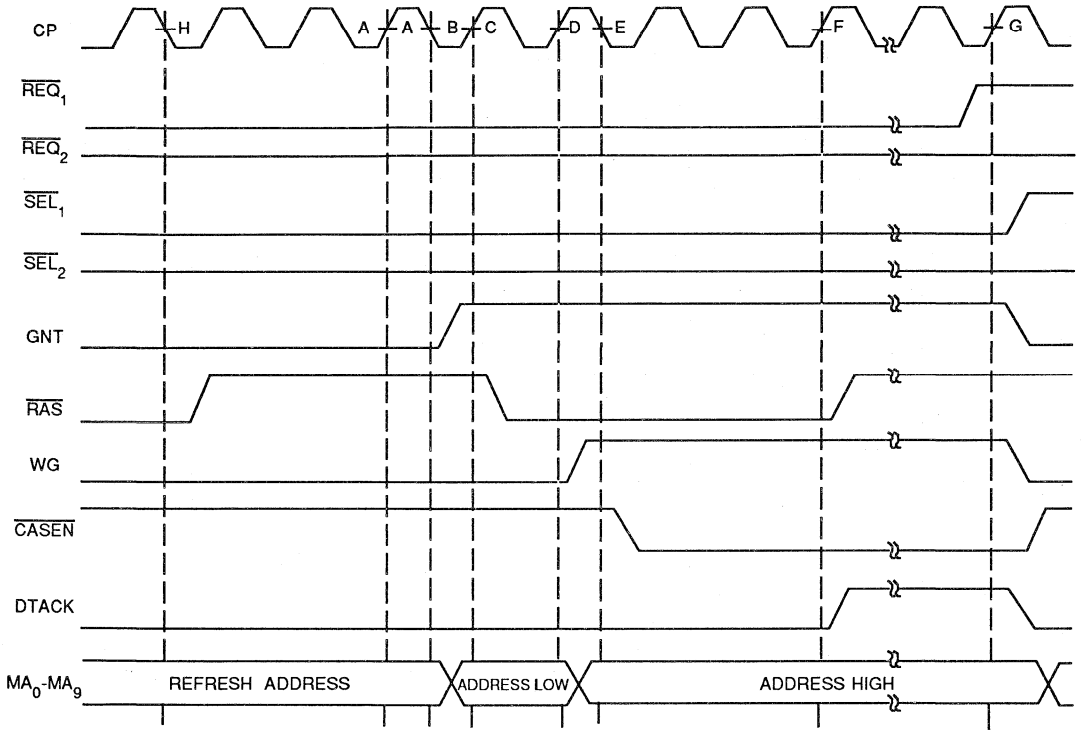


Figure 8. Request 1 ($\overline{REQ_1}$) Memory Access Cycle Timing Following a refresh Cycle

TIMING DIAGRAM

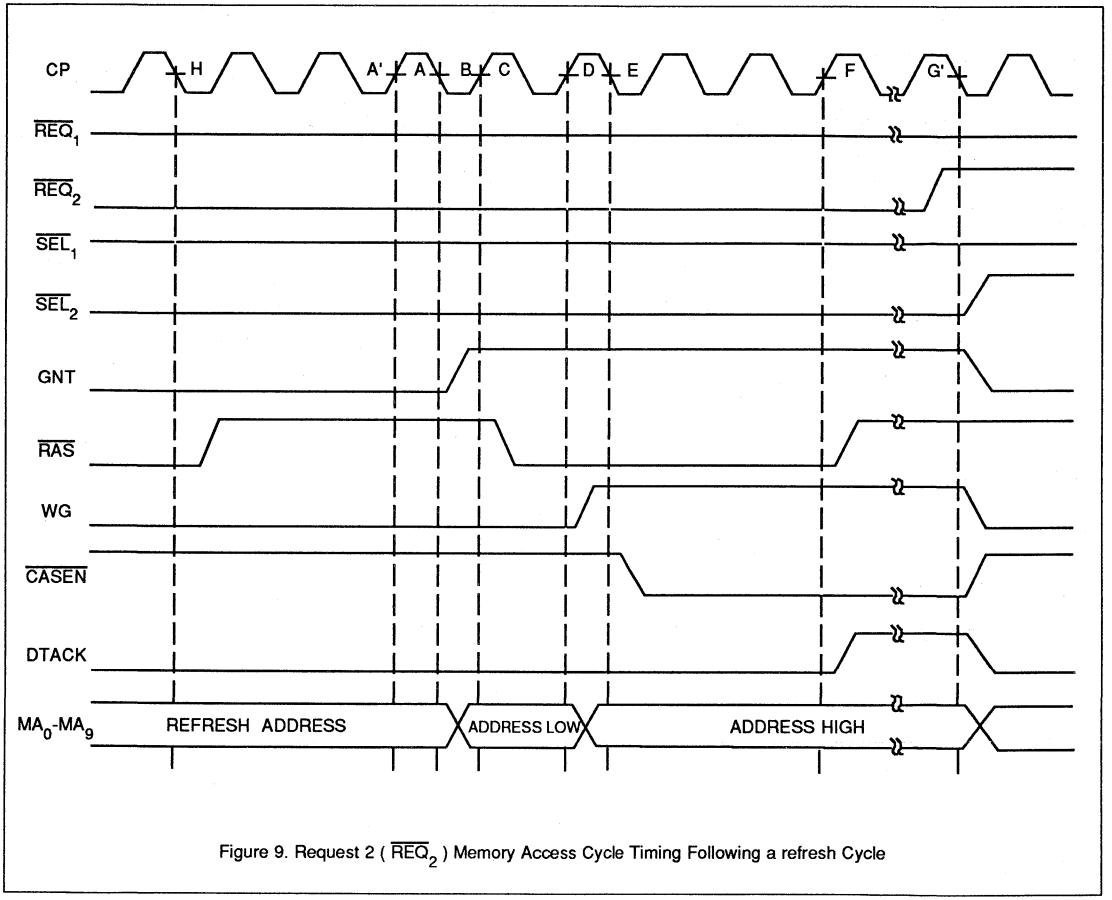


Figure 9. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing Following a refresh Cycle

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current[1]	74F1764/74F1765			-15	mA
		74F1764-1/74F1765-1			-20	mA
I_{OL}	Low-level output current[1]	74F1764/74F1765			24	mA
		74F1764-1/74F1765-1			8	mA
T_A	Operating free-air temperature range		0		70	°C

NOTES:

1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for a detailed discussion.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	74F1764, 74F1765	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7			V
V_{OH2}[3]				I_{OH2}[3]=-35mA	±5%V_{CC}	2.4			V
V_{OH}		74F1764-1, 74F1765-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-20mA	±10%V_{CC}	2.4	2.7		V
					±5%V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage	74F1764, 74F1765	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
				I_{OL2}[4]=60mA	±5%V_{CC}		0.45	0.80	V
		74F1764-1, 74F1765-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=8mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{OH2}[3]				I_{OL2}[3]=75mA	±5%V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[5]	74F1764, 74F1765	V_{CC} =MAX			-100		-225	mA
		74F1764-1, 74F1765-1	V_{CC} =MAX			-60	100	-150	mA
I_{CC}	Supply current (total)	I_{CCH} 74F1764, 74F1765	V_{CC} =MAX				150	200	mA
		I_{CCL} 74F1764, 74F1765					165	210	mA
		I_{CCH} 74F1764-1, 74F1765-1					120	165	mA
		I_{CCL} 74F1764-1, 74F1765-1					125	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Refer to Appendix A.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F1764/74F1765

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L =300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		100	150		100		MHz
t_{PLH}	Propagation delay, CP(G) to $\overline{SEL}_1$		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(A) to $\overline{SEL}_1$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(G') to $\overline{SEL}_2$		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(A') to $\overline{SEL}_2$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(B) to GNT		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to GNT		5.0	10.0	15.0	5.0	16.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA (row address)		5.0 5.0	12.0 11.0	17.0 15.0	5.0 5.0	18.0 16.0	ns
t_{PLH}	Propagation delay, CP(F or H) to $\overline{RAS}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(C) to $\overline{RAS}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(D) to WG		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to WG		8.0	13.0	17.0	8.0	18.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA (column address)		5.0 5.0	12.0 10.0	17.0 15.0	5.0 5.0	18.0 16.0	ns
t_{PLH}	Propagation delay, CP(G or G') to $\overline{CASEN}$		7.0	17.0	23.0	7.0	25.0	ns
t_{PHL}	Propagation delay, CP(E) to $\overline{CASEN}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(F) to DTACK		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to DTACK		6.0	13.0	17.0	5.0	18.0	ns
t_{PLH} t_{PHL}	Propagation delay RA_0-RA_9, CA_0-CA_9 to MA_0-MA_9 (74F1765 only)		4.0 2.0	7.0 5.0	12.0 8.0	4.0 4.0	13.0 9.0	ns

AC SETUP REQUIREMENTS for 74F1764/74F1765

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP		2.0 2.0			2.0 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP		2.0 2.0			3.0 3.0		ns
t_s(H) t_s(L)	Setup time, High or Low RA_0-RA_9, CA_0-CA_9 to CP (74F1764 only)		-4.0[1] -4.0			-5.0 -5.0		ns
t_h(H) t_h(L)	Hold time, High or Low RA_0-RA_9, CA_0-CA_9 to CP (74F1764 only)		5.0 5.0			5.0 5.0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low		5.0 5.0			5.0 5.0		ns
t_w(H) t_w(L)	RCP Pulse width, High or Low		10.0 10.0			10.0 10.0		ns

NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could not be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

AC ELECTRICAL CHARACTERISTICS for 74F1764-1/74F1765-1

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L =300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		150	175		100		MHz
t_{PLH}	Propagation delay, CP(G) to $\overline{SEL}_1$		9.0	12.0	15.0	8.0	17.0	ns
t_{PHL}	Propagation delay, CP(A) to $\overline{SEL}_1$		13.0	16.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(G') to $\overline{SEL}_2$		9.0	12.0	15.0	8.0	17.0	ns
t_{PHL}	Propagation delay, CP(A') to $\overline{SEL}_2$		13.0	16.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(B) to GNT		9.0	12.0	14.0	8.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to GNT		20.0	23.0	26.0	17.0	28.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA (row address)		11.0 14.0	14.0 18.0	17.0 22.0	10.0 13.0	19.0 24.0	ns
t_{PLH}	Propagation delay, CP(F or H) to $\overline{RAS}$		11.0	14.0	16.0	10.0	18.0	ns
t_{PHL}	Propagation delay, CP(C) to $\overline{RAS}$		13.0	17.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(D) to WG		9.0	11.0	14.0	8.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to WG		20.0	23.0	26.0	19.0	26.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA (column address)		12.0 14.0	14.0 18.0	17.0 21.0	11.0 13.0	19.0 23.0	ns
t_{PLH}	Propagation delay, CP(G or G') to $\overline{CASEN}$		14.0	17.0	20.0	12.0	22.0	ns
t_{PHL}	Propagation delay, CP(E) to $\overline{CASEN}$		14.0	16.0	19.0	13.0	21.0	ns
t_{PLH}	Propagation delay, CP(F) to DTACK		10.0	12.0	15.0	9.0	17.0	ns
t_{PHL}	Propagation delay, CP(G or G') to DTACK		20.0	23.0	26.0	19.0	28.0	ns
t_{PLH} t_{PHL}	Propagation delay RA_0-RA_9, CA_0-CA_9 to MA_0-MA_9 'F1765-1 only		9.0 9.0	11.0 12.0	14.0 15.0	8.0 8.0	16.0 17.0	ns

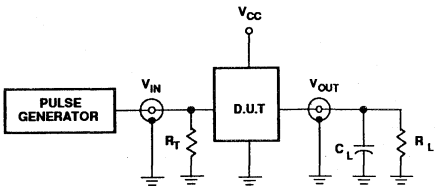
AC SETUP REQUIREMENTS for 74F1784-1/74F1765-1

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP		3.0 3.0	1.0 1.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP		2.0 2.0	0 0		3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low RA_0-RA_9, CA_0-CA_9 to CP 74F1764-1 only		0 0	-1.0[1] -1.0[1]		1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low RA_0-RA_9, CA_0-CA_9 to CP 74F1764-1 only		5.0 5.0	3.0 3.0		6.0 6.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		5.0 5.0	3.0 3.0		5.0 5.0		ns
$t_w(H)$ $t_w(L)$	RCP Pulse width, High or Low		5.0 5.0			5.0 5.0		ns

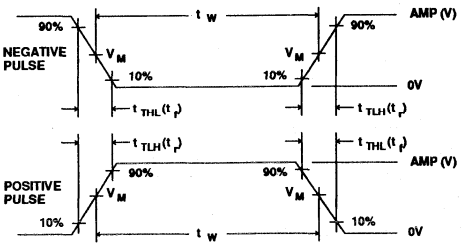
NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could not be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

APPLICATIONS

The 1 Megabit DRAM dual-ported controller can be designed into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (microcontrollers) and the data bus may differ in size.

Figure 10 shows two 68000 processors sharing a 4Meg X 8 (two banks each consisting of sixteen 1 Meg devices) memory. Since the 68000 does not have a multiplexed address and data bus, the 'F 1765/'F1765-1 is appropriate.

Address bit (A21) from either the two 68000 processors distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

Upper and Lower Data Strobes (UDS and LDS) from either of the two 68000 determine whether a byte or word transfer will take place. The additional circuitry is to ensure that DTACK to the 68000 is asserted only when it is selected.

Figure 11 shows two 8086 processors sharing 1 Mbyte (two banks each consisting of sixteen 256K X 1 devices) of dynamic RAM. Using 'F1764/1764-1 in this application may eliminate the need for an external address latch.

Similarly Figure 12 shows two 6020 processors sharing 4Mbyte of memory.

APPLICATION

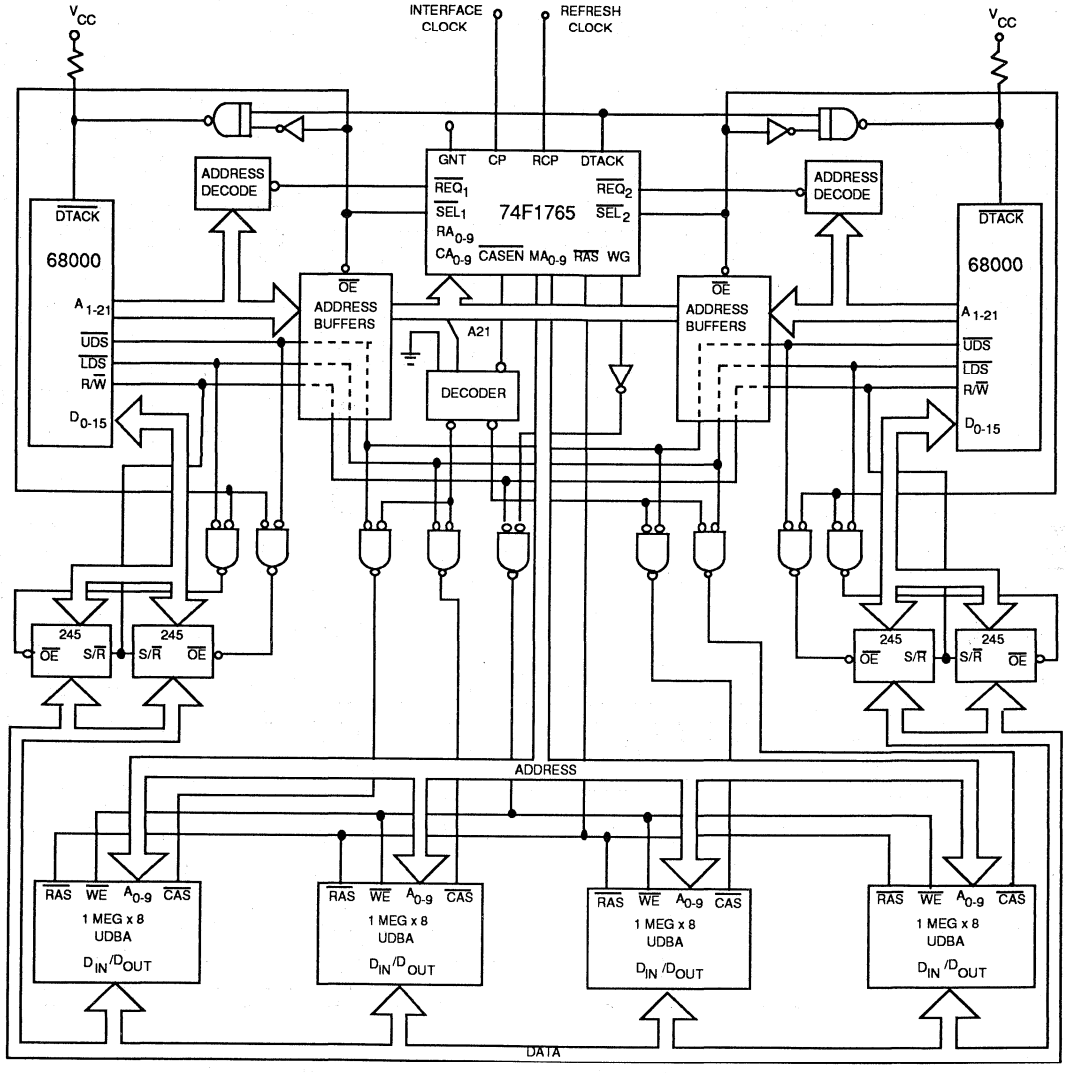
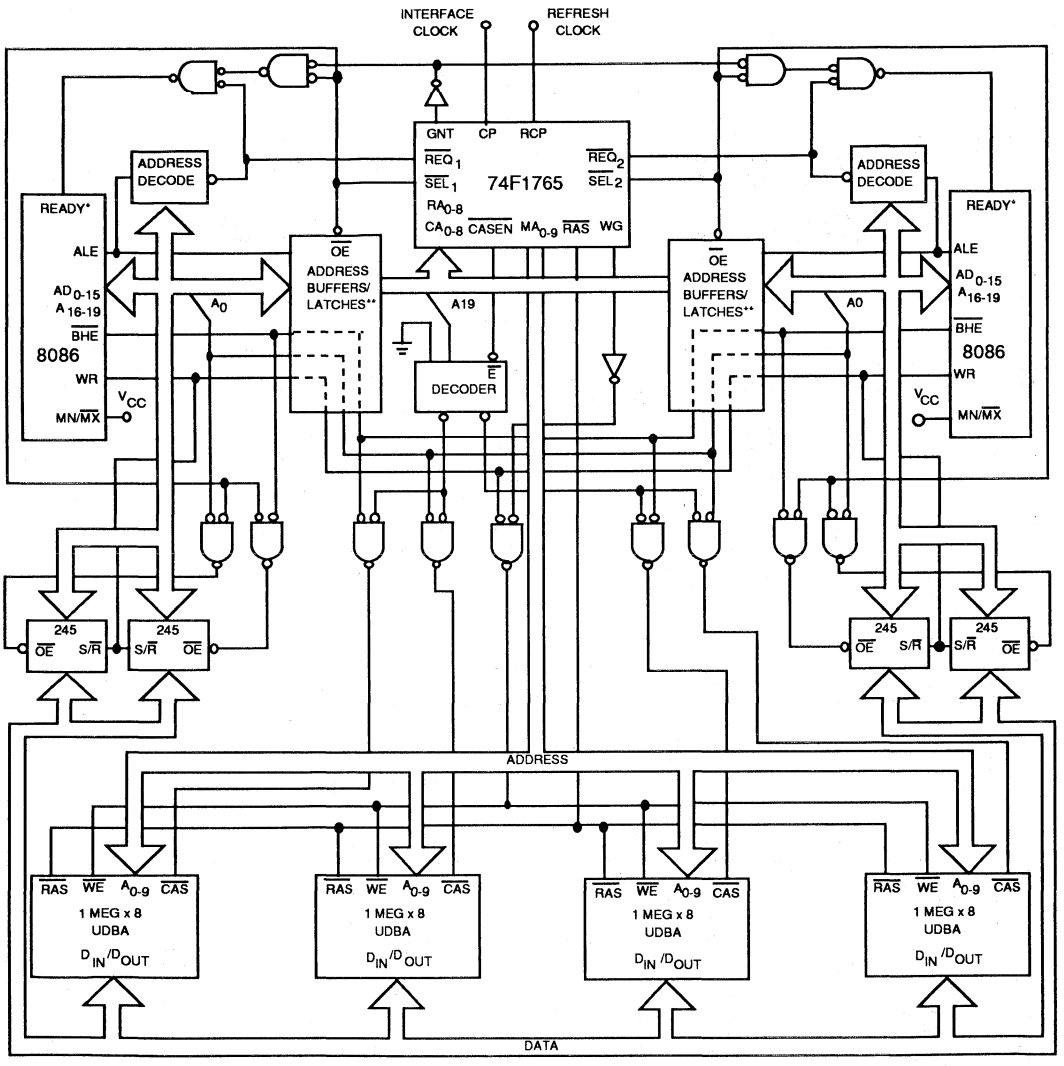


Figure 10. Two 68000 Processors Sharing 4Mbyte of DRAM

APPLICATION



Notes:
*= It might be necessary to synchronize READY by the 8284A. Please refer to the 8086 data sheet.
**= Whether or not the 8086 address needs to be latched externally, should be determined by the relative speeds of the 8086 and the controller

Figure 11. Two 8086 Processors Sharing 1Mbyte of DRAM

APPLICATION

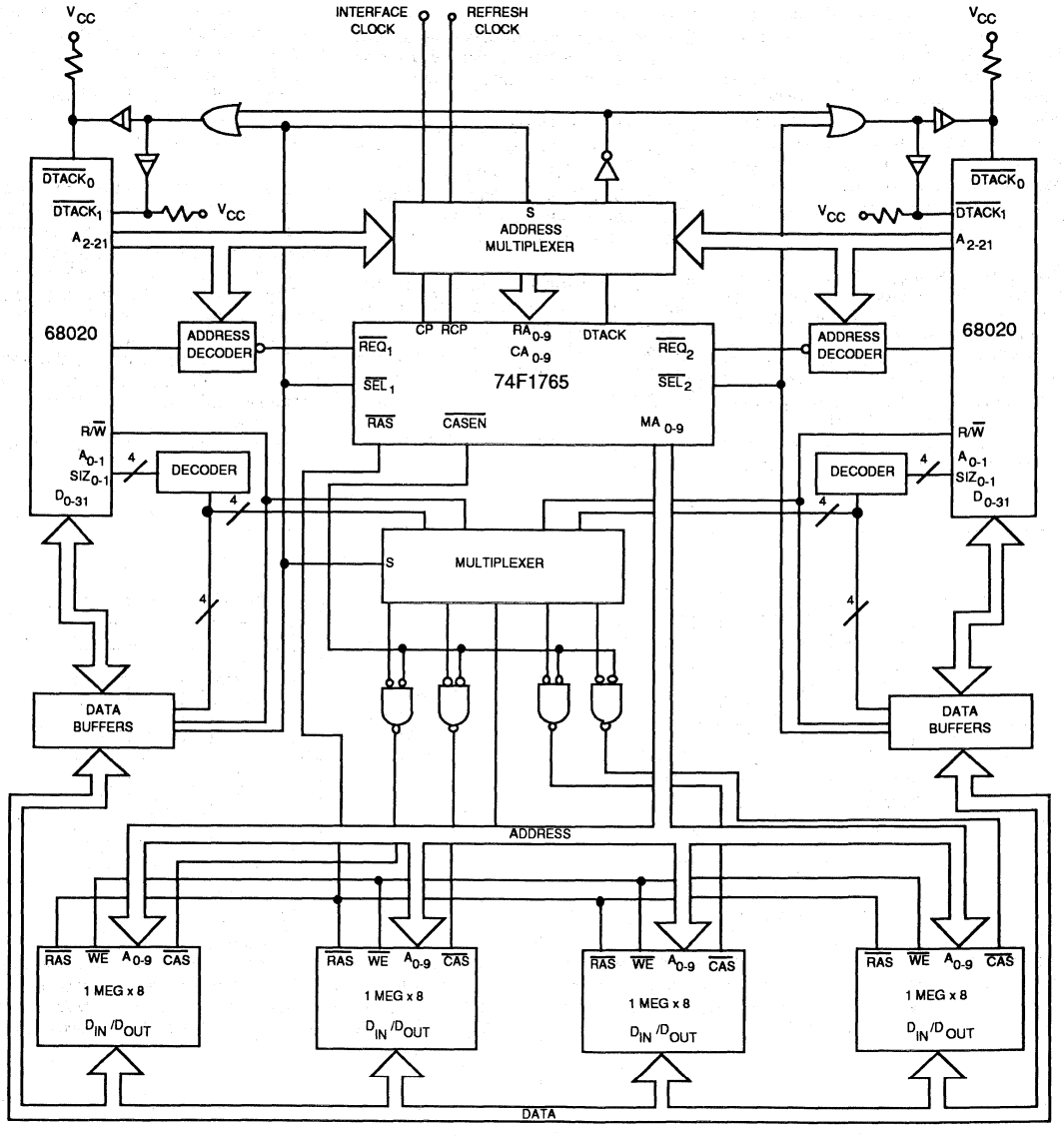


Figure 12. Two 68020 Processors Sharing 4Mbyte of DRAM

APPENDIX A

74F1764 FAMILY LINE DRIVING CHARACTERISTICS

The 74F1764/1765 are designed to provide wave switching in dual-in package (DIP) or zig-zag in-line package (ZIP) housed memory arrays and first reflected wave switching in single in-line package (SIP) or single in-line module(SIM) housed arrays. The 74F1764-1/1765-1, on the other hand, are designed to provide first reflected wave switching with as wide a range of characteristics impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP housed memory arrays is usually around 70Ω. If a signal line has settled out in a High state at 4V and must be pulled down to 0.8V or less on the incident wave, the DRAM controller output must sink (4-0.8)/70A or 46mA at 0.8V. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be swithced on the incidient wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady-state operation at these currents may result in electromigration).

Figures 1-4 show the output I/V characteristics of the DRAM Controller family of devices. These figures also demonstrate graphical method for determining the incident wave (and first reflected wave) characteristics of the devices.

The suggested line termination for the 74F1764/1765 driving a dual in-line packaged or zig-zag packaged DRAMs is shown in Figure 8a. When driving single in-line modules using the 74F1764/1765 or when driving any type of memory arrays with the 74F1764-1/1765-1, The Schottky diode termination shown in Figure 8b can be used (most of these will need no termination at all).

Figures 5-7 are double exposures showing the High to Low to High transitions while driving four banks of eight dual in-line packaged DRAMs. The signal line is unterminated in Figures 5 and 6 , allowing the 74F1764/1765 to ring two volts below ground while the 74F1764-1/1765-1 make nice clean transitions. In Figure 7 the 74F1764/1765 is driving the same signal line but with one of its four branches terminated with its characteristic impedance in series with 300 pF to ground (the worst of the four branches is shown).

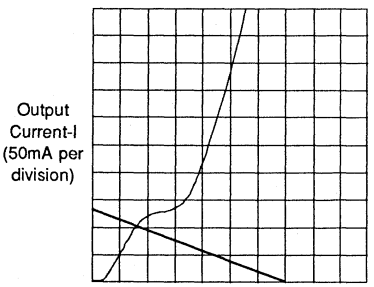


Figure 1.
I-V Output Characteristics of the 74F1764/1765 in the Low state. Light line is the I-V Curve of a 25Ω transmission line settled to 3.5V (typical for recommended termination). The High to Low incident wave on this line will typically be to 0.8V.

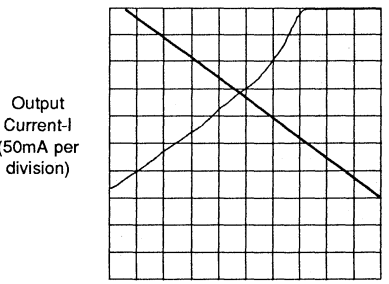


Figure 2.
I-V Output Characteristics of the 74F1764/1765 in the High state. Light line is the I-V Curve of a 35Ω transmission line settled to 0.25V The incident wave on the Low to High transition will typically be to 2.4V on this line. Any line over 35Ω will typically be switched on the incident wave.

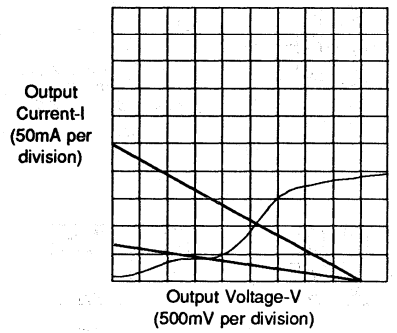


Figure 3.
I-V Output Characteristics of the 74F1764-1/1765-1 in the Low state. Any unterminated line impedance between 18Ω and 70Ω (both shown) will typically switch on the first reflected wave without violating the -1V minimum input voltage specification typical of DRAMs

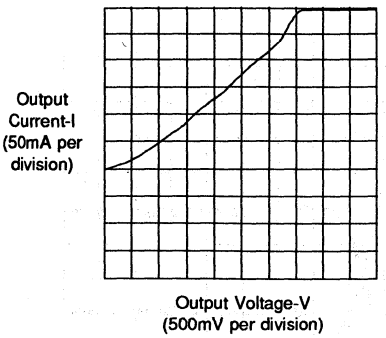


Figure 4.
I-V Output Characteristics of the 74F1764-1/1765-1 in the High state.

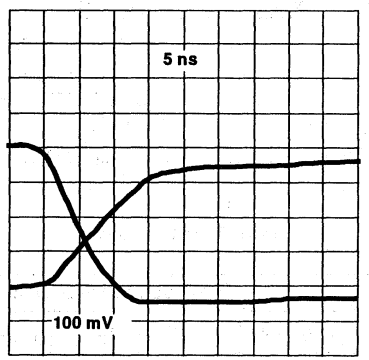


Figure 5.
74F1764-1/1765-1 Driving 32 DRAMS (Unterminated)

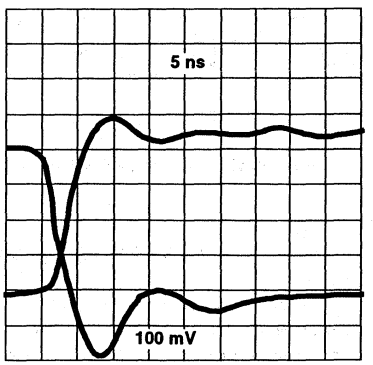


Figure 6.
74F1764/1765 Driving 32 DRAMS (Unterminated)

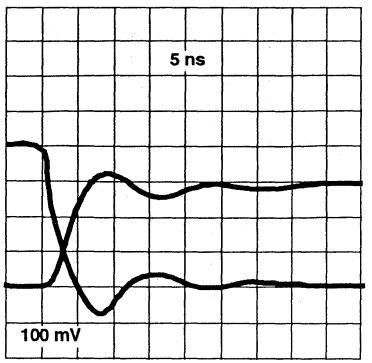


Figure 7.
74F1764/1765 Driving 32 DRAMS (Terminated as in Figure 8a)

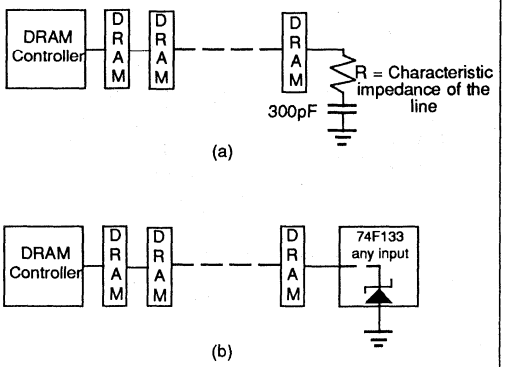
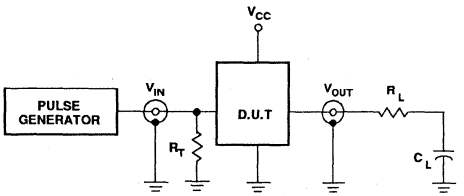


Figure 8.
74F1764/1765 Driving 32 DRAMS (Unterminated)

TEST CIRCUIT AND WAVEFORMS



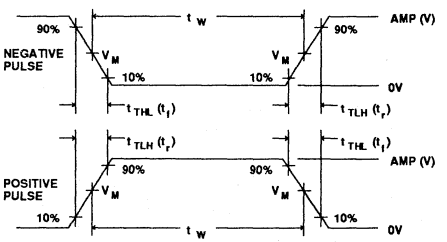
Test Circuit Simulating RAM Boards

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

Document No.	853-
ECN No.	
Date of Issue	June 4, 1990
Status	Product Specification
FAST Products	

FAST 74F1766
Burst Mode DRAM Controller (BMDC)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1766	150MHz	200mA

FEATURES

- Allows burst-mode access for systems using Nibble/Page/Static column mode DRAMs
- Complete control of DRAM access, acknowledge, refresh and address multiplexing functions
- True $\overline{RAS}$ interleaving for minimum refresh and $\overline{RAS}$ precharge overhead
- Asynchronous arbitration to speed up accesses
- Selectable Precharge and Acknowledge times
- Selectable Row address hold times
- Supports $\overline{CAS}$ before $\overline{RAS}$ refresh
- Allows control of dynamic RAMs with row access times down to 30ns
- Output drivers designed for incident wave switching

DESCRIPTION

The Signetics Burst Mode DRAM Controller (BMDC) is a high performance memory timing generator designed to support Page, Nibble or Static Column modes of operation in addition to the normal DRAM access cycles. It performs memory access/refresh arbitration, refresh and memory access timing, $\overline{RAS}$ interleaving, $\overline{CAS}$ byte decoding and controls up to four banks of DRAM.

The BMDC generates DRAM timing and thus requires a companion address multiplexer like the 74F1762 Memory Address Multiplexer for row and column address generation. This provides the flexibility of using the controller with any size of DRAM array by simply using an appropriate address multiplexer. For example when used with the 74F1762, it can control 4Mbit DRAMs.

ORDERING INFORMATION

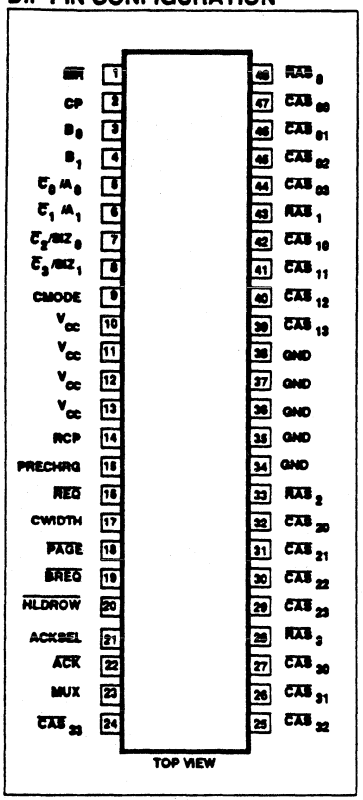
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
48-Pin Plastic DIP	N74F1766N
44-Pin PLCC	N74F1766A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

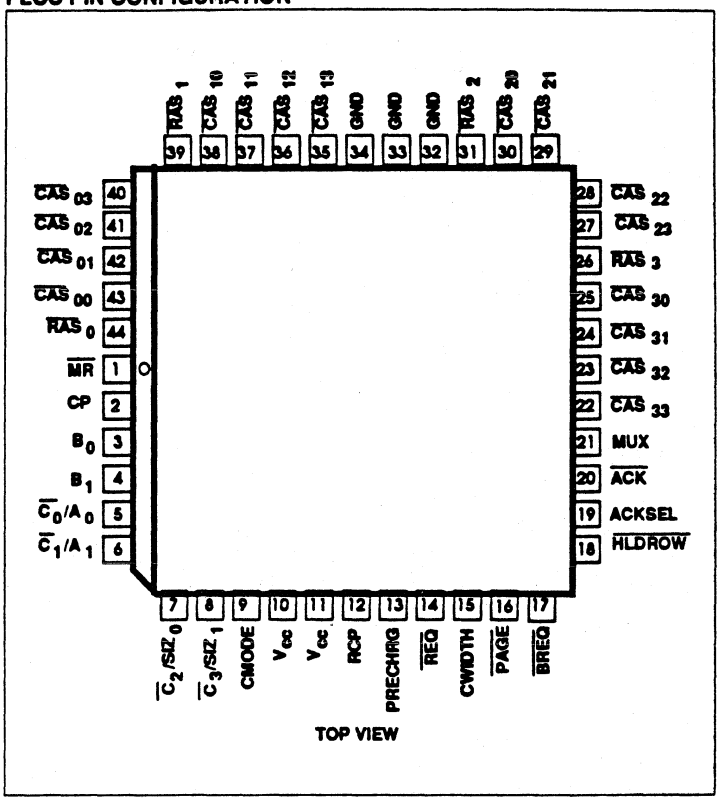
PINS	DESCRIPTION	74F(U.L) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{C}_0/A_0$, $\overline{C}_1/A_1$, $\overline{C}_2/SIZ_0$, $\overline{C}_3/SIZ_1$,	$\overline{CAS}$ Enable inputs	1.0/1.0	20µA/0.6mA
PRECHRG	$\overline{RAS}$ Precharge Select Input	1.0/1.0	20µA/0.6mA
$\overline{REQ}$	Memory access request input	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
RCP	Refresh clock input	1.0/1.0	20µA/0.6mA
B_0, B_1	Bank select inputs	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Reset input	1.0/1.0	20µA/0.6mA
$\overline{BREQ}$	Burst request input	1.0/1.0	20µA/0.6mA
ACKSEL	Acknowledge select input	1.0/1.0	20µA/0.6mA
$\overline{HLDROW}$	Row address hold select input	1.0/1.0	20µA/0.6mA
$\overline{PAGE}$	Page mode select input	1.0/1.0	20µA/0.6mA
CMODE	$\overline{CAS}$ mode select input	1.0/1.0	20µA/0.6mA
CWIDTH	$\overline{CAS}$ width select input	1.0/1.0	20µA/0.6mA
$\overline{ACK}$	Acknowledge output	750/40	3.0mA/24mA
MUX	Address Multiplexer output	150/40	15.0mA/24mA
$\overline{RAS}_{0-3}$	Row address strobe outputs	750/40	15.0mA/24mA
$\overline{CAS}_{00-33}$	Column address strobe outputs	750/40	15.0mA/24mA

NOTE:
1.One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state

DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PINS DIP	PINS PLCC	TYPE	NAME AND FUNCTION
CP	2	2	Input	Clock input. Used by the controller for all timing and arbitration functions.
RCP	14	12	Input	Refresh clock input. Divided internally by 64 to produce an internal Refresh Requst.
PRECHRG	15	13	Input	$\overline{RAS}$ Precharge input. A Low will program the Controller to guarantee 4 CP clock cycles of precharge. A High will guarantee 3 clock cycles of precharge.
$\overline{REQ}$	16	14	Input	Active Low Memory Access Request input, must be asserted for the entire DRAM access cycle. $\overline{REQ}$ is sampled on the rising edge of the CP clock.
B_0,B_1	3,4	3,4	Input	$\overline{RAS}$ Bank Select inputs.See Table1 for decoding information.
$\overline{BREQ}$	19	17	Input	Active Low Burst Request input. If active during an access cycle, the controller automatically toggles $\overline{CAS}_X$ outputs for burst access. The duration of the $\overline{CAS}_X$ outputs are controlled by the CWIDTH and $\overline{PAGE}$ inputs.
ACKSEL	21	19	Input	Acknowledge timing Select input. A Low will program the Controller to assert $\overline{ACK}$ output 2 CP clock cycles after $\overline{CAS}_X$ is asserted. When High $\overline{ACK}$ output will be asserted at the time of assertion of $\overline{CAS}_X$.
$\overline{HLDROW}$	20	18	Input	Row Address Hold input. A Low will program the Controller to assert MUX output 1/2 CP clock cycles after $\overline{RAS}_X$ is asserted. When High MUX output will be asserted at the time of assertion of $\overline{RAS}_X$.
$\overline{ACK}$	22	20	Output	Active Low, 3-state Acknowledge output. Asserted as selected by the ACKSEL input. This is asserted only once during a burst or non-burst memory access cycle, and is not asserted during a memory refresh cycle.
CMODE	9	9	Input	$\overline{CAS}$ Mode select input. When Low $\overline{CAS}_X$ outputs are enabled directly by the $\overline{C}_{0-3}$ inputs. When High $\overline{CAS}_X$ outputs are enabled by decoding the A_{0-1} and SIZ_{0-1} inputs (see Table 2).
$\overline{C}_0/A_0$	5	5	Input	$\overline{CAS}_{X0}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{C}_1/A_1$	6	6	Input	$\overline{CAS}_{X1}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{C}_2/SIZ_0$	7	7	Input	$\overline{CAS}_{X2}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{C}_3/SIZ_1$	8	8	Input	$\overline{CAS}_{X3}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{RAS}_{0-3}$	48,43, 33,28	44,39, 31,26	Output	Active Low Row Address Strobe outputs. Asserted as dictated by the B_{0-1} inputs. (see Table 1 for decoding information)
CWIDTH	17	15	Input	$\overline{CAS}_X$ pulse Width select input. This input selects the initial $\overline{CAS}_X$ pulse width in the burst mode. When Low the initial $\overline{CAS}_X$ pulse is selected equal to 3 CP clock cycles and when High it's selected equal to 2 CP clock cycles. This input is ignored in the non-burst mode.
MUX	23	21	Output	Row/Column address Multiplex output. Asserted as selected by the $\overline{HLDROW}$ input and is used by an external address multiplexer like the 74F1762.
$\overline{CAS}_{00-33}$	47-44, 42-39, 32-29, 27-24	43-40, 38-35, 30-27, 25-22	Output	Active Low Column Address Strobe outputs. Asserted when enabled by the $\overline{CAS}_X$ enable inputs (Table 2) and $\overline{RAS}_X$ bank circuitry.
$\overline{PAGE}$	18	16	Input	$\overline{PAGE}$ mode select input. Controls $\overline{CAS}_X$ pulse width after the initial $\overline{CAS}_X$ pulse in the burst mode. When this input is Low the $\overline{CAS}_X$ pulse is selected equal to 2 CP cycles and when High it's selected equal to 1 CP cycle. This is ignored in the non-burst mode.
$\overline{MR}$	1	1	Input	Active Low Master Reset input. The first Low to High transition on the CP clock after $\overline{RESET}$ is Low will reset the controller. After reset, the 74F1766 remains in test mode until the first rising edge of CP clock.
Vcc	10-13	10,11		Power
GND	34-38	32-34		Ground

ARCHITECTURE

The 74F1766 Burst Mode DRAM controller is a synchronous device, with all signal generation being a function of the input clock (CP).

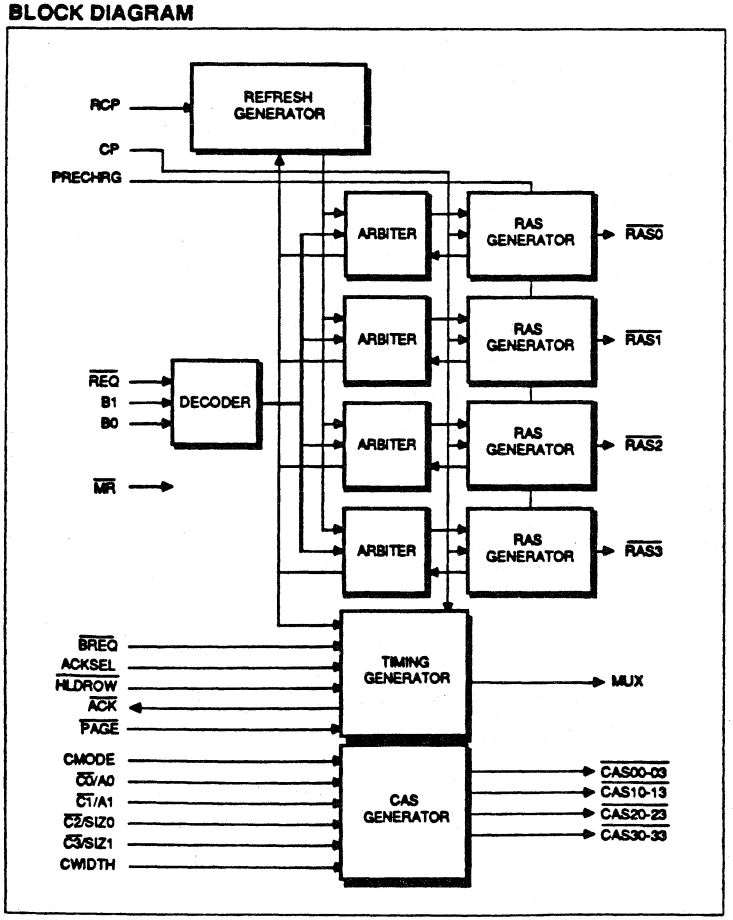
The F1766 Block Diagram (Figure 1) shows the overall architecture of the device. The refresh generator uses $\overline{CAS}$ before $\overline{RAS}$ refresh and produces refresh requests based upon the frequency of the refresh clock (RCP). A memory refresh request is generated for all four banks every 64 cycles of the RCP clock. This request is arbitrated individually for all banks with it's corresponding memory access request made through the $\overline{REQ}$ input. If both memory access and refresh requests are active at a given time the request sampled first will begin immediately and the other request (if still asserted) will be serviced upon completion of the current cycle and it's associated precharge time.

Every one of the four banks have individual refresh monitors to keep track of any missed refreshes during a long page mode access. A total of 127 missed refreshes can be stored by each bank. After the page mode access cycle the controller will burst refresh that bank until all missed refreshes have been performed. In order to limit the number of outputs switching at the same time the refresh generator will stagger the refresh cycles to individual banks, starting from Bank 0. The bank select inputs (B_{0-1}) select which $\overline{RAS}_x$ output will be enabled during the access cycle. Each $\overline{RAS}_x$ output has it's own arbiter and timing generator to allow true $\overline{RAS}$ interleaving between access cycles and refresh cycles. This also enables transparant $\overline{RAS}$ precharge between access cycles. The $\overline{RAS}$ precharge time can be selected by the PRECHRG input to be equal to either 3 or 4 CP clock cycles.

The timing generator allows burst or non-burst accesses selected by the $\overline{BREQ}$ input. If $\overline{BREQ}$ input is asserted during a memory access cycle the controller will automatically toggle $\overline{CAS}_x$ outputs for burst accesses. The duration of the first $\overline{CAS}_x$ pulse is determined by the CWIDTH input, and by the $\overline{PAGE}$ input for subsequent $\overline{CAS}_x$ pulses. This is particularly useful when block moves are made into and out of memory for cache transfers. The $\overline{CAS}_x$ outputs may be gated by the byte select inputs ($\overline{C}_{0-3}$) or by a decoding function generated by the $A_0/A_1/\overline{SIZ}_0/\overline{SIZ}_1$ using the CMODE input. Each $\overline{RAS}$ output has an associated set of $\overline{CAS}$ outputs for that bank, for example $\overline{RAS}_0$ uses $\overline{CAS}_{00-03}$ outputs. This allows simultaneous refresh of $\overline{RAS}$ banks while another bank is being accessed by the processor.

The ACKSEL input allows the assertion of Acknowledge ($\overline{ACK}$) output to be either when $\overline{CAS}_x$ is asserted or 2 CP clock cycles after that. $\overline{ACK}$ stays asserted in the burst mode until $\overline{REQ}$ is negated. The $\overline{HLDROW}$ input can be used to assert MUX output when $\overline{RAS}_x$ is asserted or one-half CP clock cycle after that.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Most DRAMs require that $\overline{RAS}$ and $\overline{CAS}$ inputs be toggled a number of times before the DRAM may be used. The BMDC has an initialization feature which allows the automatic excersizing of the DRAMs. This is done by resetting the device, which forces the refresh counter to be offset by ten, thus forcing ten refresh cycles before allowing any memory access cycles. The $\overline{REQ}$ input is sampled on the rising edge of the CP clock. If no refresh request is being serviced, one of the $\overline{RAS}_x$ outputs (depending on the B_{0-1} inputs) will be asserted immediately. Depending on the state of the $\overline{HLDROW}$ input, the MUX output will be driven High either at the assertion of $\overline{RAS}_x$ or one-half CP cycle after that. One CP cycle after the assertion of $\overline{RAS}_x$, the $\overline{CAS}_x$ outputs enabled either by the $\overline{C}_{0-3}$ inputs or the decoded function of $A_0/A_1/\overline{SIZ}_0/\overline{SIZ}_1$ (as selected by the CMODE input) will be asserted. If the ACKSEL input is High, the $\overline{ACK}$ output will be asserted at this time; otherwise it will be asserted 2 CP cycles after this time.

The $\overline{BREQ}$ input is sampled when the $\overline{CAS}_x$ outputs are initially asserted, and this determines what will take place on the $\overline{CAS}_x$ outputs after their initial assertion. If $\overline{BREQ}$ is High, the $\overline{RAS}_x$, MUX and $\overline{CAS}_x$ outputs will remain in their present state until the negation of $\overline{REQ}$, at which time all these signals are negated. Negation of $\overline{REQ}$ is asynchronous to the CP clock cycle and therefore is not sampled

by the clock. If the $\overline{BREQ}$ is Low at the assertion of $\overline{CAS}_X$, the $\overline{RAS}_X$ and MUX outputs will stay in their existing state but the $\overline{CAS}_X$ outputs after staying Low for 2 CP cycles will alternately be negated and asserted for one CP clock cycle if $\overline{PAGE}$ input is High or for two CP clock cycles if $\overline{PAGE}$ input is Low. This process will continue untill the negation of the $\overline{REQ}$ input, at which time the $\overline{RAS}_X$, MUX, $\overline{CAS}_X$ and $\overline{ACK}$ outputs will be negated.

As mentioned before, the controller guarantees a $\overline{RAS}$ precharge on all the $\overline{RAS}_X$ outputs to be either 3 or 4 CP clock cycles as selected by the PRECHRG input. This precharge function is independent among the $\overline{RAS}_X$ outputs, which means that, by connecting the appropriate low-order address lines from the processor to the B_{0-1} inputs, sequential accesses, a common occurance with microprocessors, will result in no precharge overhead.

The refresh function is also independent between the $\overline{RAS}_X$ outputs, which means that three $\overline{RAS}_X$ outputs can be performing a $\overline{CAS}$ before $\overline{RAS}$ refresh, while the fourth is in the precharge mode or is being accessed, thus reducing the overall refresh overhead.

Output driving Characteristics

Considering the transmission line characteristics of the DRAM arrays, the outputs of the DRAM controller have been designed to provide incident-edge switching (in Dual-Inline-Packaged memory ar rays), needed in high performance systems. For more information on the driving characteristics, please refer to Signetics application note number AN218. The driving characteristics of the 74F1766 are the same as those of the 74F765 shown in the application note.

Testing the BMDC

Precautions have been taken in the design of the BMDC to facilitate testing of the device. After a $\overline{MR}$ is issued and the CP input is toggled from Low to High all internal flip-flops are brought into a known state, and the device goes into the test mode from the time $\overline{MR}$ is deasserted till the time the first Low to High transition occurs on the CP clock. During the test mode, bank refresh counters (that keep track of missed refreshes) are clocked by a High to Low transition on the $\overline{C}_{0-3}$ inputs and the main refresh counter is clocked on the rising RCP clock edge. The comparators that compare the contents of the main refresh counter and refresh counters of individual banks are clocked by the Low to High transition on the PRECHRG input and are gated on to $\overline{RAS}_X$ outputs by the $\overline{C}_{0-3}$ inputs. So whenever $\overline{C}_{0-3}$ are Low, $\overline{RAS}$ outputs are disabled (pulled High). If the contents of the main refresh counter and the individual bank counters are equal, the corresponding $\overline{RAS}$ output will be High, if not equal the corresponding $\overline{RAS}$ output will be Low. This allows full testing of the Counters and comparators with relatively few lines of code.

B_0	B_1	$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$
0	0	0	1	1	1
0	1	1	0	1	1
1	0	0	1	0	1
1	1	0	1	1	0

TABLE 1: BANK SELECT DECODE

CMODE	OPERATION	$\overline{C}_3/SIZ_1$	$\overline{C}_2/SIZ_0$	$\overline{C}_1/A_1$	$\overline{C}_0/A_0$	$\overline{CAS}_{X3}$	$\overline{CAS}_{X2}$	$\overline{CAS}_{X1}$	$\overline{CAS}_{X0}$
1	LONG WORD	0	0	0	0	0	0	0	0
1		0	0	0	1	0	0	0	1
1		0	0	1	0	0	0	1	1
1		0	0	1	1	0	1	1	1
1	BYTE	0	1	0	0	1	1	1	0
1		0	1	0	1	1	1	0	1
1		0	1	1	0	1	0	1	1
1		0	1	1	1	0	1	1	1
1	WORD	1	0	0	0	1	1	0	0
1		1	0	0	1	1	0	0	1
1		1	0	1	0	0	0	1	1
1		1	0	1	1	0	1	1	1
1	THREE BYTES	1	1	0	0	1	0	0	0
1		1	1	0	1	0	0	0	1
1		1	1	1	0	0	0	1	1
1		1	1	1	1	0	1	1	1

TABLE 2: BYTE SELECT DECODE

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	All pins except $\overline{ACK}$			-15	mA
		$\overline{ACK}$ output			-3	mA
I_{OL}	Low-level output current				24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	All pins except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.5	3.2		V
					±5%V_{CC}	2.7	3.4		V
V_{OH2}[3]				I_{OH2}[3]=-35mA	±5%V_{CC}	2.4			V
V_{OH}		$\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	All pins except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{OL2}[3]				I_{OL2}[3]=60mA	±5%V_{CC}		0.45	0.80	V
V_{OL}		$\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V					-0.6	mA
I_{OZH}	Off-state output current, High level voltage applied		V_{CC} =MAX, V_o = 2.7V					50	µA
I_{OZL}	Off-state output current, Low level voltage applied		V_{CC} =MAX, V_o = 0.5V					-50	µA
I_{OS}[4]	Short-circuit output current		V_{CC} =MAX	All pins except $\overline{ACK}$		-100		-225	mA
				$\overline{ACK}$ output		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX				185	240	mA
		I_{CCL}					200	260	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH}[2] & I_{OL}[2] are transient currents necessary to guarantee a Low to High & a High to Low transition in a 30 OHM transmission line respectively. Refer to Application note number AN218 for further explanation.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

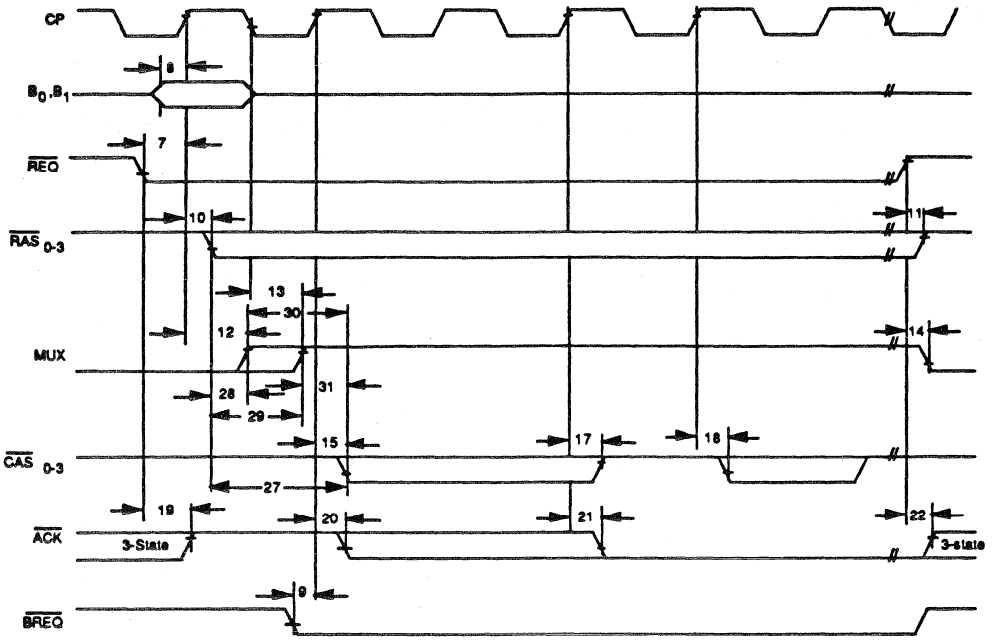
AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=25°C, V_{cc}=+5.0V ±10%, C_L=300pF, RL=70Ω			T_A=0°C to +70°C, V_{cc}=+5.0V ±10%, C_L=300pF, RL=70Ω		
			Min	Typ	Max	Min	Max	
1	CP clock period (tcp)		10			10		ns
2	CP clock low time		4			4		ns
3	CP clock high time		6			6		ns
4	RCP clock period		100			100		ns
5	RCP clock low time		10			10		ns
6	RCP clock high time		10			10		ns
7	Setup time $\overline{REQ}$(↓) to CP(↑)		2.5			4		ns
8	Setup time B_0, B_1 to CP(↑)		3			4		ns
9	Setup time $\overline{BREQ}$ to CP(↑)		3			4		ns
10	Propagation delay CP(↑) to $\overline{RAS}$(↓)		3	7.5	9.5	3	10	ns
11	Propagation delay $\overline{REQ}$(↑) to $\overline{RAS}$(↑)		4	9	12	3	13	ns
12	Propagation delay CP(↑) to MUX(↑)	$\overline{HLDROW}$ = 1	3	8	10	3	11	ns
13	Propagation delay CP(↓) to MUX(↑)	$\overline{HLDROW}$ = 0	2	5.5	7.5	2	8.5	ns
14	Propagation delay $\overline{REQ}$(↑) to MUX(↓)		4	8.5	10.5	4	11.5	ns
15	Propagation delay CP(↑) to $\overline{CAS}$(↓)		3	8.5	11.5	3	12	ns
16	Propagation delay $\overline{REQ}$(↑) to $\overline{CAS}$(↑)		4	9.5	12	4	14	ns
17	Propagation delay CP(↑) to $\overline{CAS}$(↑)	$\overline{BREQ}$ = 0	3	8	10	3	11	ns
18	Propagation delay CP(↑) to $\overline{CAS}$(↓)	$\overline{BREQ}$ = 0	3	9	11	3	12	ns
19	Propagation delay $\overline{REQ}$(↓) to $\overline{ACK}$(3-state to High)		2	5	7	2	8	ns
20	Propagation delay CP(↑) to $\overline{ACK}$(↓)	ACKSEL = 1	3	7.5	9.5	3	10	ns
21	Propagation delay CP(↑) to $\overline{ACK}$(↓)	ACKSEL = 0	3	7.5	9.5	3	10	ns
22	Propagation delay $\overline{REQ}$(↑) to $\overline{ACK}$(Low to 3- state)		2	5	7	2	7.5	ns
23	Propagation delay CP(↑) to $\overline{CAS}$(↓) *	REFRESH CYCLE	4	9.5	12	4	13	ns
24	Propagation delay CP(↑) to $\overline{RAS}$(↓) *	REFRESH CYCLE	3	7.5	9.5	3	10	ns
25	Propagation delay CP(↑) to $\overline{CAS}$(↑) *	REFRESH CYCLE	4	9.5	12	4	14	ns
26	Propagation delay CP(↑) to $\overline{RAS}$(↑) *	REFRESH CYCLE	4	9	11	3	13	ns
27	Propagation delay $\overline{RAS}$(↓) to $\overline{CAS}$(↓)		1tcp-1	1tcp+1	1tcp+2.5	1tcp-1	1tcp+3	ns

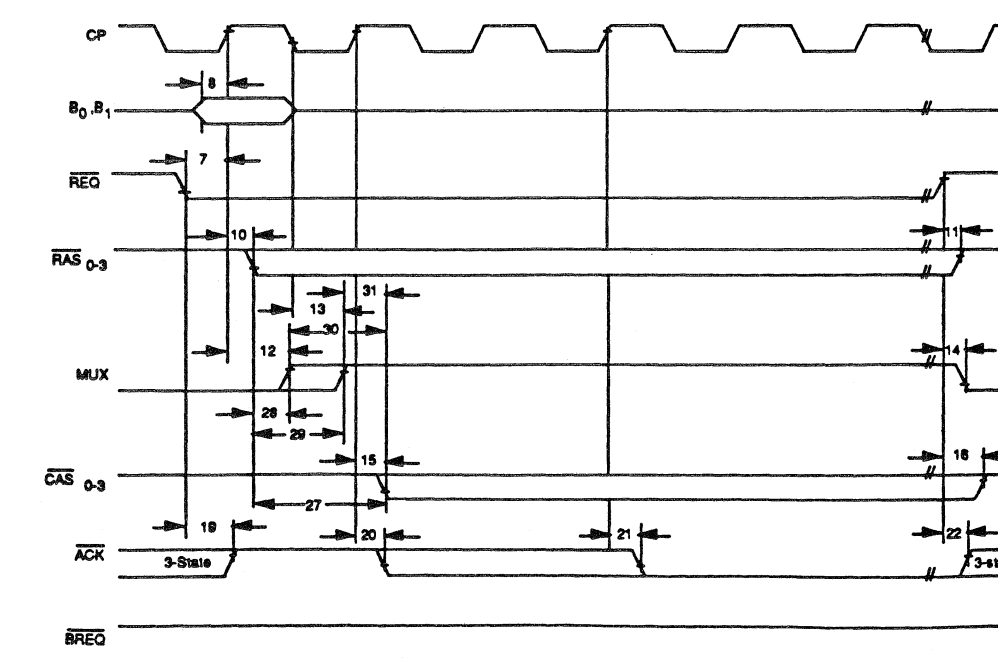
* The same parameters will hold for a refresh cycle during $\overline{RAS}_1$, $\overline{RAS}_2$ and $\overline{RAS}_3$ access cycles.

AC ELECTRICAL CHARACTERISTICS

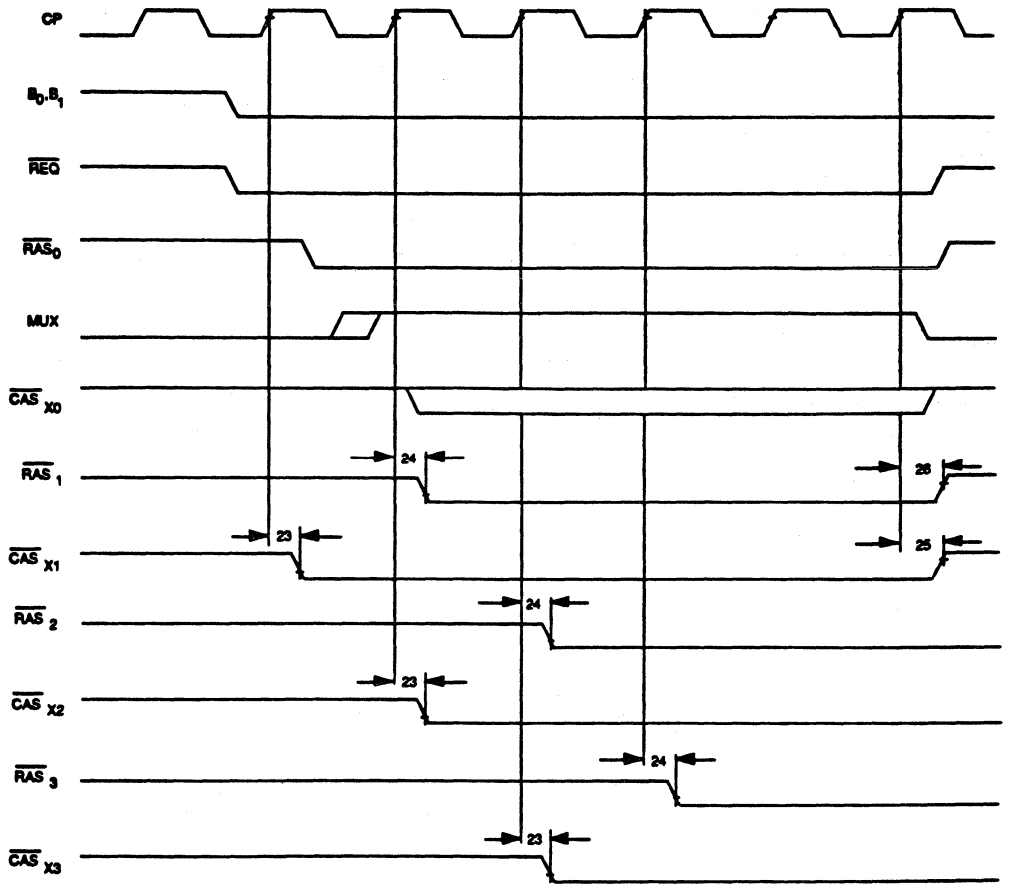
NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=25°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
28	Propagation delay $\overline{RAS}$(↓) to MUX(↑)	HLDROW = 1	-1	0.5	2	-1.5	2.5	ns
29	Propagation delay $\overline{RAS}$(↓) to MUX(↑)	HLDROW = 0	1/2tcp-3.5	1/2tcp-1.5	1/2tcp	1/2tcp-1.5	1/2tcp+2.5	ns
30	Propagation delay MUX(↑) to $\overline{CAS}$(↓)	HLDROW = 1	1tcp-1.5	1tcp+0.5	1tcp+2	1tcp-2.5	1tcp+2.5	ns
31	Propagation delay MUX(↑) to $\overline{CAS}$(↓)	HLDROW = 0	1/2tcp+0.5	1/2tcp+2	1/2tcp+4.5	1/2tcp-0.5	1/2tcp+5	ns



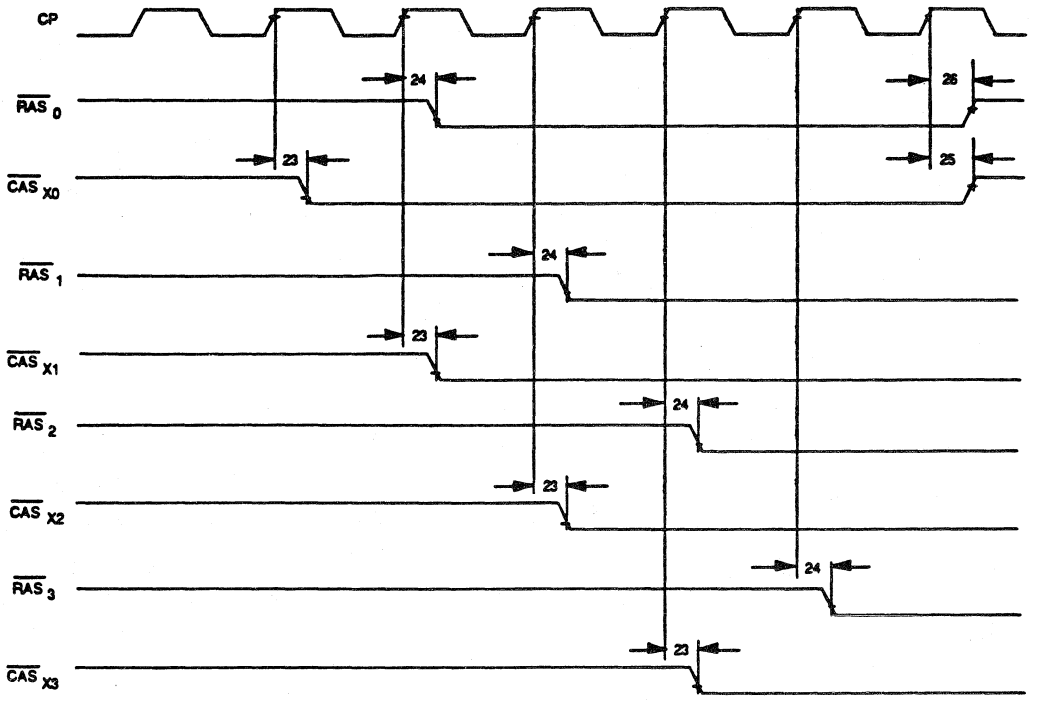
Waveform 1: Burst mode access timing



Waveform 2: Non-Burst mode access timing

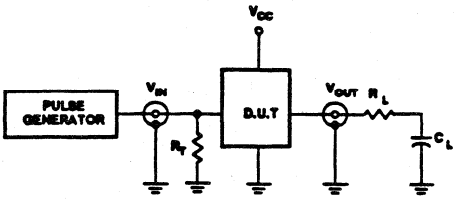


Waveform 3: Refresh cycle timing during $\overline{RAS}_0$ access

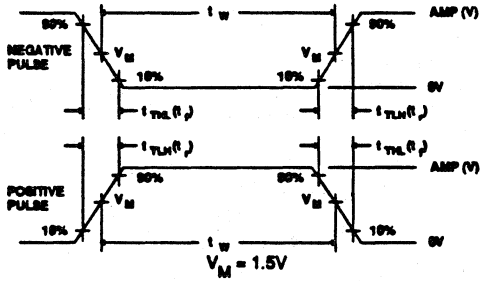


Waveform 4: Refresh cycle timing when memory is not being accessed

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

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FAST Products	

FAST 74F1779 Counter

8-Bit Bidirectional Binary Counter (3-state)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1779	130MHz	100mA

FEATURES

- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built-in look-ahead carry capability**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 145MHz typical**
- **Supply current 90mA typical**
- **See 'F269 for 24 pin separate I/O port version**
- **See 'F579 for 20 pin version**
- **See 'F779 for 16 pin version with abbreviated function table**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F1779N
16-Pin Plastic SOL[1]	N74F1779D

NOTE 1: Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70µA/0.6mA
	Data outputs	150/40	3.0mA/24mA
S_0, S_1	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

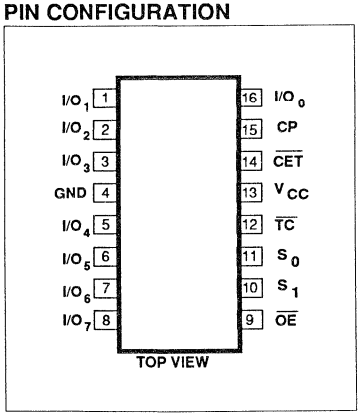
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

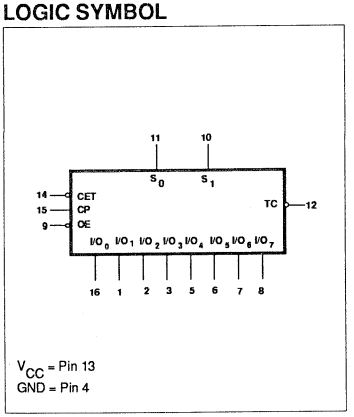
The 74F1779 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-state I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0,S_1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock. When $\overline{CET}$ is HIgh the data outputs are held in their current state and $\overline{TC}$ is held High. The $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

The 74F1779 differs from 74F779 in that it has an additional hold mode as described in the Function Table.

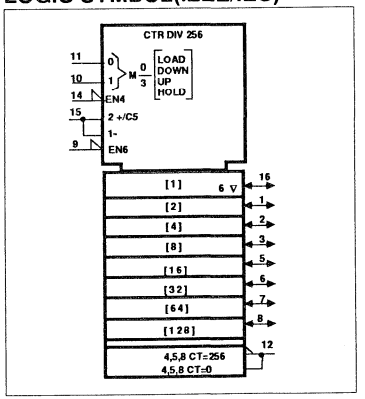
PIN CONFIGURATION



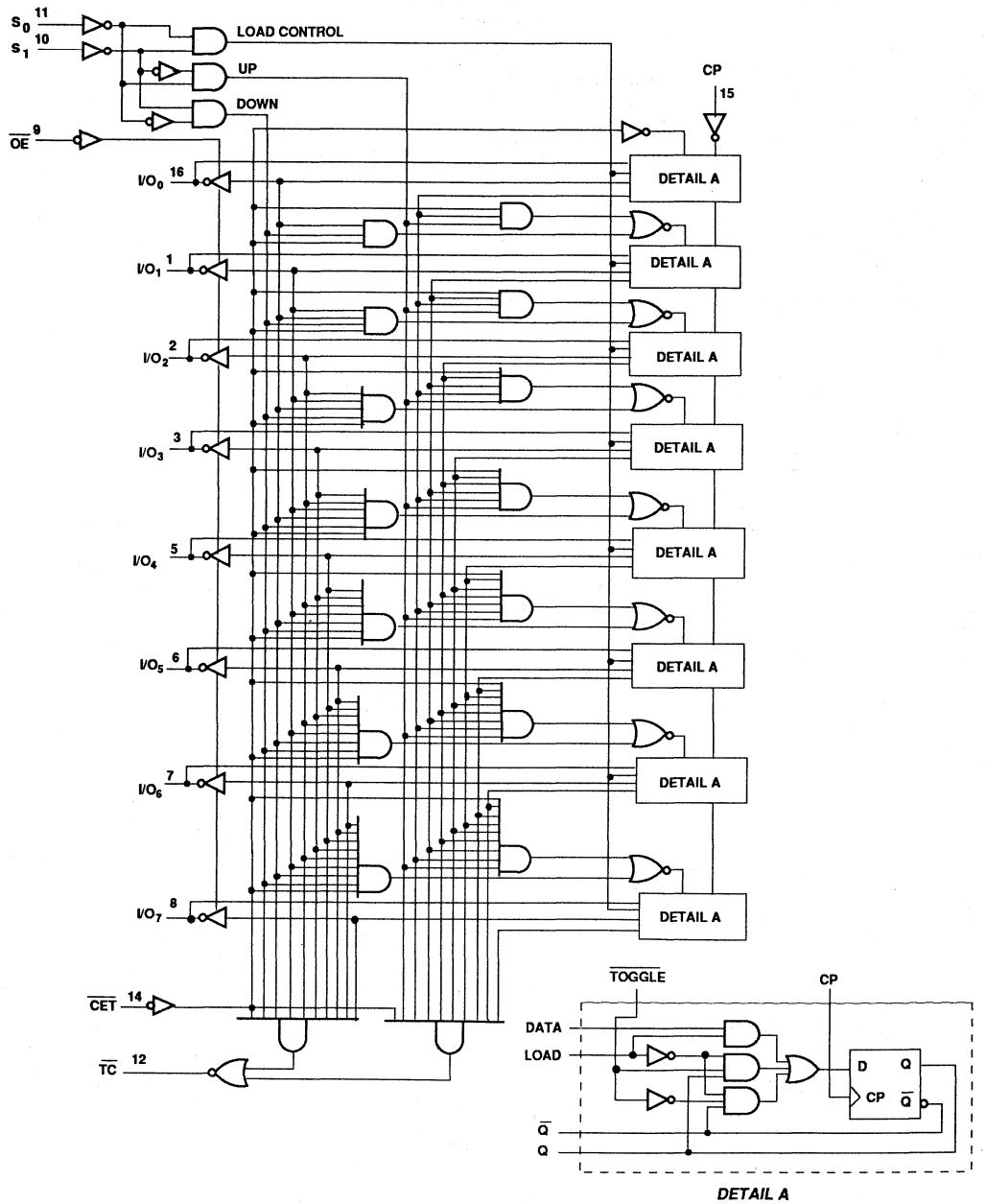
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 13
GND= pin 4

FUNCTION TABLE

INPUTS					OPERATING MODE
S_1	S_0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/O_0 to I/O_7 in high impedance
X	X	X	L	X	Flip-flop outputs appears on I/O lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held High)
H	H	X	X	↑	Hold
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = S_0 and S_1 should never be Low voltage level at the same time in the hold mode only.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
		others	V_{CC} = 5.5V, V_I =7.0V					100	µA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	I/O_n	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				100	145	mA
		I_{CCL}					100	145	mA
		I_{CCZ}					110	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

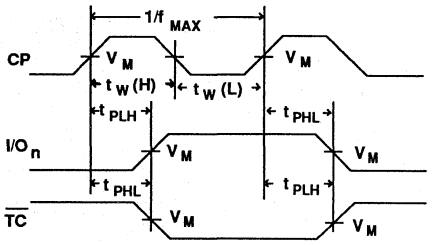
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	115	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 5.0	6.5 7.0	10.0 10.5	4.0 5.0	10.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.0 4.5	6.5 6.5	9.0 9.0	3.5 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	2.0 2.5	4.0 4.5	6.5 7.0	2.0 2.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low level	Waveform 4 Waveform 5	2.0 4.5	4.0 6.5	6.5 9.0	2.0 4.0	7.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.0 7.0	1.0 1.0	6.5 7.5	ns

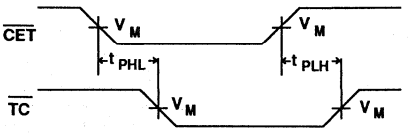
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	4.0 3.5			4.5 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ to CP	Waveform 3	4.5 7.0			5.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 3	7.5 8.5			8.0 9.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 4.5			3.0 5.5		ns

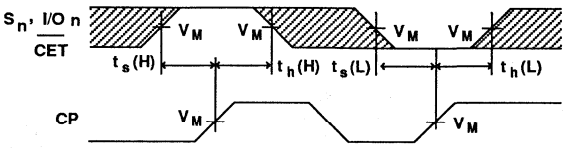
AC WAVEFORMS



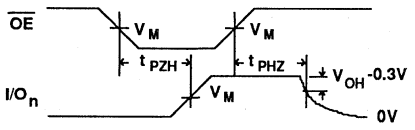
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



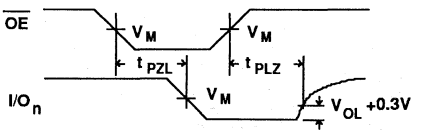
Waveform 2.
Propagation Delay, $\overline{CET}$ input to Terminal Count Output



Waveform 3. Data Setup And Hold Times



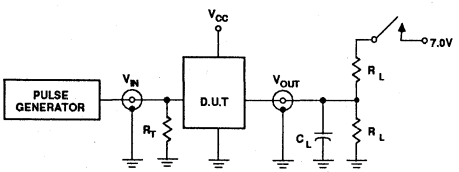
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



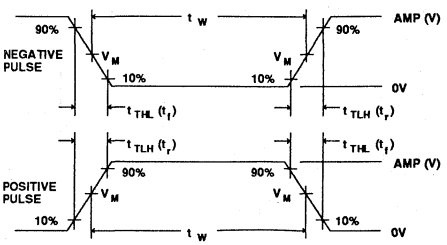
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal buffers — 74F2240/74F2241

74F2240 Octal inverter buffer (3-State) with 30Ω equivalent output termination
74F2241 Octal buffer (3-State) with 30Ω equivalent output termination

FEATURES

- Octal bus interface
- 30Ω output termination ideal for driving DRAM
- 15mA source current

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F2240	4.3ns	37mA
74F2241	4.5ns	30mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20-pin plastic DIP	N74F2240N, N74F2241N
20-pin plastic SOL	N74F2240D, N74F2241D

DESCRIPTION

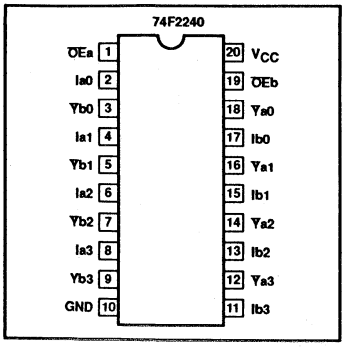
The 74F2240 and 74F2241 are octal buffers that are ideal for driving dynamic DRAM with impedance matching. The outputs are all capable of sinking 5mA and sourcing up to 15mA. The device features two output enables, each controlling four of the 3-state outputs.

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

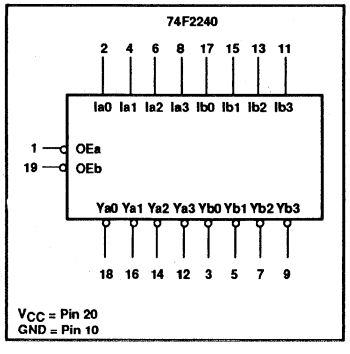
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/0.33	20µA/0.2mA
$\overline{OE}$a, $\overline{OE}$b	Output enable inputs (active low)	1.0/0.33	20µA/0.2mA
OEb	Output enable input (74F2241)	1.0/0.33	20µA/0.2mA
Yan, Ybn	Data outputs (74F2241)	750/8.33	15mA/5mA
$\overline{Y}$an, $\overline{Y}$bn	Data outputs (74F2240)	750/8.33	15mA/5mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

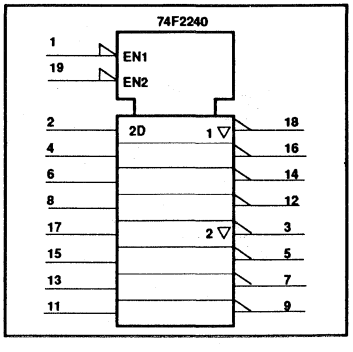
PIN CONFIGURATION



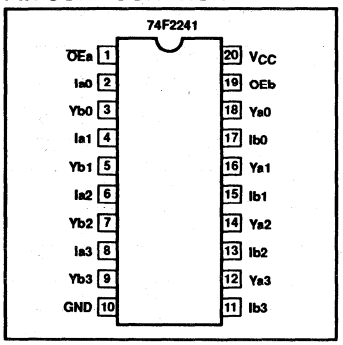
LOGIC SYMBOL



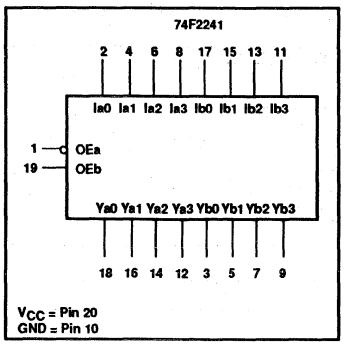
IEC/IEEE SYMBOL



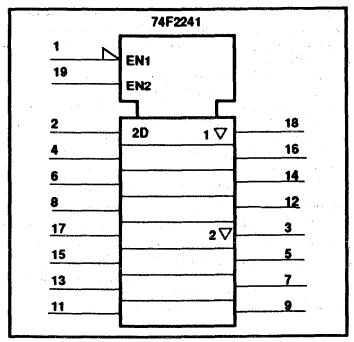
PIN CONFIGURATION



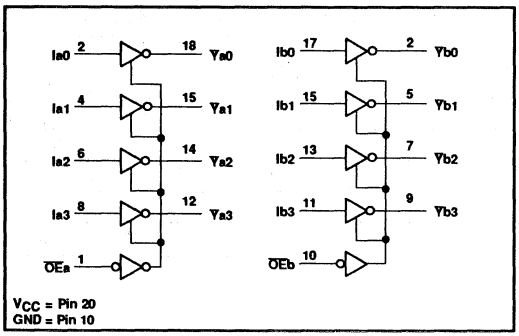
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM FOR 74F2240



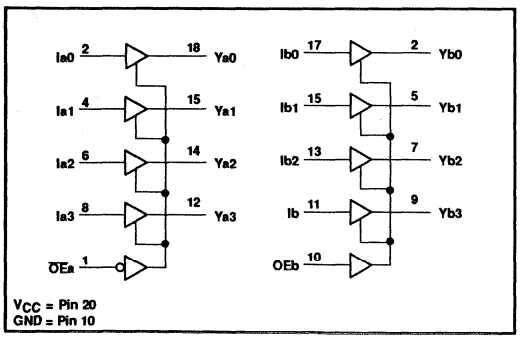
FUNCTION TABLE FOR 74F2240

INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	$\overline{OEb}$	Ib	$\overline{Ya}$	$\overline{Yb}$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

Notes to function table for 74F2240

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

LOGIC DIAGRAM FOR 74F2241



FUNCTION TABLE FOR 74F2241

INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

Notes to function table for 74F2241

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	10	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High–level output current			–15	mA
I_{OL}	Low–level output current			5	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH} = –15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = MAX	±10%V_{CC}			0.50	V
				±5%V_{CC}		0.42	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	V_{CC} = MAX, V_I = 0.5V					–0.2	mA
I_{OZH}	Off–state output current, high–level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied	V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short–circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	74F2240	I_{CCH}	V_{CC} = MAX		25	35	mA
			I_{CCL}			53	75	mA
			I_{CCZ}			35	45	mA
		74F2241	I_{CCH}	V_{CC} = MAX		19	30	mA
			I_{CCL}			45	65	mA
			I_{CCZ}			27	40	mA

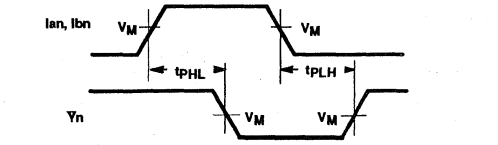
NOTES:

3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
4. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

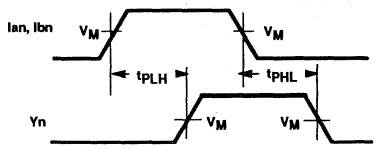
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to $\overline{Y}$n	74F2240	Waveform 1	3.0 2.0	5.0 3.5	7.0 5.5	2.5 2.0	8.0 6.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	74F2240	Waveform 3 Waveform 4	3.0 3.5	4.5 5.0	7.0 8.0	2.5 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	74F2240	Waveform 3 Waveform 4	2.0 1.0	3.5 2.5	6.5 5.5	1.5 1.0	7.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	74F2241	Waveform 2	3.0 2.5	4.5 4.5	7.0 6.5	2.5 2.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	74F2241	Waveform 3 Waveform 4	3.0 3.5	5.0 5.5	7.0 7.5	2.0 3.0	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	74F2241	Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	6.0 6.0	1.5 1.0	7.0 6.5	ns

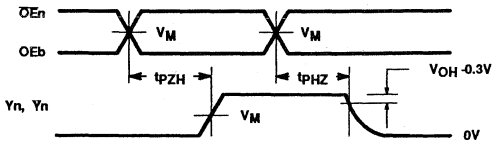
AC WAVEFORMS



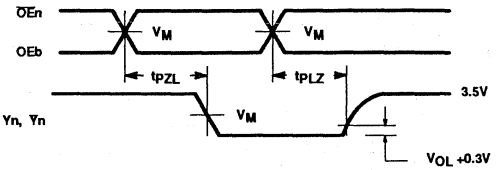
Waveform 1. Propagation delay for inverting outputs



Waveform 2. Propagation delay for non–invertng outputs



Waveform 3. 3-state eoutput enable time to high level and output disable time from high level



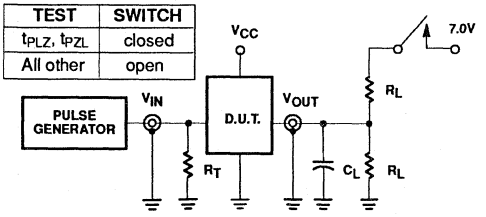
Waveform 4. 3-state output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



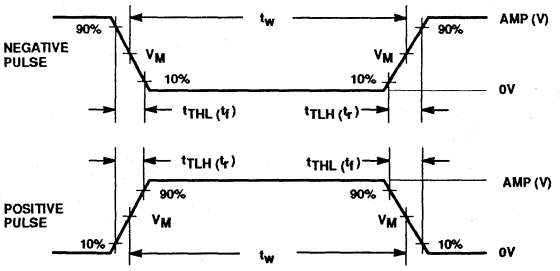
Test circuit for 3–state outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Octal buffer with 30Ω equivalent output termination (3-State) 74F2244

FEATURES

- Octal bus interface
- 30Ω output termination ideal for driving DRAM
- 15mA source current

DESCRIPTION

The 74F2244 is an octal buffer that is ideal for driving dynamic DRAM with matching impedance. The outputs are all capable of sinking 5mA and sourcing up to 15mA. The device features two output enables, $\overline{OE}a$ and $\overline{OE}b$, each controlling four of the 3–state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F2244	4.0ns	30mA

ORDERING INFORMATION

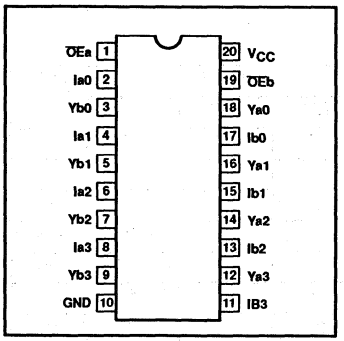
DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20-pin plastic DIP	N74F2244N
20-pin plastic SOL	N74F2244D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

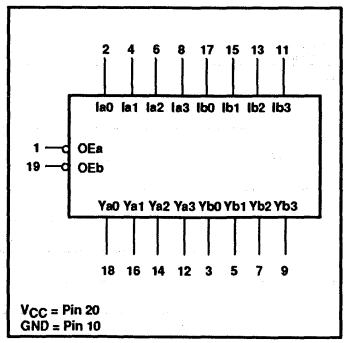
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/0.33	20µA/0.2mA
$\overline{OE}a$, $\overline{OE}b$	Output enable inputs (active low)	1.0/0.33	20µA/0.2mA
Yan, Ybn	Data outputs	750/8.33	15mA/5mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

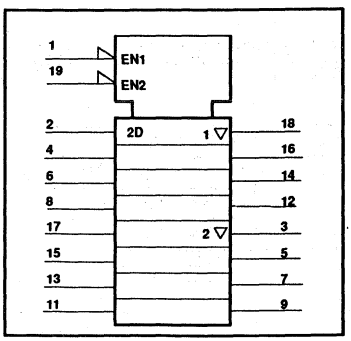
PIN CONFIGURATION



LOGIC SYMBOL

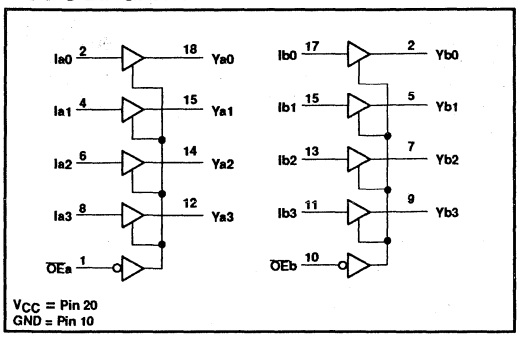


IEC/IEEE SYMBOL



Octal buffer with 30Ω equivalent output termination (3-State) 74F2244

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	Ya	Yb
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

Notes to function table
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	10	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–15	mA
I_{OL}	Low–level output current			5	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH} = –15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = MAX	±10%V_{CC}			0.50	V
				±5%V_{CC}		0.42	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	V_{CC} = MAX, V_I = 0.5V					–0.2	mA
I_{OZH}	Off–state output current, high–level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied	V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short–circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			20	30	mA
		I_{CCL}				45	65	mA
		I_{CCZ}				26	40	mA

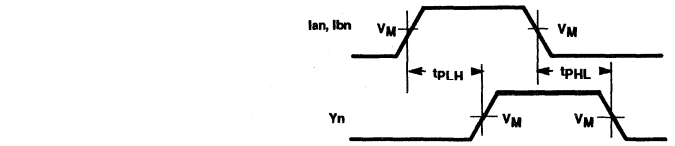
NOTES:

3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
4. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

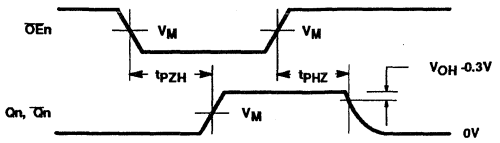
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	Waveform 1	3.0 2.5	4.5 4.5	7.0 7.0	2.5 2.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	Waveform 2 Waveform 3	2.5 3.0	4.5 5.0	7.5 8.0	2.0 3.0	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 2 Waveform 3	1.5 1.5	3.5 2.5	6.0 5.5	1.0 1.0	6.0 5.5	ns

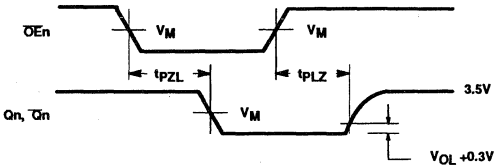
AC WAVEFORMS



Waveform 1. Propagation delay for data to outputs



Waveform 2. 3-state eoutput enable time to high level and output disable time from high level



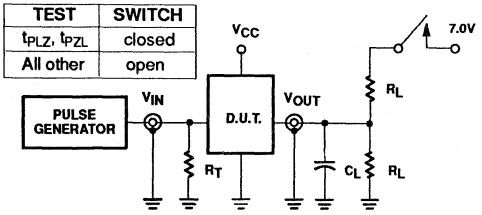
Waveform 3. 3-state output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



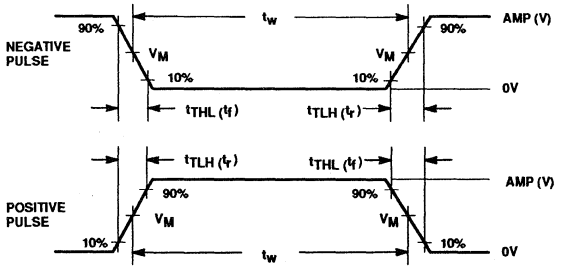
Test circuit for 3–state outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-1097
ECN No.	97708
Date of issue	September 22, 1989
Status	Product Specification
FAST Products	

FAST 74F2952, 74F2953 Transceivers

74F2952 Registered Transceiver, Non-Inverting (3-State)
74F2953 Registered Transceiver, Inverting (3-State)

FEATURES

- **8-bit Registered Transceivers**
- **Two 8-bit , back-to-back registers store data moving in both directions between two bidirectional busses**
- **Separate Clock, Clock Enable and 3-state Enable provided for each register**
- **'F2952 Non-inverting 'F2953 Inverting**
- **AM2952/2953 functional equivalent**
- **A outputs sink 24mA and source 3mA**
- **B outputs sink 64mA and source 15mA**
- **300 mil wide 24-pin Slim DIP package**

DESCRIPTION

The 74F2952 and 74F2953 are 8-bit Registered Transceivers. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-state output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F2952	160MHz	105mA
74F2953	160MHz	105mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F2952N, N74F2953N
24-Pin Plastic SOL[1]	N74F2952D, N74F2953D
28-Pin Plastic PLCC	N74F2952A, N74F2953A

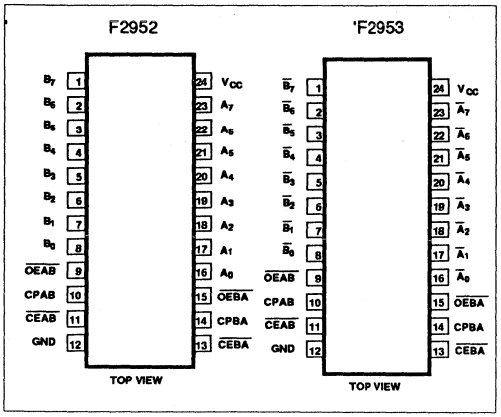
NOTE:
1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

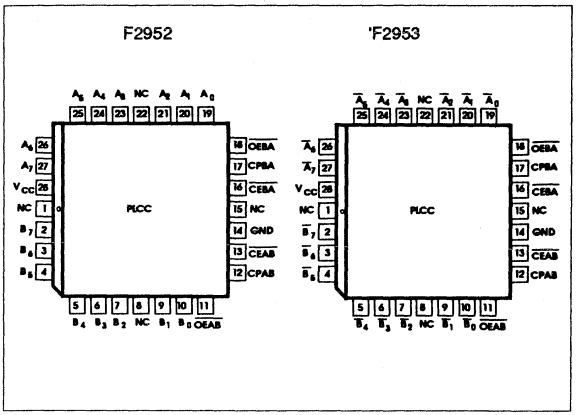
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	Port A, 3-state inputs	3.5/1.0	70µA/0.6mA
B_0 - B_7	Port B, 3-state inputs	3.5/1.0	70µA/0.6mA
CPAB,CPBA	Clock inputs	1.0/1.0	20µA/0.6mA
$\overline{CEAB}$,$\overline{CEBA}$	Clock Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{OEAB}$,$\overline{OEBA}$	Output Enable inputs	1.0/1.0	20µA/0.6mA
A_0 - A_7	Port A, 3-state outputs	150/40	3.0mA/24mA
B_0 - B_7	Port B, 3-state outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

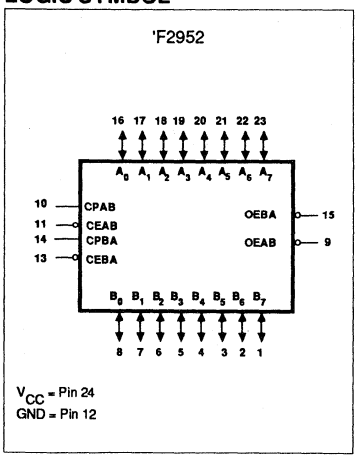
PIN CONFIGURATION DIP



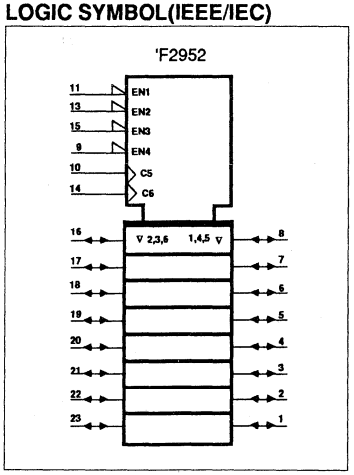
PIN CONFIGURATION PLCC



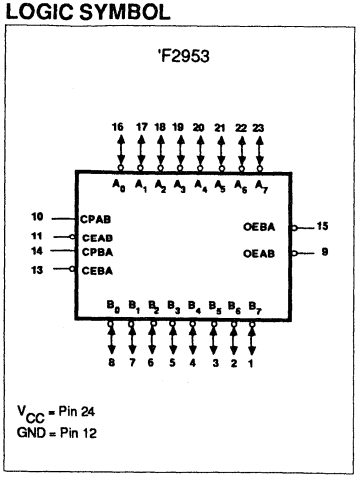
LOGIC SYMBOL



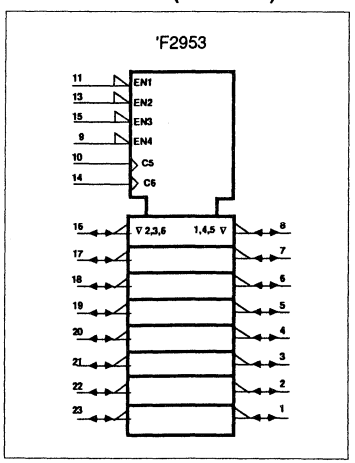
LOGIC SYMBOL(IEEE/IEC)



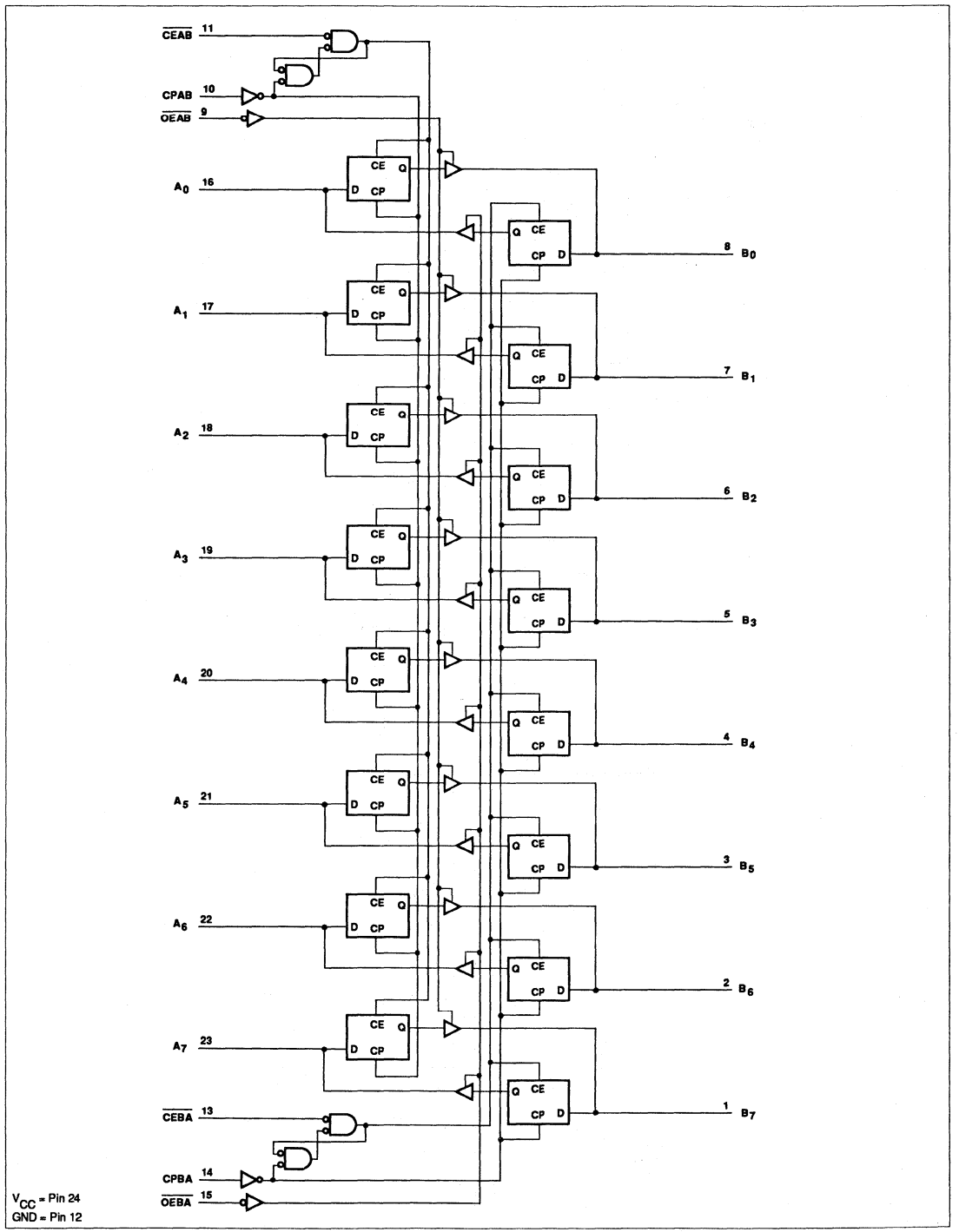
LOGIC SYMBOL



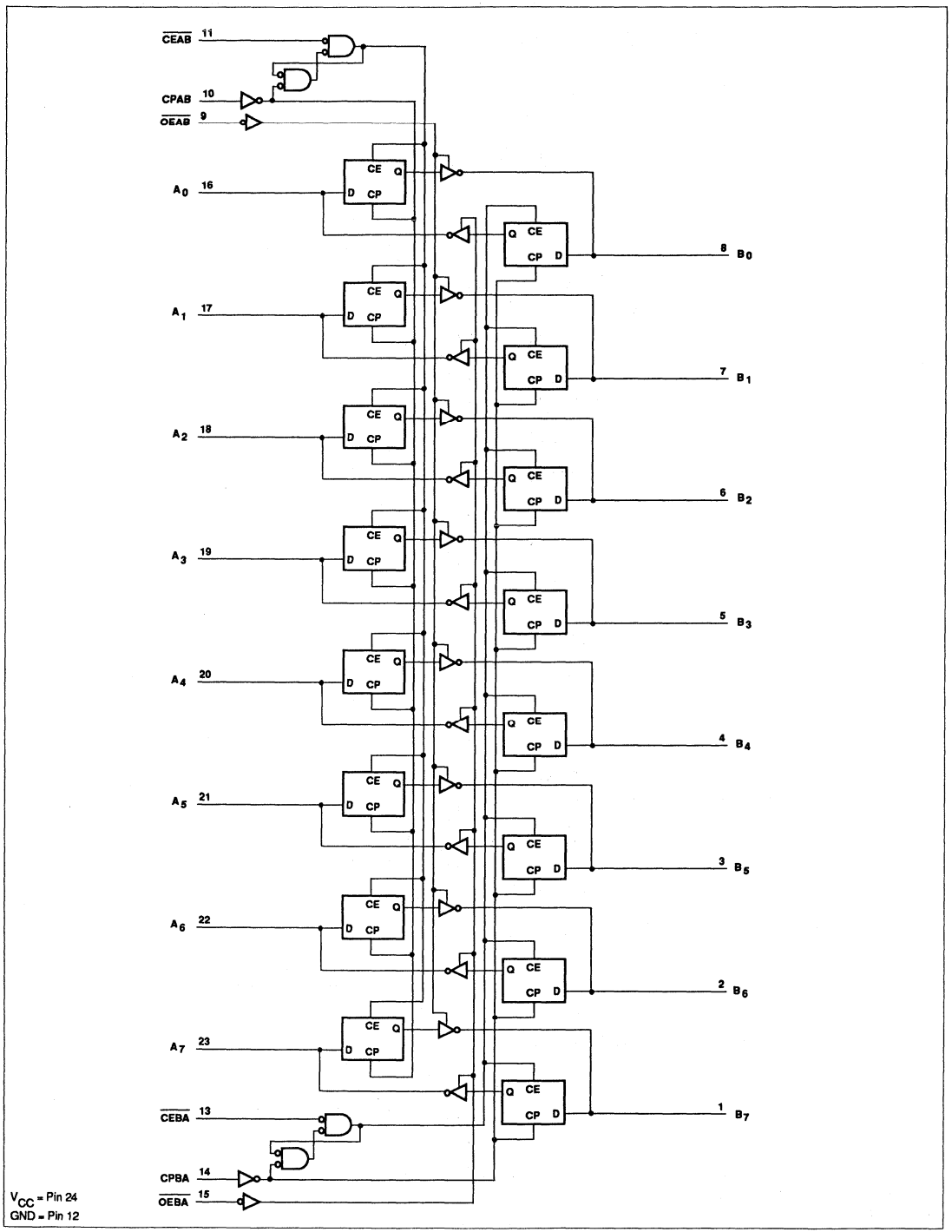
LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM for 'F2952



LOGIC DIAGRAM for 'F2953



FUNCTION TABLE for Register A_n or B_n

INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

H= High voltage level
L= Low voltage level
↑ =Low-to-High transition
X=Don't care
XX=AB or BA
NC=No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	A_n or B_n OUTPUTS		OPERATING MODE
$\overline{OEXX}$		'F2952	'F2953	
H	X	Z	Z	Disable outputs
L	L	L	H	Enable outputs
L	H	H	L	

H= High voltage level
L= Low voltage level
X=Don't care
XX=AB or BA
Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{CPAB}$, $\overline{CPBA}$, $\overline{OEAB}$ $\overline{OEBA}$,$\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{CPAB}$, $\overline{CPBA}$, $\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O = 0.5V					-600	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX, V_O=0.00V			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	140	mA
		I_{CCL}					120	175	mA
		I_{CCZ}					105	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

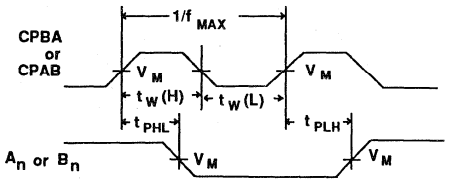
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	145	160		135		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to A_n or B_n	Waveform 1	3.0 3.5	5.0 6.0	7.5 8.5	2.5 3.5	8.0 9.0	ns
t_{PZH} t_{PZH}	Output Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 3 Waveform 4	2.0 3.5	4.5 6.0	7.0 9.5	2.0 3.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	8.0 6.5	1.5 1.0	9.0 7.0	ns

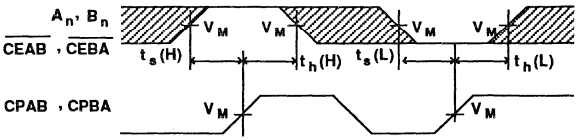
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	'F2952	Waveform 2	4.5 3.5			5.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	'F2953	Waveform 2	4.0 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA		Waveform 2	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEAB}$,$\overline{CEBA}$ to CPAB , CPBA		Waveform 2	0.0 4.0			0.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEAB}$,$\overline{CEBA}$ to CPAB , CPBA		Waveform 2	2.5 2.5			2.5 3.0		ns
$t_w(H)$ $t_w(L)$	CPAB or CPBA Pulse width, High or Low		Waveform 1	3.0 3.5			3.0 3.5		ns

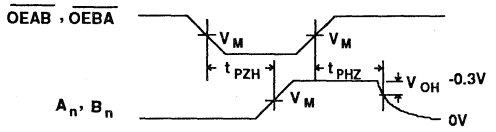
AC WAVEFORMS



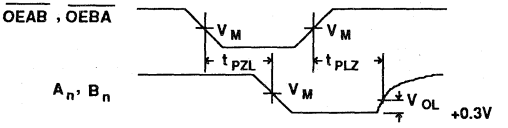
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup And Hold Times



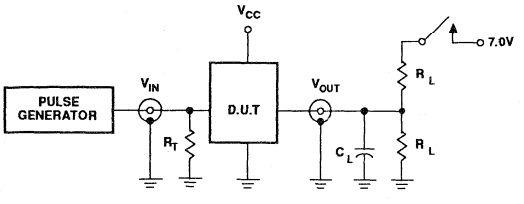
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



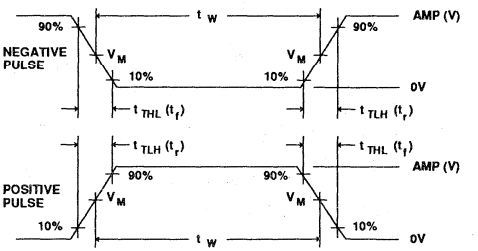
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Quad 2-input NAND 30Ω driver | 74F3037

FEATURES

- 30Ω line driver
- 67mA output drive capability in the high state
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V_{CC} and GND when both side pins are used
- 160mA output drive capability in the low state
- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F3037	2.0ns	16mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
16–pin plastic DIP	N74F3037N	I74F3037N
16–pin plastic SOL[1]	N74F3037D	I74F3037D

Note to ordering information

1. Thermal mounting techniques are recommended. See SMD Applications (page 17) for a discussion for surface mounted devices. If driving impedances 42 ohms or greater then thermal mounting is not necessary.

DESCRIPTION

The 74F3037 is a high current line driver composed of four 2–input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 74F3037 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8mA while driving impedances as low as 30 ohms. This is applicable with any combination of outputs using continuous duty. The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performances may be improved by full or partial line termination.

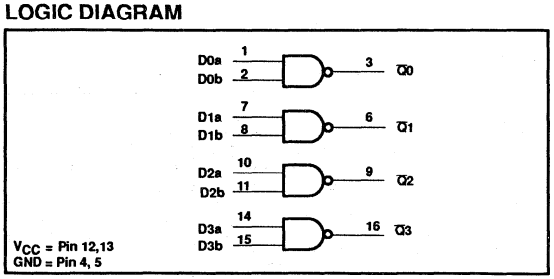
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}n$	Data output	3350/266	67mA/160mA

Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM



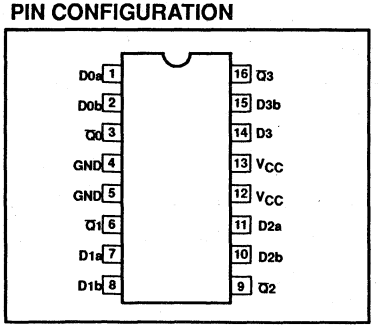
FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}n$
L	L	H
L	H	H
H	L	H
H	H	L

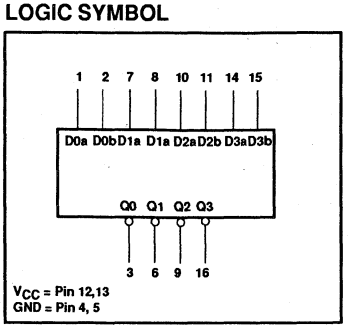
Notes to function table

1. H = High voltage level
2. L = Low voltage level

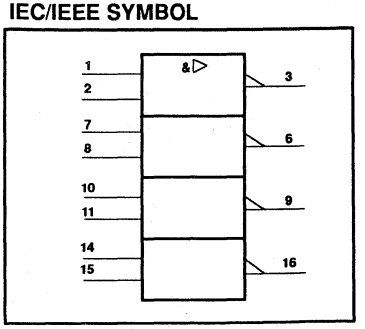
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		320	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.4			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–67	mA
I_{OL}	Low–level output current				160	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial rtange	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN,	I_{OH} = –45mA	±10%V_{CC}	2.5			V
			V_{IL} = MAX,		±5%V_{CC}	2.7			V
			V_{IH} = MIN	I_{OH1} = –67mA[3]	±10%V_{CC}	2.0			V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = 100mA	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN	I_{OL1} = 160mA[4]	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]		V_{CC} = MAX, V_O = 2.25V			-100		-200	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				6.0	9.0	mA
		I_{CCL}					30	40	mA

Notes to DC electrical characteristics

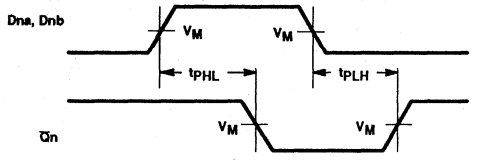
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. I_{OH1} is the current necessary to guarantee the low to high transition in a 30 ohm transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the high to low transition in a 30 ohm transmission line on the incident wave.

5. I_O is tested under conditions that produce current approximately one half of the true short-circuit current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	1.0 1.0	2.0 2.0	5.0 4.5	1.0 1.0	5.5 5.0	1.0 1.0	5.5 5.0	ns

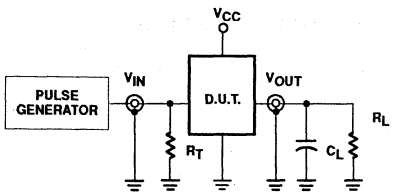
AC WAVEFORMS



Waveform 1. Propagation delay for inverting outputs

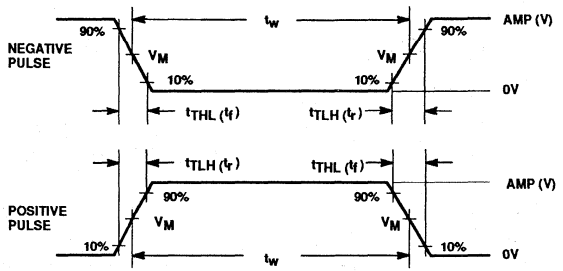
Note to AC waveforms
1. For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs

DEFINITIONS:
R_L = Load resistor;
see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0022
ECN No.	98644
Date of issue	January 29, 1990
Status	Product
FAST Products	

FAST 74F3038
30Ω Line Driver

Quad Two-Input NAND 30Ω Line Driver (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3038	6.0 ns	17 mA

FEATURES

- **30Ω line driver**
- **160mA output drive capability**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

DESCRIPTION

The 74F3038 is a high current Open-Collector Line Driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The 74F 3038 can sink 160mA with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OL} not more than 0.8V while driving impedances as low as 30 ohm. This is applicable with any combination of outputs using continuous duty.

The AC specifications for the 74F3038 were determined using the standard FAST load for open-collector parts of 50 pf capacitance, a 500 ohm pull-up resistor and a 500 ohm pull-down resistor. (See Test Circuit).

Reducing the load resistors to 100 ohm will decrease the t_{PLH} propagation delay by approximately 50 % while increasing t_{PHL} only slightly. The graph of typical propagation delay vs load resistor (See AC Characteristics section for Graph) shows a spline fit curve from four measured data points. R_L=30 ohm, R_L=100 ohm, R_L=300 ohm, and R_L=500 ohm.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	74F3038N
16-Pin Plastic SOL[1]	74F3038D

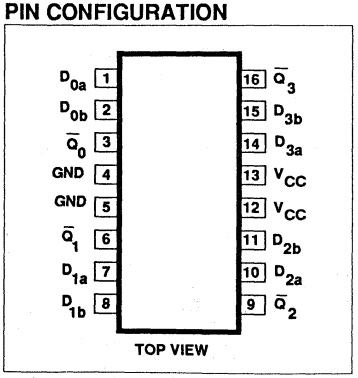
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices. If driving impedances 42 ohms or greater then thermal mounting is not necessary.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_n$	Data outputs	OC/266	OC/160mA

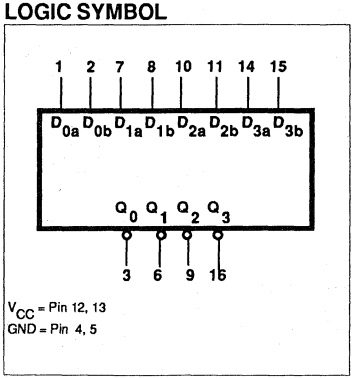
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

PIN CONFIGURATION

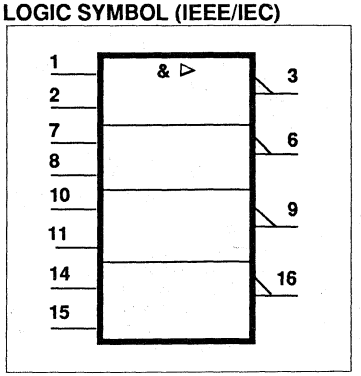


TOP VIEW

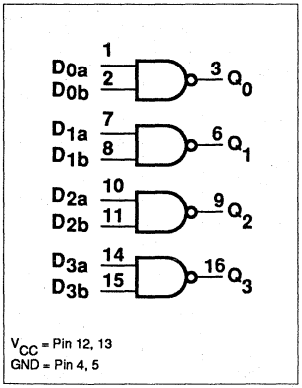
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

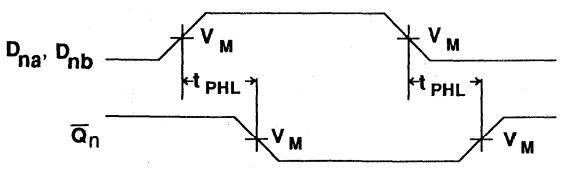
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		.42	.55	V
				I_{OL} = 160mA[3]	±5%V_{CC}			.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current [total]	I_{CCH}	V_{CC} = MAX		V_{IN} =GND		3.5	6.0	mA
		I_{CCL}			V_{IN} = 4.5V		30	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH}	Propagation delay	Waveform 1	6.0	8.5	11.5	6.0	12.0	ns
t_{PHL}	D_{na}, D_{nb} to $\overline{Q}_n$		1.0	2.0	5.0	1.0	5.0	

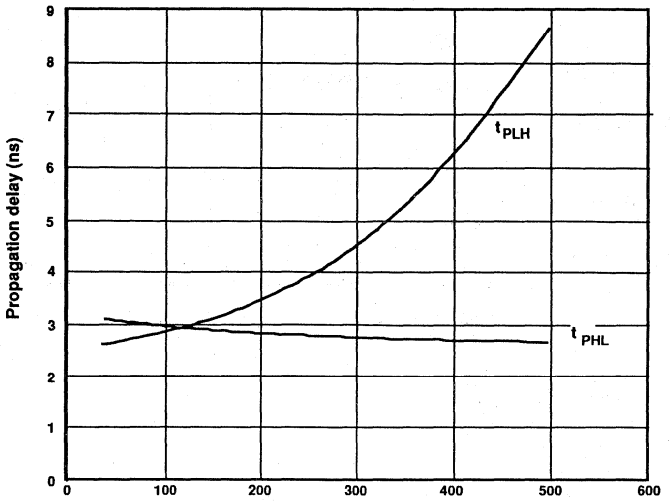
AC WAVEFORMS



Waveform 1.Propagation Delay for Inputs to Output

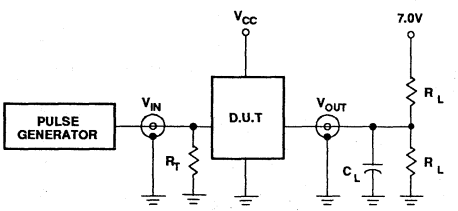
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



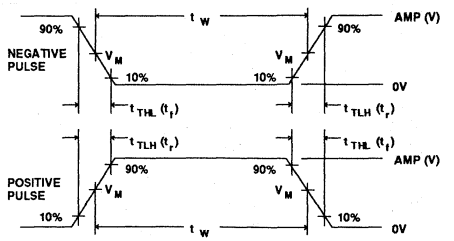
Test Circuit For Open Collector Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-0023
ECN No.	98639
Date of issue	January 29, 1990
Status	Product
FAST Products	

FAST 74F3040
30Ω Line Driver

Dual 4-Input NAND 30Ω Line Driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3040	2.0 ns	10 mA

FEATURES

- **30Ω line driver**
- **160mA output drive capability in the Low state**
- **67mA output drive capability in the High state**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

DESCRIPTION

The 74F3040 is a high current Line Driver composed of two 4-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 'F3040 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30 ohms. This is applicable with any combination of outputs using continuous duty. The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices, Performance may be improved by full or partial line termination.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F3040N
16-Pin Plastic SOL[1]	N74F3040D

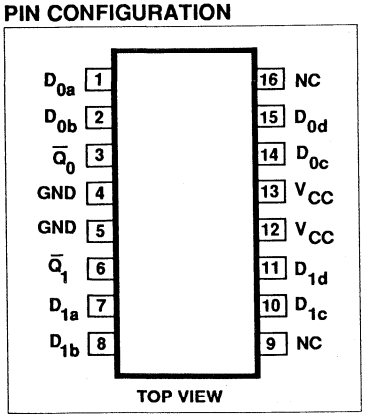
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices. If driving impedances 42 ohms or greater then thermal mounting is not necessary.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

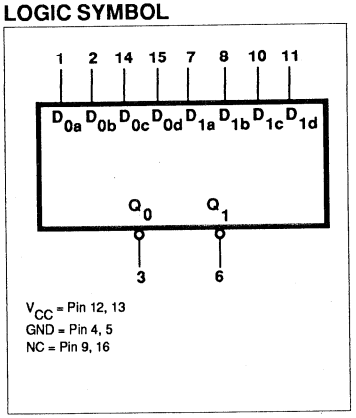
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_n$	Data output	3350/266	67mA/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

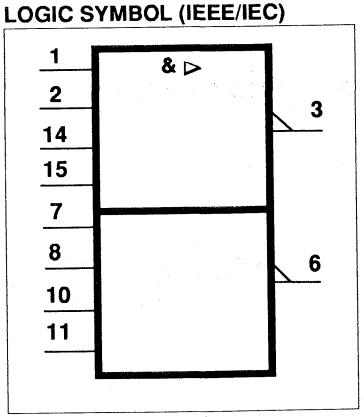
PIN CONFIGURATION



LOGIC SYMBOL

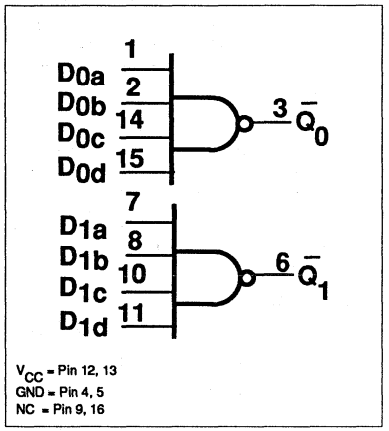


LOGIC SYMBOL (IEEE/IEC)



30Ω Line Driver | FAST 74F3040

LOGIC DIAGRAM



V_{CC} = Pin 12, 13
GND = Pin 4, 5
NC = Pin 9, 16

FUNCTION TABLE

INPUTS				OUTPUT
D_{na}	D_{nb}	D_{nc}	D_{nd}	$\overline{Q}_n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't carre

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-67	mA
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

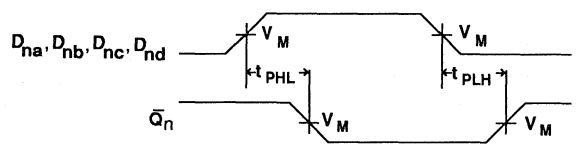
SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -45mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH1} = -67mA[3]	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.30	0.50	V
			I_{OL1} = 160mA[4]	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]	V_{CC} = MAX, V_O = 2.25V			-100		-200	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			3.0	5.0	mA
		I_{CCL}				16	22	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the Low to High transition in a 30 ohm transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30 ohm transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to $\overline{Q}_n$	Waveform 1	1.0 1.0	2.0 2.0	5.0 4.5	1.0 1.0	5.5 5.0	ns

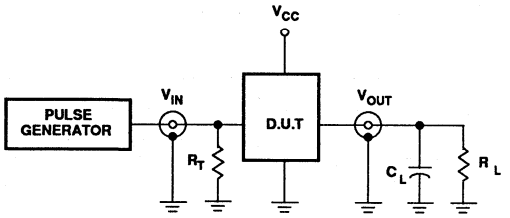
AC WAVEFORMS



Waveform 1. Propagation Delay for Inputs to Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



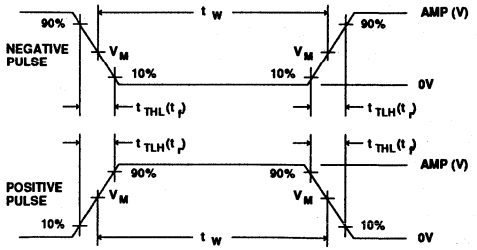
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Quad futurebus backplane transceiver — FAST 74F3893

FEATURES

- Quad backplane transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- Futurebus drivers sink 100mA
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE 896 and IEEE 1194.1 Futurebus Standards
- Built–in precision band–gap (BG) reference provides accurate receiver thresholds and improved noise immunity
- Glitch–free power up/power down operation on all outputs
- Pin and function compatible with NSC DS3893

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F3893	3.0ns	55mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20–pin PLCC	N74F3893A

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE
D0 – D3	Data inputs	1.0/0.067	20µA/40µA
DE	Data enable input	1.0/0.33	20µA/200µA
$\overline{RE}$	Receiver enable input	1.0/0.067	20µA/40µA
I/O0 – I/O3	Bus inputs	5.0/0.033	100µA/20µA
I/O0 – I/O3	Bus outputs	OC/166.7	OC/100mA
R0 – R7	Receiver outputs	150/40	3mA/24mA

Notes to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.
2. OC= Open collector.

DESCRIPTION

The 74F3893 is a quad backplane transceivers and is intended to be used in very high speed bus systems.

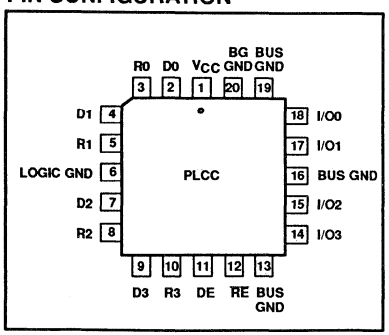
The 74F3893 interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (< 5pF).

Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

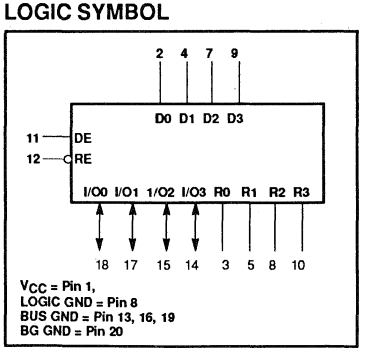
BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F3893 has four TTL outputs (Rn) on the receiver side with a common receiver enable input ($\overline{RE}$). It has four data inputs (Dn) which are also TTL. These data inputs are NANDed with the data enable input (DE). The four I/O pins (bus side) are futurebus compatible, sink a minimum of 100mA, and are designed to drive heavily loaded backplanes with load impedances as low as 10 ohms. All outputs are designed to be glitch–free during power up and down.

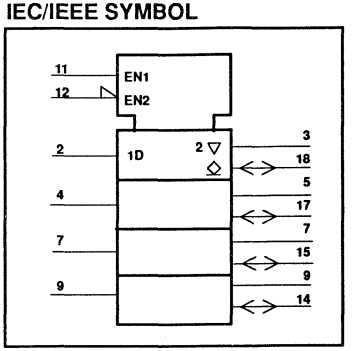
PIN CONFIGURATION



LOGIC SYMBOL

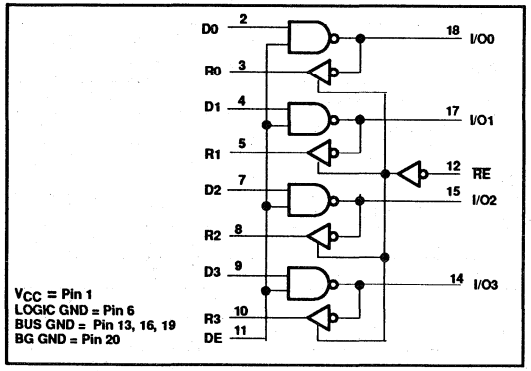


IEC/IEEE SYMBOL



Quad futurebus backplane transceiver | FAST 74F3893

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INPUT/ OUTPUT	OUTPUT	OPERATING MODE
$\overline{DE}$	$\overline{RE}$	Dn	I/On	Rn	
H	L	L	H	L	Transmit to bus
H	L	H	L	H	
H	H	Dn	$\overline{Dn}$	Z	Receiver 3–state,
L	H	X	H	Z	transmit to bus
L	L	X	H	L	Receive, I/On = inputs
L	L	X	L	H	

Notes to function table
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–1.5 to +6.5	V
V_{IN}	Input voltage	–1.5 to +6.5	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to 5.5	V
I_{OUT}	Current applied to output in low output state	200	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Dn, DE, $\overline{RE}$	2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
V_{TH}	Bus input threshold	I/On only	1.475	1.55	1.625	mA
I_{OH}	High–level output current	Rn only			–3	mA
I_{OL}	Low–level output current				100	mA
T_{amb}	Operating free air temperature		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
I_{OH}	High–level output current	I/On	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.5V			10	100	µA
V_{OH}	High-level output voltage	Rn	V_{CC} = MAX, V_{IL} = 1.3V, $\overline{RE}$ = 0.8V, I_{OH} = MAX		2.5			V
V_{OHB}	High-level output bus voltage	I/On	V_{CC} = MAX, Dn = DE = 0.8V, V_T = 2.0V, R_T = 10Ω, $\overline{RE}$ = 2.0V		2.5			V
V_{OL}	Low-level output voltage	Rn	V_{CC} = MIN, V_{IN} = 1.8V, $\overline{RE}$ = 0.8V, I_{OL} = 6mA			0.35	0.5	V
V_{OLB}	Low-level output bus voltage	I/On	Dn = DE = V_{IH}, I_{OL} = 100mA		0.75	1.0	1.2	V
			Dn = DE = V_{IH}, I_{OL} = 80mA		0.75	1.0	1.1	V
V_{OCB}	Driver output positive clamp voltage	I/On	V_{CC} = MAX or 0V, Dn = DE = 0.8V, $\overline{RE}$ = 2.0V	I/On = 1mA	1.9		2.9	V
				I/On = 10mA	2.3		3.2	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V, DE = $\overline{RE}$ = Dn = V_{CC}				100	µA
I_{IH}	High–level input current	Dn, $\overline{RE}$, DE	V_{CC} = MAX, DE = $\overline{RE}$ = Dn =5.5V				20	µA
I_{IHB}	High–level I/O bus current (power off)	I/On	V_{CC} = 0V, Dn = DE = 0.8V, I/On =1.2V, $\overline{RE}$ = 0V				100	µA
I_{IL}	Low–level input current	Dn, $\overline{RE}$	V_{CC} = MAX, V_I = 0.5V, DE = 4.5V				–40	µA
		DE	V_{CC} = MAX, V_I = 0.5V, Dn = 4.5V				–200	µA
I_{ILB}	Low–level I/O bus current (power on)	I/On	V_{CC} = MAX, Dn = DE = 0.8V, I/On =0.75V, $\overline{RE}$ = 0V		–20		20	µA
I_{OZH}	Off–state output current, high–level voltage applied	Rn	V_{CC} = MAX, V_I = 2.7V, $\overline{RE}$ = 2V				20	µA
I_{OZL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V, $\overline{RE}$ = 2V				–20	µA
I_{OS}	Short circuit output current[3]	Rn	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX, ($\overline{RE}$ = V_{IH} or V_{IL})			55	80	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR DRIVER AND DRIVER ENABLE

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_D = 50pF, R_T = 10Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D = 50pF, R_T = 10Ω MIN	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to I/On	Waveform 1	1.0 1.5	2.0 3.0	5.0 5.5	1.0 1.5	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay DE to I/On	Waveform 1	1.0 1.5	2.0 3.0	4.5 5.5	1.0 1.5	5.5 6.0	ns
t_{TLH} t_{THL}	Dn to I/O transition time 10% to 90%, 90% to 10%	Waveform 1	1.0 1.0		4.0 4.0	1.0 1.0	5.0 5.0	ns
$t_{sk(o)}$	Skew between drivers in same package			1.0				ns

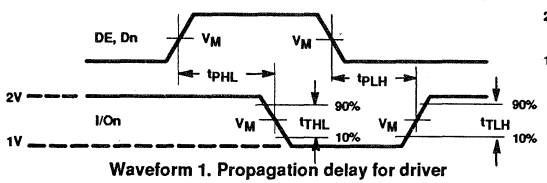
AC ELECTRICAL CHARACTERISTICS FOR RECEIVER

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 1kΩ			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 1kΩ		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay I/On to Rn	Waveform 2	1.0 3.6	2.0 5.5	4.5 7.5	1.0 3.6	5.5 8.5	ns

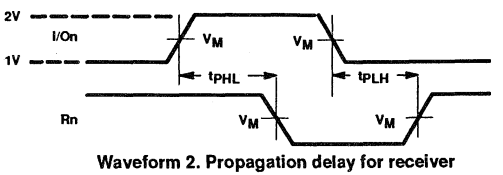
AC ELECTRICAL CHARACTERISTICS FOR RECEIVER ENABLE

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PZH} t_{PZL}	Output enable time to high or low level, $\overline{RE}$ to Rn	Waveform 3, 4	1.5 2.5	3.0 4.0	5.5 7.0	1.5 2.0	6.0 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level, $\overline{RE}$ to Rn	Waveform 3, 4	1.5 1.5	3.0 3.0	5.5 5.5	1.0 1.0	6.5 6.0	ns

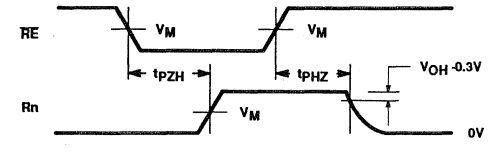
AC WAVEFORMS



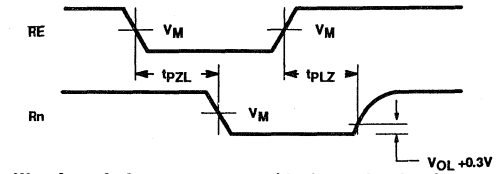
Waveform 1. Propagation delay for driver



Waveform 2. Propagation delay for receiver



Waveform 3. 3–state output enable time to high level and output disable time from high level



Waveform 4. 3-state output enable time to low level and output disable time from low level

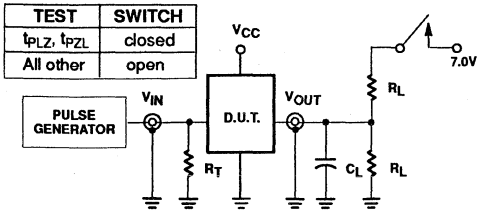
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

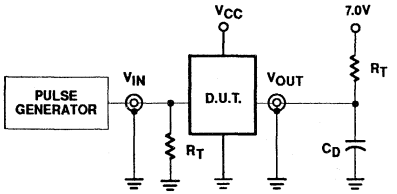
TEST CIRCUITS AND WAVEFORMS

SWITCH POSITION

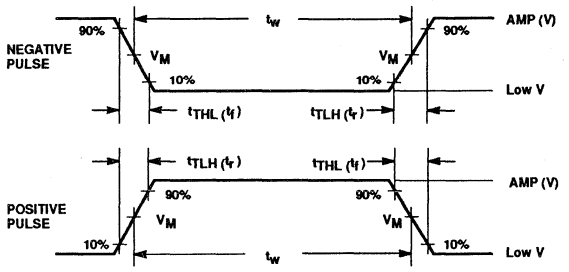
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–state outputs on D port



Test circuit for outputs on I/O port



Input pulse definition

family	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
D port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
I/O port	2.0V	1.0V	1.5V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_U = Pull up resistor; see AC Electrical Characteristics for value.
C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Synchronizing dual D-type flip-flop/clock driver — 74F5074

FEATURES

- Metastable immune characteristics
- Output skew guaranteed less than 1.5ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- Pin out compatible with 74F74
- 74F50728 for synchronizing cascaded D–type flip–flop
- See 74F50729 for synchronizing dual D–type flip–flop with edge–triggered set and reset
- See 74F50109 for synchronizing dual J–$\overline{K}$ positive edge–triggered flip–flop
- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F5074	120MHz	20mA

ORDERING INFORMATION

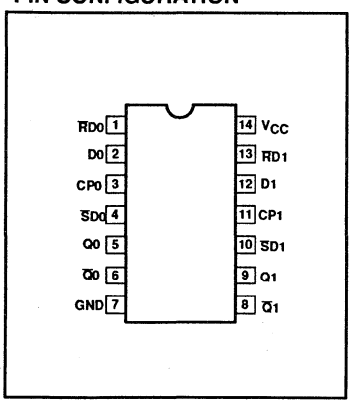
DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
14–pin plastic DIP	N74F5074N
14–pin plastic SO	N74F5074D

INPUT AND OUTPUT LOADNG AND FAN OUT TABLE

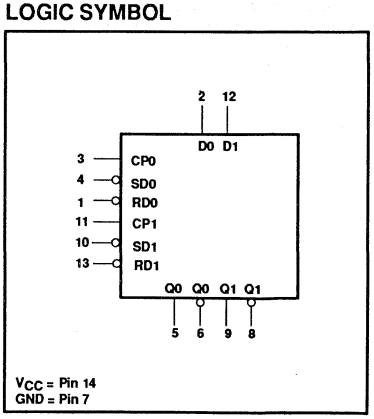
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
D0, D1	Data inputs	1.0/0.417	20µA/250µA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/20µA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active low)	1.0/1.0	20µA/20µA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active low)	1.0/1.0	20µA/20µA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	750/33	15mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

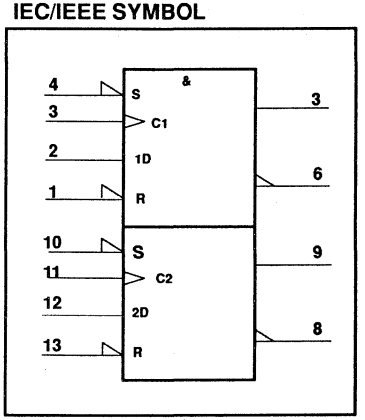
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



Synchronizing dual D-type flip-flop/clock driver | 74F5074

DESCRIPTION

The 74F5074 is a dual positive edge–triggered D–type featuring individual data, clock, set and reset inputs; also true and complementary outputs.

Set ($\overline{S}$Dn) and reset ($\overline{R}$Dn) are asynchronous active low inputs and operate independently of the clock (CPn) input. Data must be stable just one setup time prior to the low–to–high transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive–going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output.

The 74F5074 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F5074 are: $\tau \cong 135$ps and $T_o \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

Metastable Immune Characteristics

Philips Components–Signtetics uses the term 'metastable immune' to describe characteristics of some of the products in its family. Specifically the 74F50XXX family presently consist of 4 products which will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074. By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10MHz clock and 10.02 MHz data) the device–under–test can be often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device–under–test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Figure 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5V volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device–under–test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will appear as in Fig. 3. The 74F5074 Q output will not vary with respect to the Q trigger point even when the a part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Components–Signetics patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased clock–to–Q/$\overline{Q}$ propagation delay.

This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_0.

The metastability characteristics of the 74F5074 and related part types represent state–of–the–art TTL technology.

After determining the T_0 and t of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74F5074 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74F5074 10 nanoseconds after the clock edge. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/\tau)} / T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' < h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51×10^{10} seconds or about 480 years.

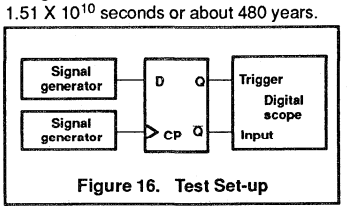


Figure 16. Test Set-up

COMPARISON OF METASTABLE IMMUNE AND NON–IMMUNE CHARACTERISTICS

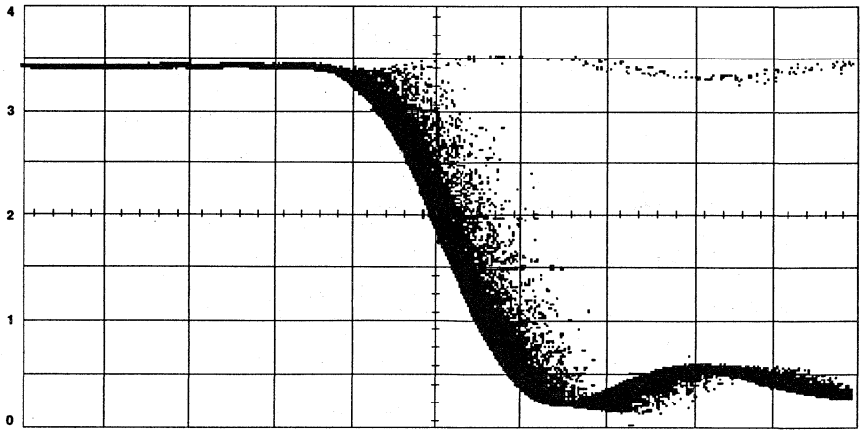


Figure 17. 74F74 $\overline{Q}$ Output triggered by Q output, set-up and hold times violated

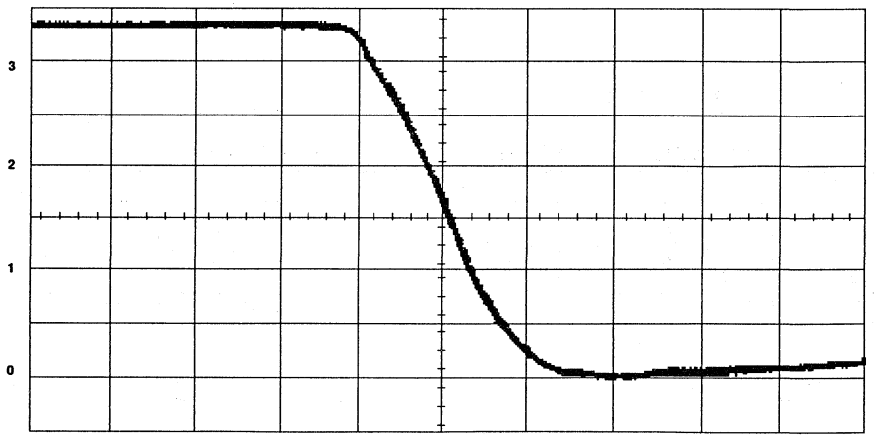


Figure 18. 74F74 $\overline{Q}$ Output triggered by Q output, set-up and hold times violated

MEAN TIME BETWEEN FAILURES (MTBF) VERSUS t'

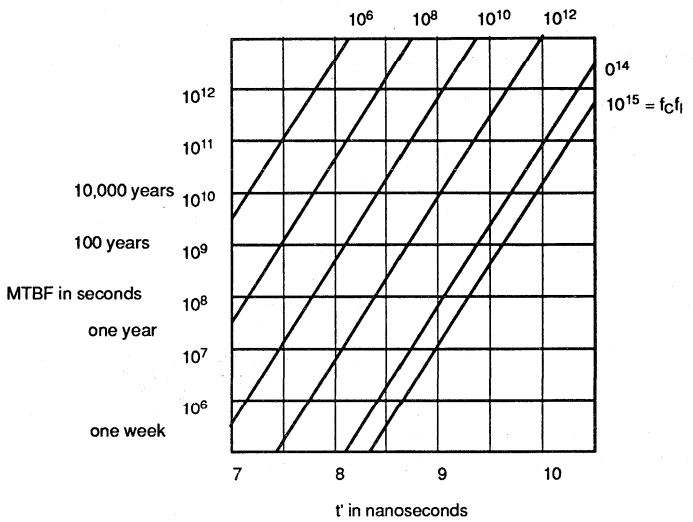


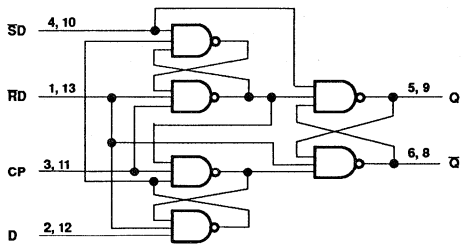
Figure 19.

NOTE: V_{CC} = 5V, T_{amb} = 25°C, τ =135ps, To = 9.8 X 10^6 sec

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.5V	125ps	1.0 X 10^9 sec	138ps	5.4 X 10^6 sec	160ps	1.7 X 10^5 sec
5.0V	115ps	1.3 X 10^{10} sec	135ps	9.8 X 10^6 sec	167ps	3.9 X 10^4 sec
4.5V	115ps	3.4 X 10^{13} sec	132ps	5.1 X 10^8 sec	175ps	7.3 X 10^4 sec

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

Synchronizing dual D-type flip-flop/clock driver | 74F5074

FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↕	X	NC	NC	Hold

NOTES:
3. H = High voltage level
4. h = High voltage level one setup time prior to low–to–high clock transition
5. L = Low voltage level
6. l = Low voltage level one setup time prior to low–to–high clock transition
7. NC = No change from the previous setup
8. X = Don't care
9. ↑ = Low–to–high clock transition
10. ↕ = Not low–to–high clock transition
11. * = This setup is unstable and will change when either set or reset return to the high level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			T_A =
UNIT						
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current	V_{CC} ± 10%			–12	mA
		V_{CC} ± 5%			–15	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Dn	V_{CC} = MAX, V_I = 0.5V					-250	µA
		CPn, $\overline{SD}$n, $\overline{RD}$n	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				20	30	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	105	120		90		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	3.9 3.9	6.0 6.0	1.5 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}$n, $\overline{RD}$n to Qn or $\overline{Q}$n	Waveform 2	3.0 3.0	4.5 5.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
$t_{sk(o)}$	Output skew[1,2]	Waveform 4			1.5		1.5	ns

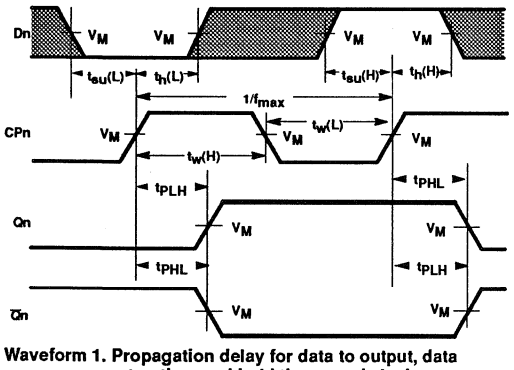
NOTES:

1. $|t_{PN}$ actual – t_{PM} actual| for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

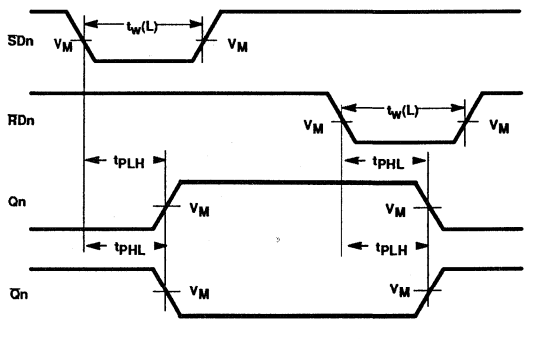
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Dn to CPn	Waveform 1	1.5 1.5			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.5 1.5		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 1	3.0 4.0			3.0 4.5		ns
t_w (L)	$\overline{SD}$n or $\overline{RD}$n pulse width, low	Waveform 2	3.0			4.0		ns
t_{rec}	Recovery time $\overline{SD}$n or $\overline{RD}$n to CPn	Waveform 3	3.0			3.5		ns

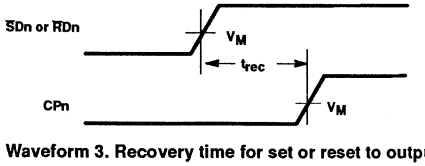
AC WAVEFORMS



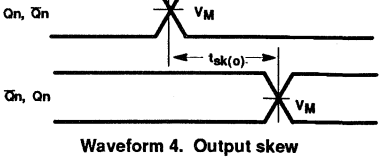
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width



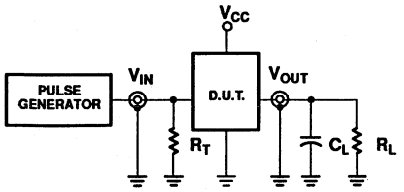
Waveform 3. Recovery time for set or reset to output



Waveform 4. Output skew

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



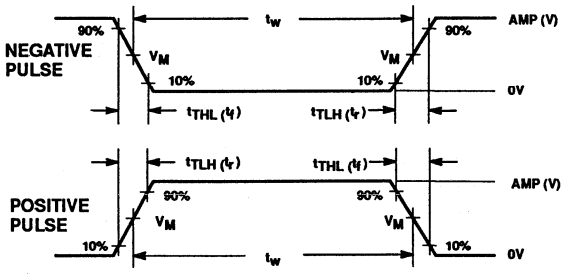
Test circuit for totem-pole outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Philips Semiconductors-Signetics

Document No.	853-1409
ECN No.	98304
Date of issue	December 13, 1989
Status	Product Specification
FAST Products	

FAST 74F5300
Fiber Optic LED Driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F5300	2.5 ns	8.0mA

FEATURES

- TTL inputs
- Output enable control
- High current source and sink capability
- Matched propagation delay times (t_{PLH}, t_{PHL})
- Symmetrical rise and fall times
- ESD protection greater than 2000 volts
- Single +5V supply
- Surface mount package

APPLICATIONS

- High speed serial data communication
- Fiber optic data links
- Local area and metropolitan area networks
- Digital Television
- PBX systems

ASSOCIATED PRODUCTS

- NE 5210/11/12 transimpedance amplifiers
- NE5214/5217 postamplifiers with link status indicator
- 74F5302 dual fiber optic LED driver

ORDERING INFORMATION

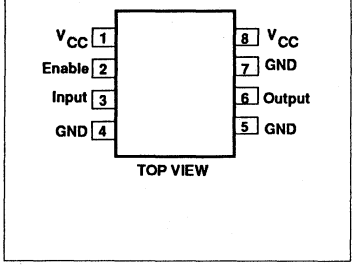
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
8-Pin Plastic DIP	74F5300N
8-Pin Plastic SO	74F5300D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Input	Data input	1.0/1.0	20µA/0.6mA
Enable	Enable input	1.0/1.0	20µA/0.6mA
Output	Current driver output	8000/266.6	160mA/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

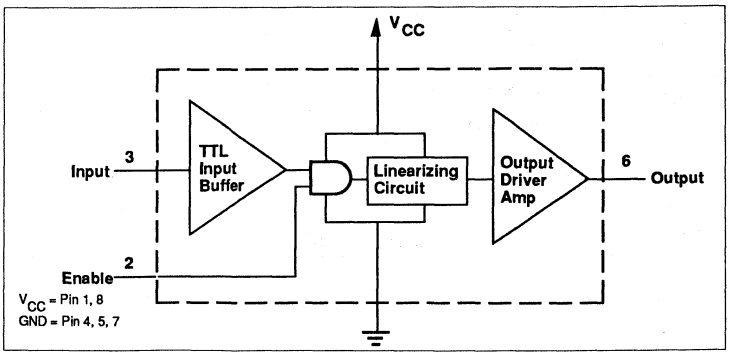


DESCRIPTION

The 74F5300 is a LED driver designed for use in fiber optics links. The 74F5300 is ideally suited for use in high speed optical high transmitter systems.

The TTL input buffer accepts TTL data. A logic High on the Enable pin enables the buffer to drive the output driver amplifier. The Linearizing Circuit ensures a constant propagation delay for t_{PLH} and t_{PHL}, and controls the rise and fall times. The output driver amplifier is capable of sourcing more than 160 mA and sinking more than 160 mA at low impedances. The high current output driver has been designed to deal with transmission line effects of high speed switching systems with fast rising and falling edges. The performance of the system can be enhanced by matching impedance at the output for proper termination. It exhibits closely matched propagation delays

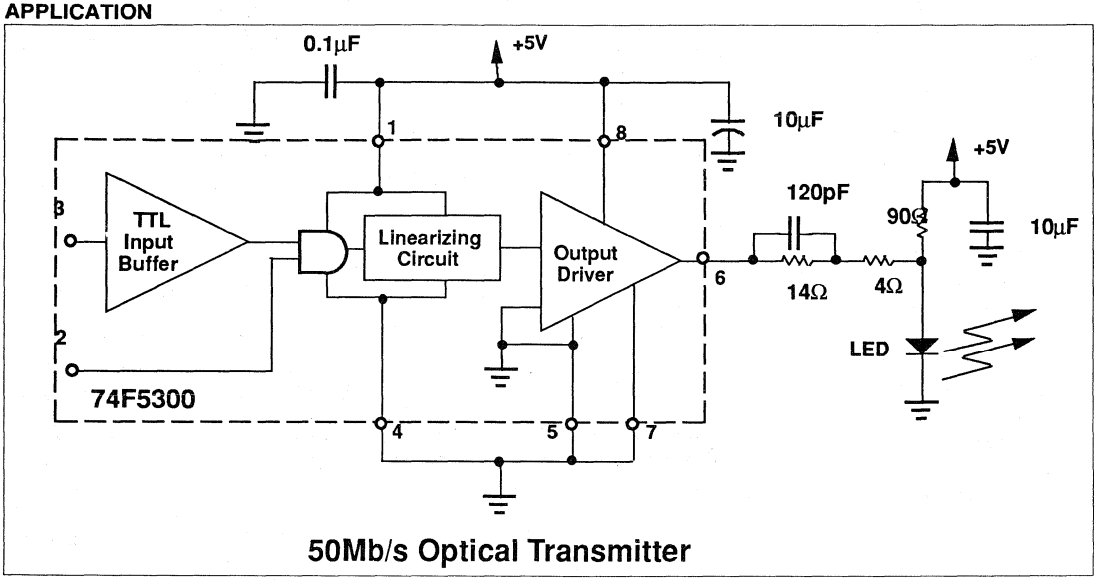
LOGIC DIAGRAM



(t_{PHL}, t_{PLH}) and symmetrical rise and fall times. The resulting optical waveform has minimal Duty Cycle Distortion (DCD). When used with the external pre-bias and pre-charging circuits, the response can be tailored to a specific LED to eliminate any overshoot and to minimize the long fall response.

Additionally, this part can be used as the transmiter in a complete fiber optic system when combined with any of the NE5210/5211/5212 preamplifiers and NE5214/5217 preamplifiers for the optical receiver. Please refer to applications note AN1121 in the Signetics Fiber Optic Communication Data Book for more specific applications information.

APPLICATION



50Mb/s Optical Transmitter

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	240	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-160	mA
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -80mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.8	3.3	3.9	V
				V_{CC} = 5V	3.0	3.3	3.6	V
			I_{OH} = -160mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.42	0.55	V
			I_{OL} = 120mA	±10%V_{CC}		0.45	0.60	V
			I_{OL} = 160mA	±10%V_{CC}		0.55	0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				4.0	12	mA
	Supply current (total) I_{CCL}					10.5	22	mA

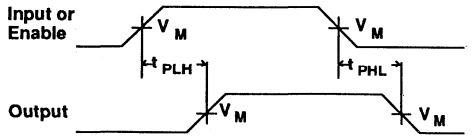
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The device is not short circuit protected.

AC ELECTRICAL CHARACTERISTICS

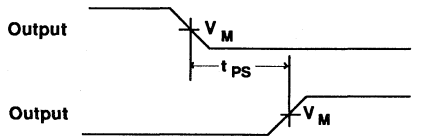
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 100Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 100Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Input or Enable to Output	Waveform 1	1.0 1.0	2.5 2.5	5.0 5.0	1.0 1.0	5.0 5.0	ns
D_{tpw}	Pulse width distortion[1]	Frequency = 10MHz		0.8	1.2		1.8	ns
t_{PS}	Propagation delay Skew[2,4]	Waveform 2		0.7	1.2		1.3	ns
t_{RFS}	Rise and Fall time Skew [3,4]			0.6	1.5		1.5	ns
t_{THL} t_{TLH}	Fall time 90% to 10% Rise time 10% to 90%	Test circuits and Waveforms	0.5 1.0	1.4 2.0	3.5 4.0	0.5 1.0	4.0 4.5	ns

NOTE:
1. D_{tpw} is defined as the difference between input pulse width and output pulse width (0 to 3 volt input swing and 50% duty cycle).
2. $|t_{PLH}$ actual - t_{PHL} actual $|$.
3. $|t_{TLH}$ actual - t_{THL} actual $|$.
4. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



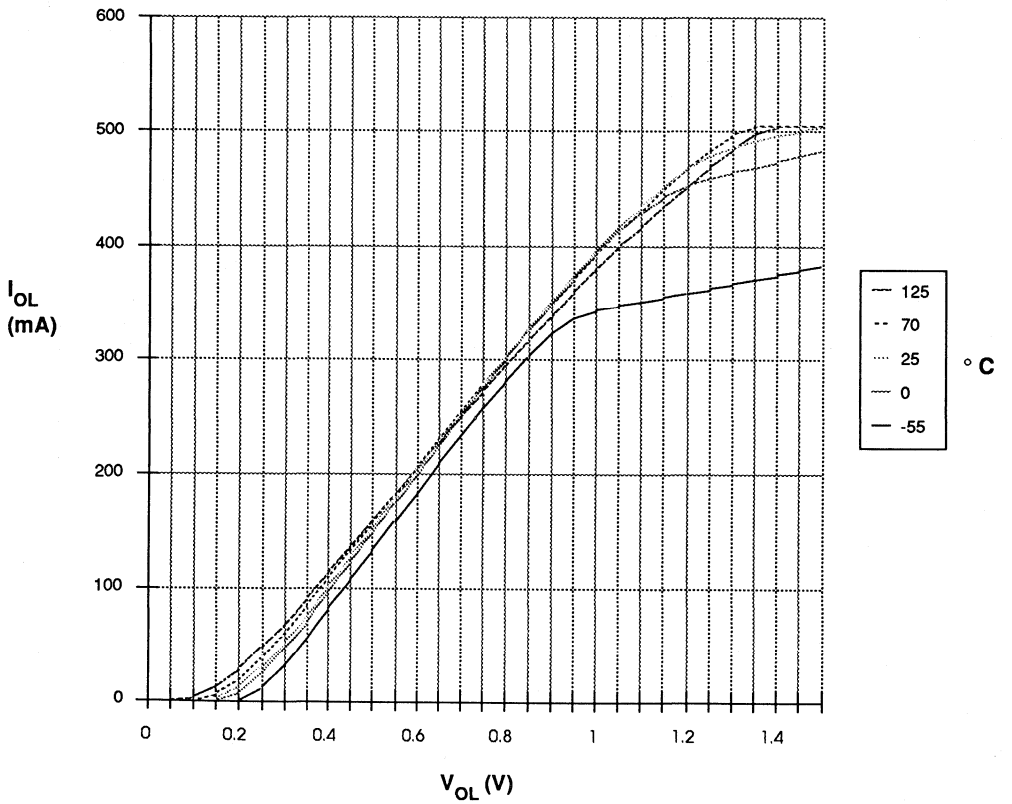
Waveform 1. Propagation Delay for Input to Output



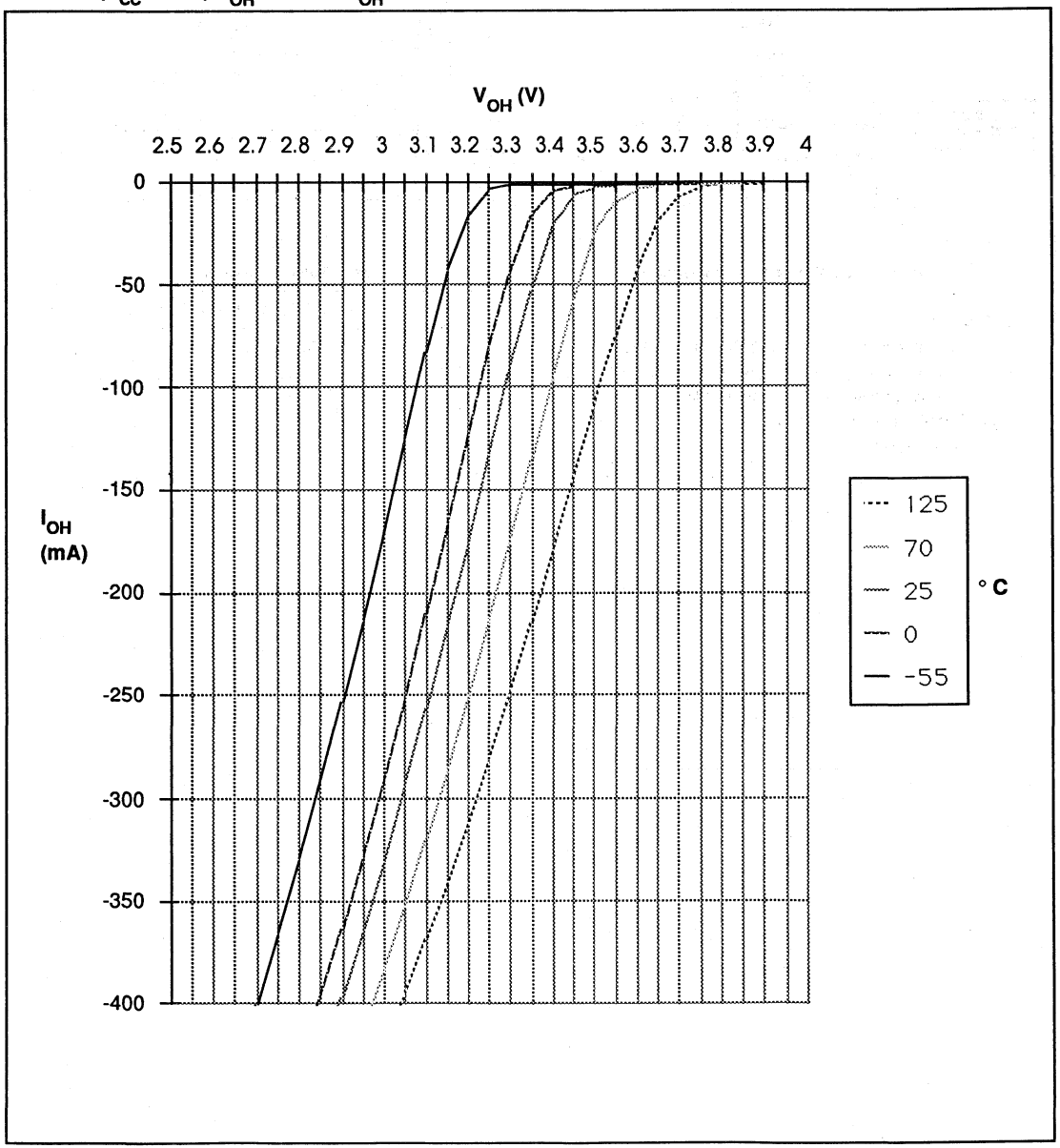
Waveform 2. Propagation Delay Skew

NOTE: For all waveforms, $V_M = 1.5V$.

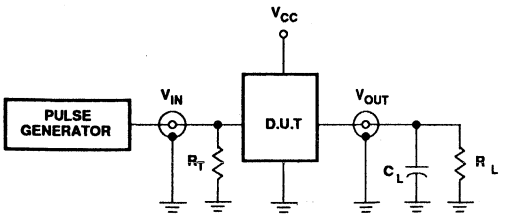
TYPICAL (V_{CC} =5.0V) V_{OL} VERSUS I_{OL} FOR VARIOUS TEMPERATURES



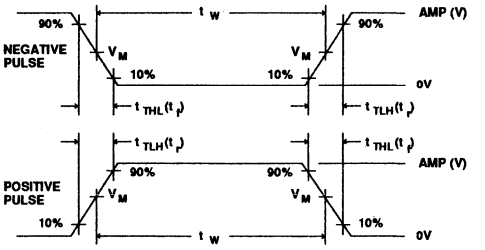
TYPICAL (V_{CC} =5.0V) V_{OH} VERSUS I_{OH} FOR VARIOUS TEMPERATURES



TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Fiber optic dual LED/clock driver — 74F5302

FEATURES

- TTL inputs
- Output enable control
- High current source and sink capability
- Matched propagation delay times (t_{PLH}, t_{PHL})
- Symmetrical rise and fall times
- ESD protection greater than 2000 volts
- Single +5V supply
- Surface mount package

APPLICATIONS

- High speed serial data communication
- Fiber optic data links
- Local area and metropolitan area networks
- Digital Television
- PBX systems

ASSOCIATED PRODUCTS

- NE5210/11/12 transimpedance amplifiers
- NE5214/5217 postamplifiers with link status indicator
- 74F5300 fiber optic LED driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F5302	2.5ns	8mA

ORDERING INFORMATION

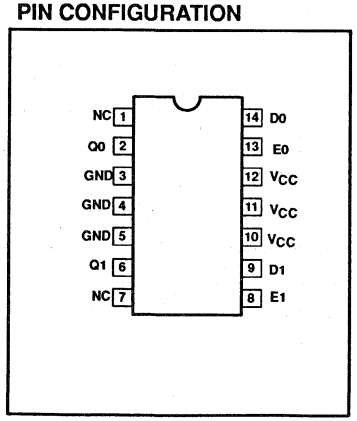
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
14–pin plastic DIP	N74F5302N
14–pin plastic SO	N74F5302D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

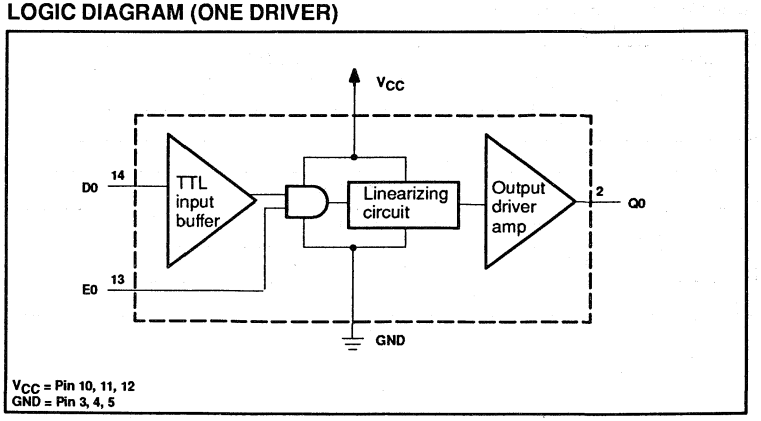
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/1.0	20µA/0.6mA
En	Enable inputs	1.0/1.0	20µA/0.6mA
Qn	Current driver output	8000/266.6	160mA/160mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

PIN CONFIGURATION



LOGIC DIAGRAM (ONE DRIVER)



Fiber optic dual LED/clock driver | 74F5302

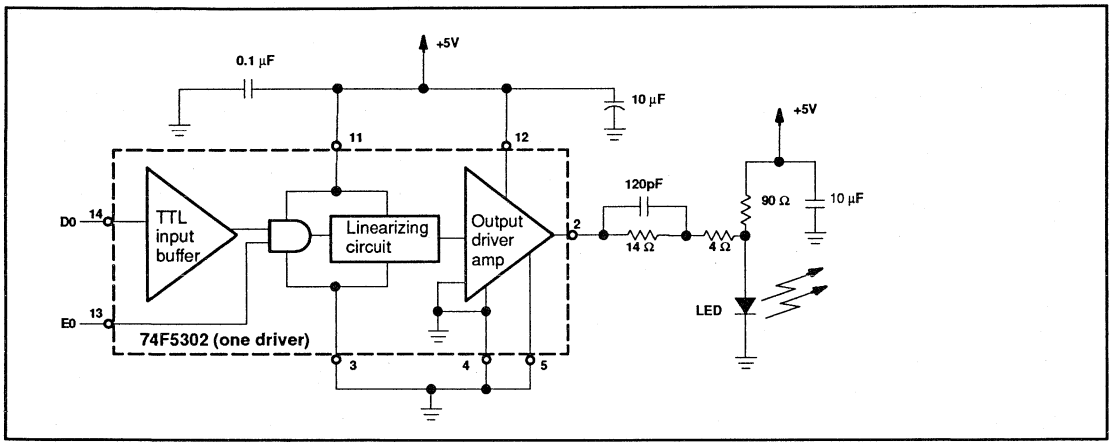
DESCRIPTION

The 74F5302 is a dual LED/clock driver designed for use in fiber optic links. The 74F5302 is ideally suited for use in high speed optical high transmitter systems. It is also ideal for use as a clock driver.

The TTL input buffer accepts TTL data. The linearizing circuits ensures a constant propagation delay for t_{PLH} and t_{PHL}, and controls the rise and fall times. The output driver amplifier is capable of sourcing more than 160mA and sinking more than 160mA at low impedances. The high current output driver has been designed to deal with transmission line effects of high speed switching systems with fast rising and falling edges. The performance of the system can be enhanced by matching impedance at the output for proper termination. It exhibits closely matched propagation delays (t_{PLH} and t_{PHL}) and symmetrical rise and fall times. The resulting optical waveform has minimal duty cycle distortion (DCD). When used with the external pre–bias and pre–charging circuits, the response can be tailored to a specific LED to eliminate any overshoot and to minimize the long fall response.

Additionally, this part can be used as the transmitter in a complete fiber optic system when combined with any of the NE5210/5211/5212 preamplifiers and NE5214/5217 postamplifiers for the optical receiver. Please refer to applications note AN1121 in the Philips Components–Signetics Fiber Optic Communication Data Book for more specific applications information.

APPLICATION FOR 50Mb/s OPTICAL TRANSMITTER



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	240	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			T_A =
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–160	mA
I_{OL}	Low–level output current			160	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN,		±10%V_{CC}	2.5			V
			V_{IL} = MAX,	I_{OH} = –80mA	±5%V_{CC}	2.8	3.3	3.9	V
			V_{IH} = MIN		V_{CC} = 5V	3.0	3.3	3.6	V
				I_{OH} = –160mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN,	I_{OL} = 100mA	±10%V_{CC}		0.42	0.55	V
			V_{IL} = MAX,	I_{OL} = 120mA	±10%V_{CC}		0.45	0.60	V
			V_{IH} = MIN	I_{OL} = 160mA	±10%V_{CC}		0.55	0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				5.0	12	mA
		I_{CCL}	V_{CC} = MAX				18	25	mA

NOTES:

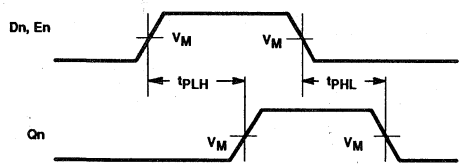
3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
4. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
5. The device is not short circuit protected.

AC ELECTRICAL CHARACTERISTICS

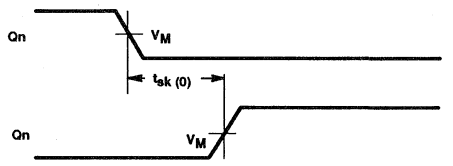
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 100Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 100Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn, En, to Qn	Waveform 1	1.0 1.0	2.0 2.5	4.5 5.0	1.0 1.0	4.5 5.0	ns
D_{tpw}	Pulse width distortion[1]	Frequency = 10MHz		0.8	1.2		1.8	ns
t_{RFS}	Rise and fall time skew[3, 4]			0.3	1.5		2.0	ns
$t_{sk(0)}$	Output skew[2, 4]	Waveform 2		0.9	1.3		1.6	ns
t_{THL} t_{TLH}	Fall time 90% to 10% Rise time 10% to 90%	Test circuits and Waveforms	1.0 1.0	1.5 1.8	3.0 3.0	0.5 0.5	4.0 4.5	ns

NOTES:
1. D_{tpw} is defined as the difference between input pulse width and output pulse width (0 to 3 volt swing and 50% duty cycle).
2. $|t_{PN}$ actual $- t_{PM}$ actual$|$ for any output compared to any other output where N and M are either LH or HL.
3. $|t_{TLH}$ actual $- t_{THL}$ actual$|$.
4. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



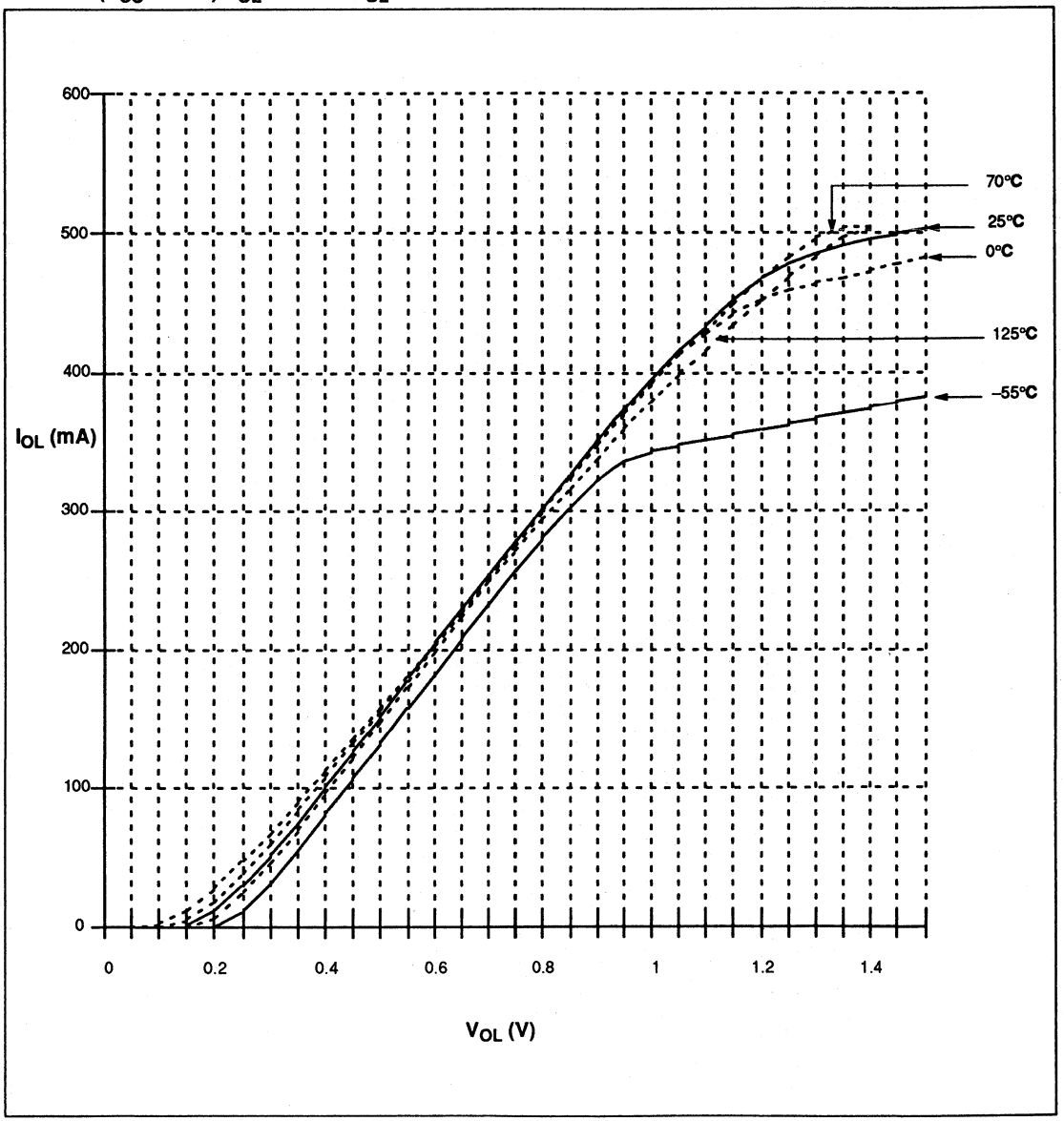
Waveform 1. Propagation delay for input to output



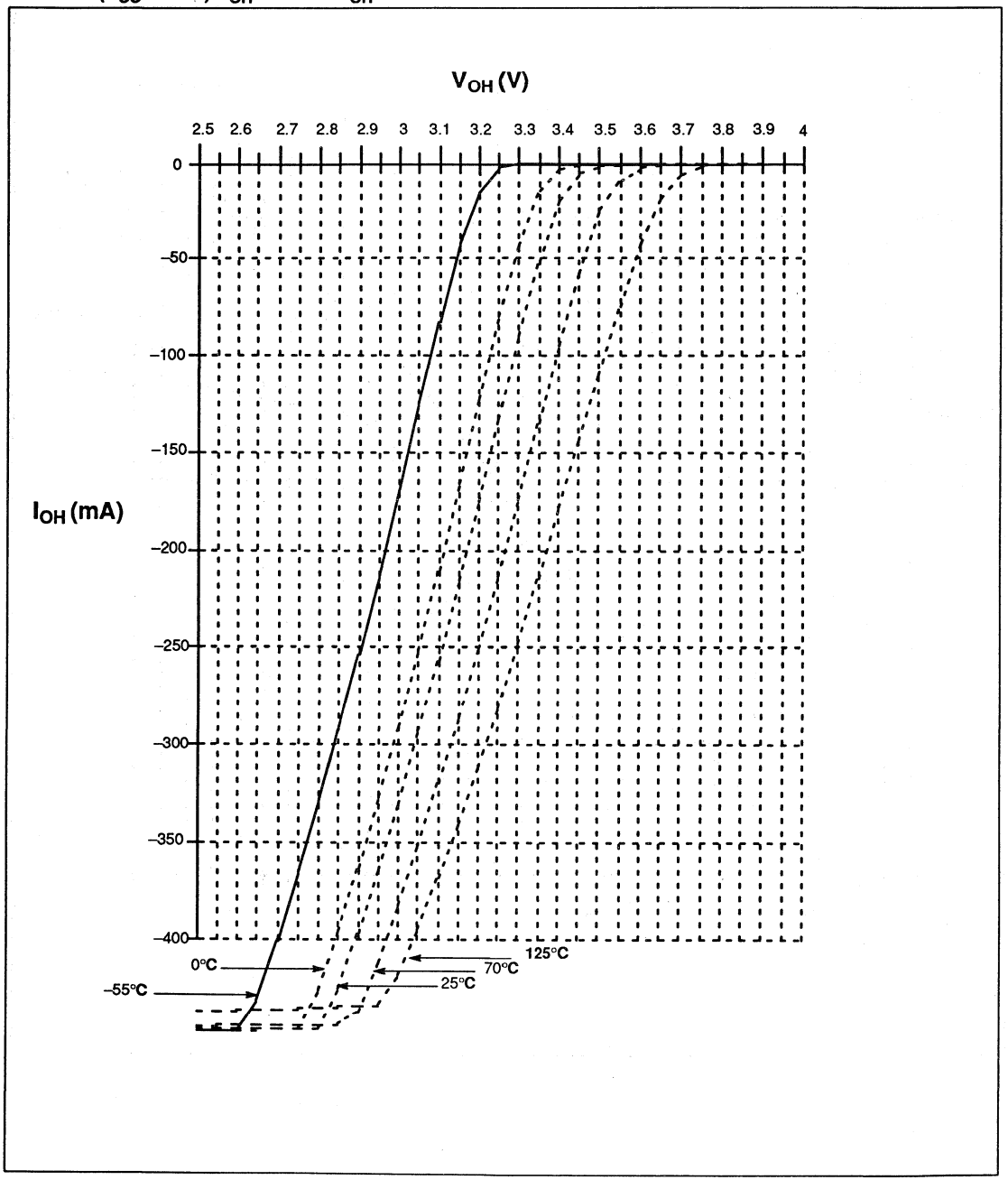
Waveform 2. Output skew

NOTE: For all waveforms, V_M = 1.5V.

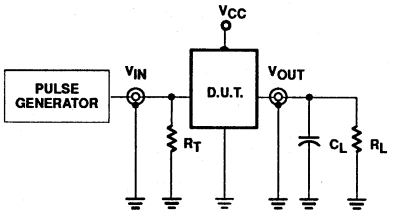
TYPICAL (V_{CC} = 5.0V) V_{OL} VERSUS I_{OL} FOR VARIOUS TEMPERATURES



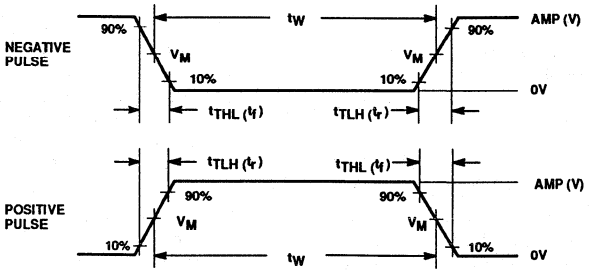
TYPICAL (V_{CC} = 5.0V) V_{OH} VERSUS I_{OH} FOR VARIOUS TEMPERATURES



TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Futurebus transceivers — 74F8960/74F8961

74F8960 Octal latched bidirectional futurebus transceiver, inverting (3-State + open collector)
74F8961 Octal latched bidirectional futurebus transceiver, non-inverting (3-State + open collector)

FEATURES

- Octal latched transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE futurebus standards
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/down operation

DESCRIPTION

The 74F8960 and 74F8961 are octal bidirectional latched transceivers and are intended to provide the electrical interface to a high performance wired–OR bus. The B port inverting drivers are low–capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a 100 mV threshold region and a 4ns glitch filter.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading.

Incident switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F8960 and 74F8961 A ports have TTL 3–state drivers and TTL receivers with a latch function. A separate High–level control input (VX) is provided to limit the A side output level to a given voltage level (such as 3.3V). For 5.0V systems, VX is simply tied to VCC.

The 74F8961 is the non–inverting version of 74F8960.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F8960	6.5ns	80mA
74F8961	6.5ns	80mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
28–pin plastic DIP (300 mil)[1]	N74F8960N, N748961N
28–pin PLCC[1]	N74F8960A, N74F8961A

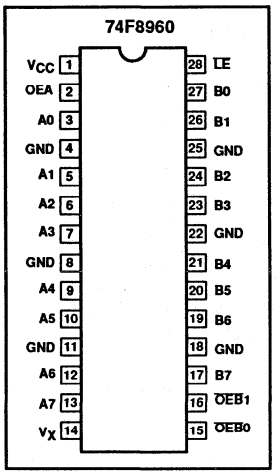
NOTE: Thermal mounting techiques are recommended.

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

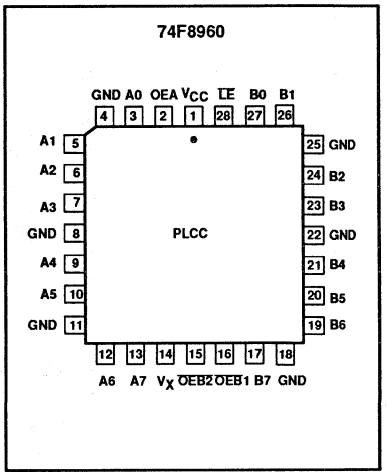
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A8	PNP latched inputs	3.5/0.117	70µA/70µA
B0 – B8	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA	A output enable input (active high)	1.0/0.033	20µA/20µA
$\overline{OEB0}$, $\overline{OEB1}$	B output enable inputs (active low)	1.0/0.033	20µA/20µA
$\overline{LE}$	Latch enable input (active low)	1.0/0.033	20µA/20µA
A0 – A7	3–state outputs	150/40	3mA/24mA
B0 – B7	Open collector outputs	OC/166.7	OC/100mA

NOTES:
5. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.
6. OC = Open collector.

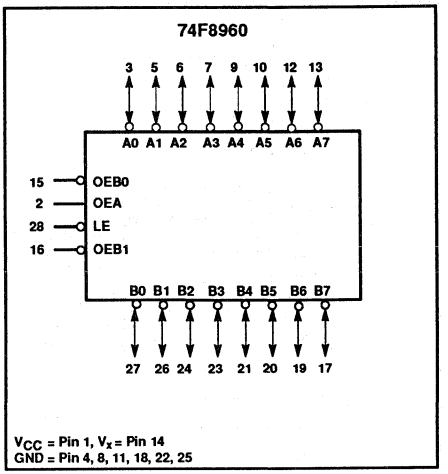
PIN CONFIGURATION



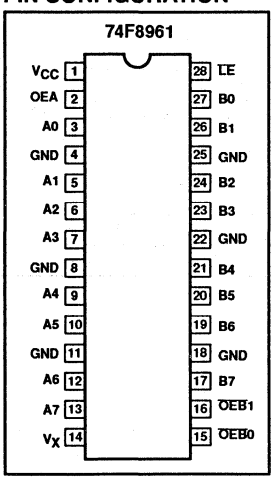
PIN CONFIGURATION PLCC



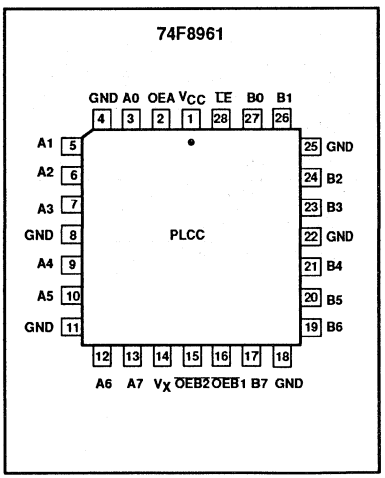
LOGIC SYMBOL



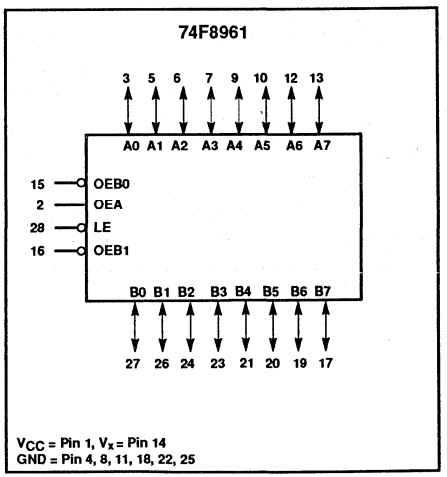
PIN CONFIGURATION



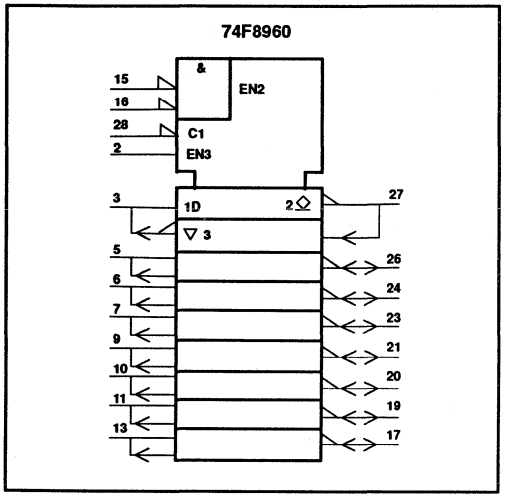
PIN CONFIGURATION PLCC



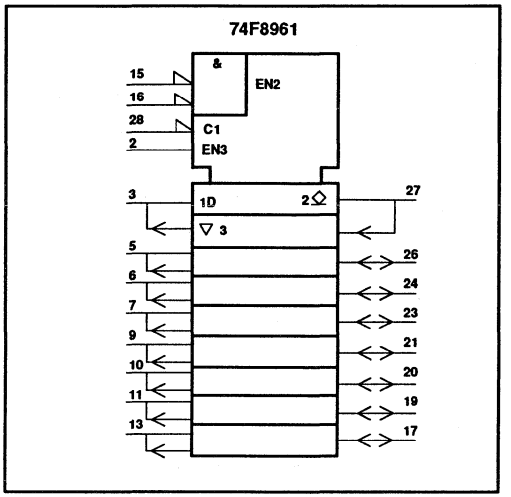
LOGIC SYMBOL



IEC/IEEE SYMBOL FOR 74F8960



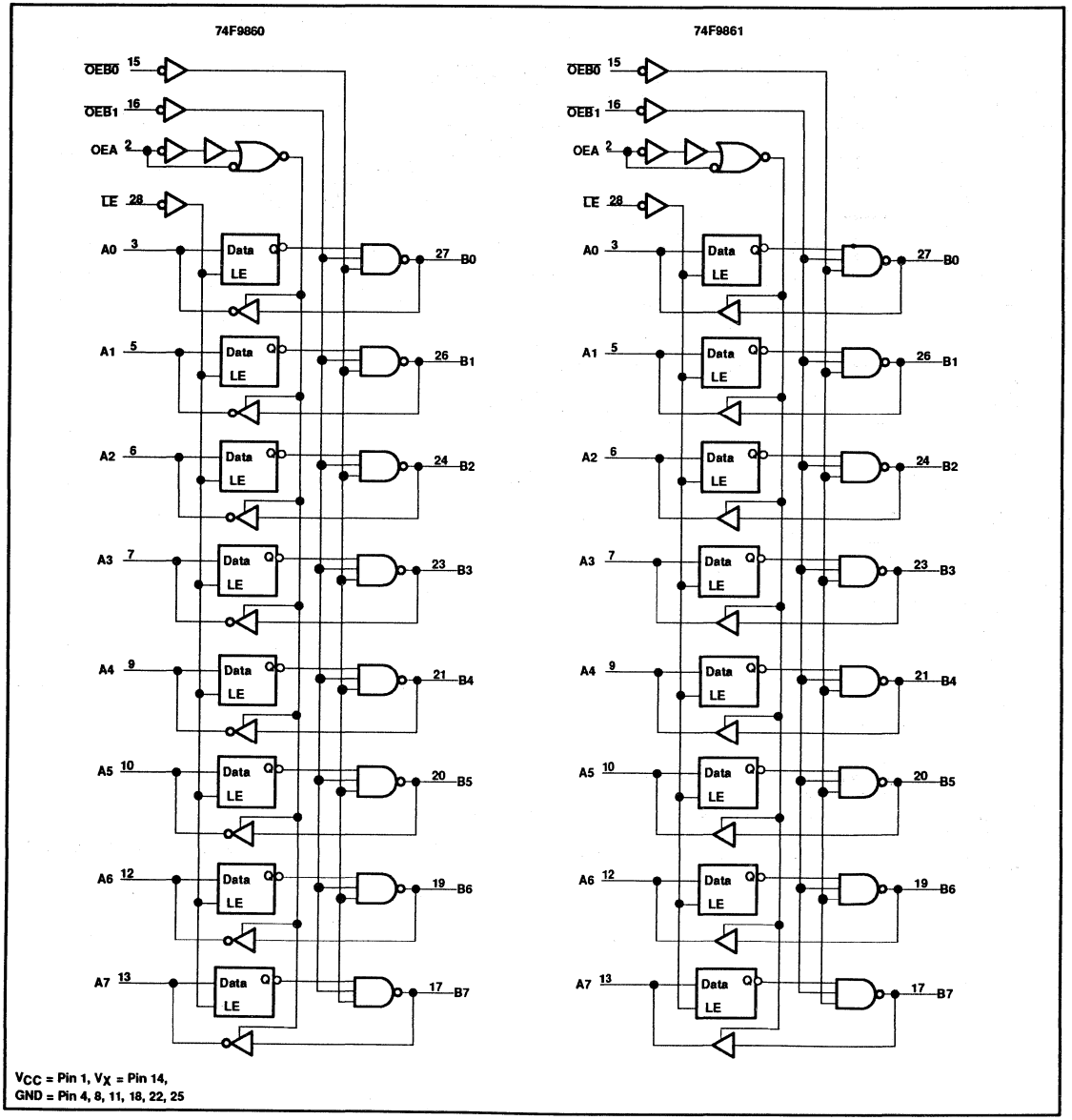
IEC/IEEE SYMBOL FOR 74F8961



PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A0 – A7	3, 5, 6, 7, 9, 10, 12, 13	I/O	PNP latched input/3–state output (with V_X control option)
B0 – B7	27, 26, 24, 23, 21, 20, 19, 17	I/O	Data input with special threshold circuitry to reject noise/ open collector output, high current drive
$\overline{OEB0}$	15	Input	Enables the B outputs when both pins are low
$\overline{OEB1}$	16	Input	Enables the A outputs when high
$\overline{LE}$	28	Input	Latched when high (a special feature is builit in for proper enabling times)
V_X	14	Input	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

LOGIC DIAGRAM



FUNCTION TABLE FOR 74F8960

INPUTS						LATCH	OUTPUTS		OPERATING MODE
An	Bn*	$\overline{LE}$	OEA	$\overline{OEB}$	$\overline{OEB}$	STATE	An	Bn	
H	X	L	L	L	L	H	Z	L	A 3–state, data from A to B
L	X	L	L	L	L	L	Z	H**	
X	X	H	L	L	L	Qn	Z	$\overline{Q}$n	A 3–state, latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
–	L	H	H	L	L	H (2)	L	Z(2)	
–	–	H	H	L	L	Qn	$\overline{Q}$n	$\overline{Q}$n	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3–state
I	X	L	L	H	X	I	Z	Z	
X	X	H	L	H	X	Qn	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3–state, data from B to A
–	L	L	H	H	H	L	L	Z	
–	H	H	H	H	H	Qn	H	Z	
–	L	H	H	H	H	Qn	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3–state
I	X	L	L	X	H	I	Z	Z	
X	X	H	L	X	H	Qn	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3–state, data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Qn	H	Z	
–	L	H	H	X	H	Qn	L	Z	

NOTES:
1. H = High–voltage level
2. L = Low–voltage level
3. X = Don't care
4. – = Input not externally driven
5. Z = High impedance (off) state
6. Q_n = High or low voltage level one setup time prior to the low–to–high $\overline{LE}$ transition.
7. (1) = Condition will cause a feedback loop path: A to B and B to A.
8. (2) = The latch must be preconmditioned such that B inputs may assume a high or low level while $\overline{OEB}$0 and $\overline{OEB}$1 are low and $\overline{LE}$ is high.
9. H**= Goes to level of pullup voltage.
10. B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to low state.

FUNCTION TABLE FOR 74F8961

INPUTS						LATCH	OUTPUTS		OPERATING MODE
An	Bn*	$\overline{LE}$	OEA	$\overline{OEB}$	$\overline{OEB}$	STATE	An	Bn	
H	X	L	L	L	L	H	Z	H**	A 3–state, data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	A 3–state, latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
–	L	H	H	L	L	H (2)	L	Z(2)	
–	–	H	H	L	L	Qn	Qn	Qn	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3–state
I	X	L	L	H	X	I	Z	Z	
X	X	H	L	H	X	Qn	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3–state, data from B to A
–	L	L	H	H	H	L	L	Z	
–	H	H	H	H	H	Qn	H	Z	
–	L	H	H	H	H	Qn	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3–state
I	X	L	L	X	H	I	Z	Z	
X	X	H	L	X	H	Qn	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3–state, data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Qn	H	Z	
–	L	H	H	X	H	Qn	L	Z	

NOTES:
1. H = High–voltage level
2. L = Low–voltage level
3. X = Don't care
4. – = Input not externally driven
5. Z = High impedance (off) state
6. Q_n = High or low–voltage level one setup time prior to the low–to–high $\overline{LE}$ transition.
7. (1) = Condition will cause a feedback loop path: A to B and B to A.
8. (2) = The latch must be preconmditioned such that B inputs may assume a high or low level while $\overline{OEB}0$ and $\overline{OEB}1$ are low and $\overline{LE}$ is high.
9. H**= Goes to level of pullup voltage.
10. B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_X	Threshold control		–0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}$, OEA, $\overline{LE}$	–0.5 to +7.0	V
		A0 – A7, B0 – B7	–0.5 to +5.5	V
I_{IN}	Input current		–40 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	A0 – A7	48	mA
		B0 – B7	200	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
Tstg	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Except B0 – B7	2.0			V
		B0 – B7	1.6			V
V_{IL}	Low–level input voltage	Except B0 – B7			0.8	V
		B0 – B7			1.475	V
I_{Ik}	Input clamp current	Except A0 – A7			–18	mA
		A0 – A7			–40	mA
I_{OH}	High–level output current	A0 – A7			–3	mA
I_{OL}	Low–level output current	A0 – A7			24	mA
		B0 – B7			100	mA
T_{amb}	Operating free air temperature		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN.	LIMITS TYP.[2]	LIMITS MAX.	UNIT
I_{OH}	High–level output current	B0 – B7	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power–off output current	B0 – B7	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A0 – A7[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA, V_X = V_{CC}	2.5		V_{CC}	V
				I_{OH} = –4mA, V_X = 3.13V and 3.47V	2.5			V
V_{OL}	Low-level output voltage	A0 – A7[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA, V_X = V_{CC}			0.50	V
		B0 – B78		I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A0 – A7	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A0 – A7	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 7.0V				100	µA
		A0–A7, B0 – B7	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High–level input current	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 2.7V				20	µA
		B0–B7	V_{CC} = MAX, V_I = 2.1V, Bn – An = 0V				100	µA
I_{IL}	Low–level input current	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 0.5V				–20	µA
		B0 – B7	V_{CC} = MAX, V_I = 0.3V				–100	µA
I_{OZH} + I_{IH}	Off–state output current, high–level current applied	A0 – A7	V_{CC} = MAX, V_O = 2.7V				70	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied	A0 – A7	V_{CC} = MAX, V_I = 0.5V				–70	µA
I_X	High–level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA = $\overline{OEB}$n = 2.7V, A0 – A7 = 2.7V, B0 – B7 = 2.0V,		–100		100	µA
			V_{CC} = MAX, V_X = 3.13 & 3.47V, $\overline{LE}$ = OEA = $\overline{OEB}$n = A0 – A7 = 2.7V, B0 – B7 = 2.0V,		–10		10	µA
I_{OS}	Short circuit output current[3]	A0–A7 only	74F8960	V_{CC} = MAX, Bn = 1.3V, OEA = 2.0V, $\overline{OEB}$n = 2.7V	-60		-150	mA
			74F8961	V_{CC} = MAX, Bn = 1.8V, OEA = 2.0V, $\overline{OEB}$n = 2.7V				
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			65	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}				75	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} =1.8v and V_{IL} = 1.3V.

AC ELECTRICAL CHARACTERISTICS FOR 74F8960

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50p, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1, 2	4.5 6.0	6.0 10.0	8.5 13.5	3.5 7.5	9.5 14.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low, OEA to An	Waveform 4 Waveform 5	8.0 8.5	10.5 11.0	13.5 13.5	7.5 8.5	15.0 16.0	ns
t_{PHZ} t_{PLZ}	Output enable time from high or low, OEA to An	Waveform 4 Waveform 5	2.0 2.0	3.5 4.5	6.5 7.0	2.0 2.0	7.0 7.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_D = 50pF, R_U = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D = 50pF, R_L = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1, 2	3.5 3.5	5.5 5.0	8.0 8.0	2.0 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to Bn	Waveform 1, 2	3.5 4.0	5.5 6.5	8.5 9.0	2.5 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Output enable/disable time $\overline{OE}$Bn to Bn	Waveform 1, 2	2.5 3.5	4.5 5.5	7.5 8.5	1.5 3.5	8.0 9.0	ns
t_{TLH} t_{THL}	Transition time, Bn port 1.3V to 1.7V, 1.7V to 1.3V	Test circuit and waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	5.0 6.0	ns

AC SETUP REQUIREMENTS FOR 74F8960

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to $\overline{CE}$	Waveform 3	5.0 3.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to $\overline{CE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(L)$	$\overline{CE}$ pulse width, low	Waveform 3	4.5			5.0		ns

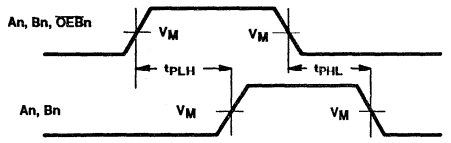
AC ELECTRICAL CHARACTERISTICS FOR 74F8961

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50p, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1, 2	5.5 4.5	8.0 6.0	12.0 9.0	5.5 4.5	12.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low, OEA to An	Waveform 4 Waveform 5	8.0 8.5	10.5 11.0	13.5 13.5	7.5 8.0	15.0 15.5	ns
t_{PHZ} t_{PLZ}	Output enable time from high or low, OEA to An	Waveform 4 Waveform 5	2.0 2.0	3.5 4.5	6.0 7.0	1.5 2.0	6.5 7.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_D = 50pF, R_U = 9Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_D = 50pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1, 2	3.0 3.0	5.0 4.5	7.0 7.5	2.5 2.5	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to Bn	Waveform 1, 2	3.5 3.5	5.0 5.0	8.0 8.0	3.0 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Output enable/disable time $\overline{OEB}$n to Bn	Waveform 1, 2	3.0 3.5	4.5 5.5	7.0 9.0	2.5 3.5	8.0 10.0	ns
t_{TLH} t_{THL}	Transition time, Bn port 1.3V to 1.7V, 1.7V to 1.3V	Test circuit and waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	5.0 4.5	ns

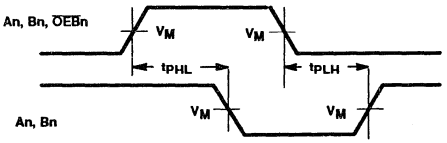
AC SETUP REQUIREMENTS FOR 74F8961

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to $\overline{LE}$	Waveform 3	3.5 4.5			4.5 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(L)$	$\overline{LE}$ pulse width, low	Waveform 3	4.0			5.0		ns

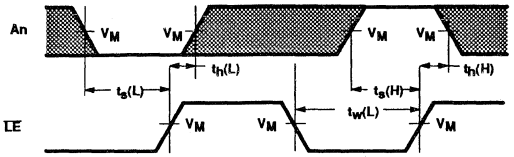
AC WAVEFORMS



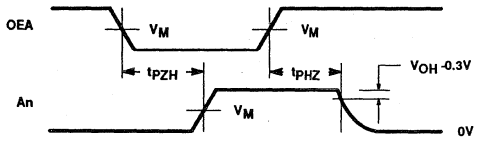
Waveform 1. Propagation delay for data to output



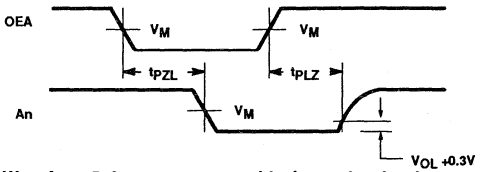
Waveform 2. Propagation delay for data to output



Waveform 3. Data setup and hold times and $\overline{LE}$ pulse width



Waveform 4. 3–state output enable time to high level and output disable time from high level



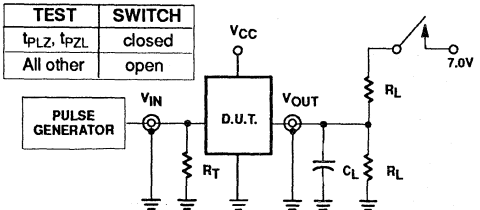
Waveform 5. 3-state output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

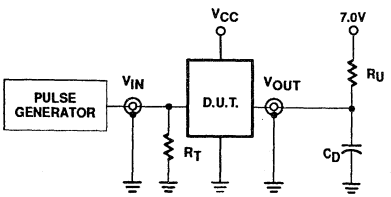
TEST CIRCUITS AND WAVEFORMS

SWITCH POSITION

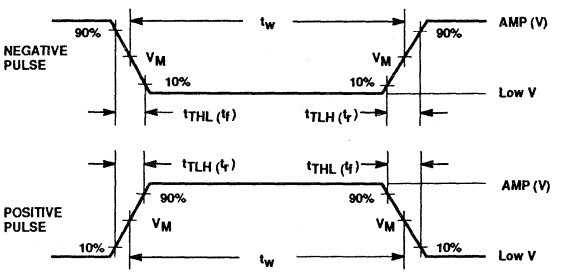
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–state outputs on A port



Test circuit for outputs on B port



Input pulse definition

family 74F	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	3.0V	1.0V	1.5V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_U = Pull up resistor; see AC electrical characteristics for value.
C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Futurebus transceivers — FAST 74F8962/8963

74F8962 9-bit latched bidirectional Futurebus transciver, INV (OC)
74F8963 9-bit latched bidirectional Futurebus transciver, NINV (OC)

FEATURES

- Octal latched transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE 896 futurebus standards
- Built–in precision band–gap reference provides accurate receiver thresholds and improved noise immunity
- Multiple GND pins minimize ground bounce
- Glitch–free power up/power down operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F8962	6.5ns	90mA
74F8963	5.5ns	90mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
44–pin quad flatpack[1]	N74F8962Y, N74F8963Y
44–pin PLCC	N74F8962A, N74F8963A

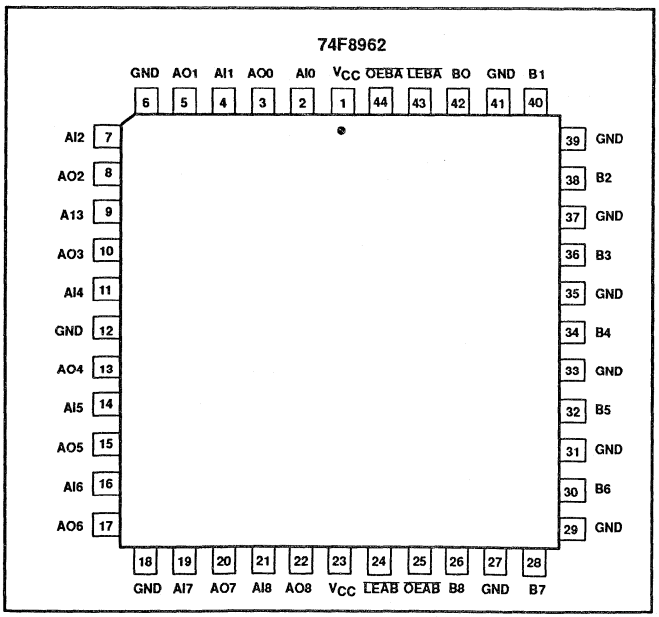
Note to ordering information
1. Flatpack package is not available at this time.

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

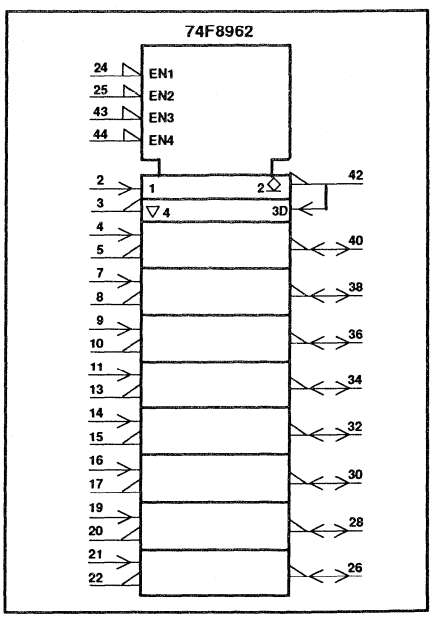
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
AI0 – AI8	PNP latched inputs	1.0/0.167	20µA/100µA
B0 – B8	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
$\overline{OEAB}$, $\overline{OEBA}$	Output enable inputs (active low)	1.0/0.033	20µA/20µA
$\overline{LEAB}$, $\overline{LEBA}$	Latch enable inputs (active low)	1.0/0.033	20µA/20µA
AO0 – AO8	3–state outputs	150/40	3mA/24mA
B0 – B8	Open collector outputs	OC/166.7	OC/100mA

Notes to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.
2. OC = Open collector.

PIN CONFIGURATION FLATPACK AND PLCC



IEC/IEEE SYMBOL



DESCRIPTION

The 74F8962 and 74F8963 are octal bidirectional latched transceivers and are intended to provide the electrical interface to a high performance wired–OR bus. The B port inverting drivers are low–capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a 150 mV threshold region.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading.

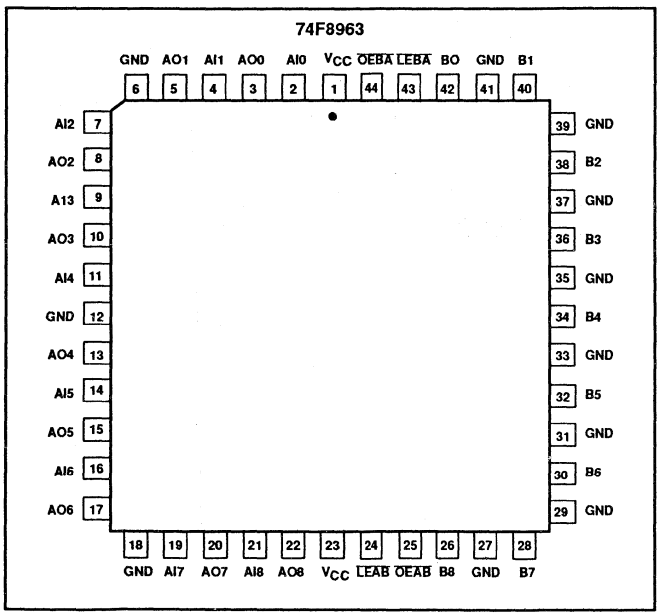
Incident wave switching to 9 ohms is guaranteed. The voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

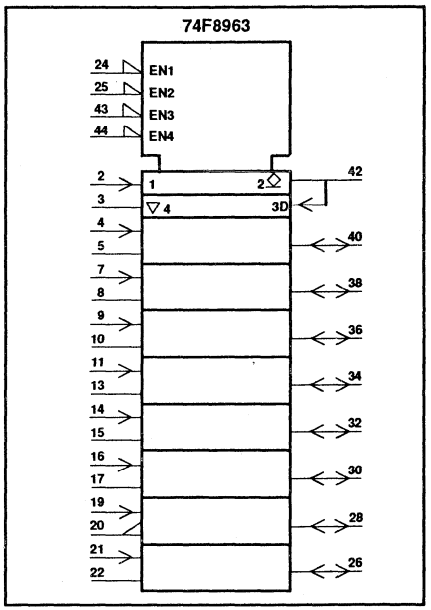
The 74F8962 and 74F8963 A ports have TTL 3–state drivers and TTL receivers with a latch function.

The 74F8963 is the non–inverting version of 74F8962.

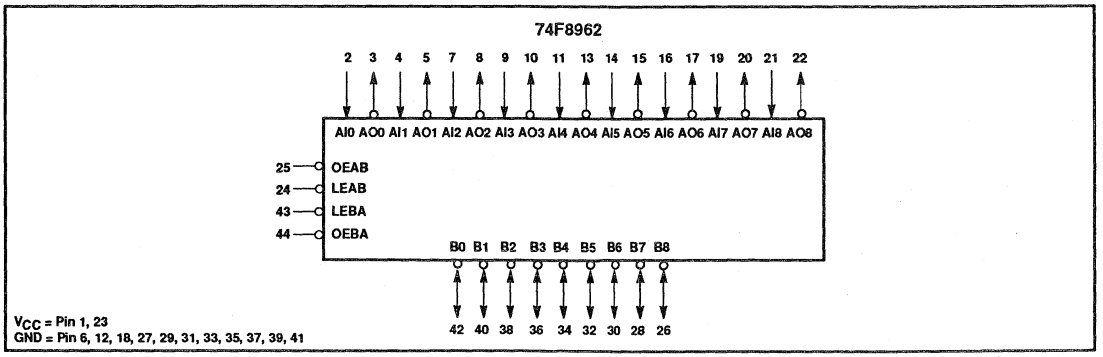
PIN CONFIGURATION FLATPACK AND PLCC



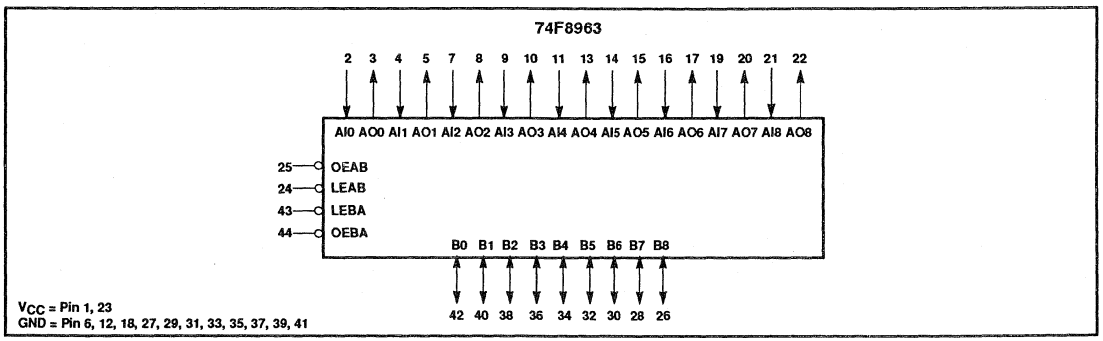
IEC/IEEE SYMBOL



LOGIC SYMBOL FOR 74F8962



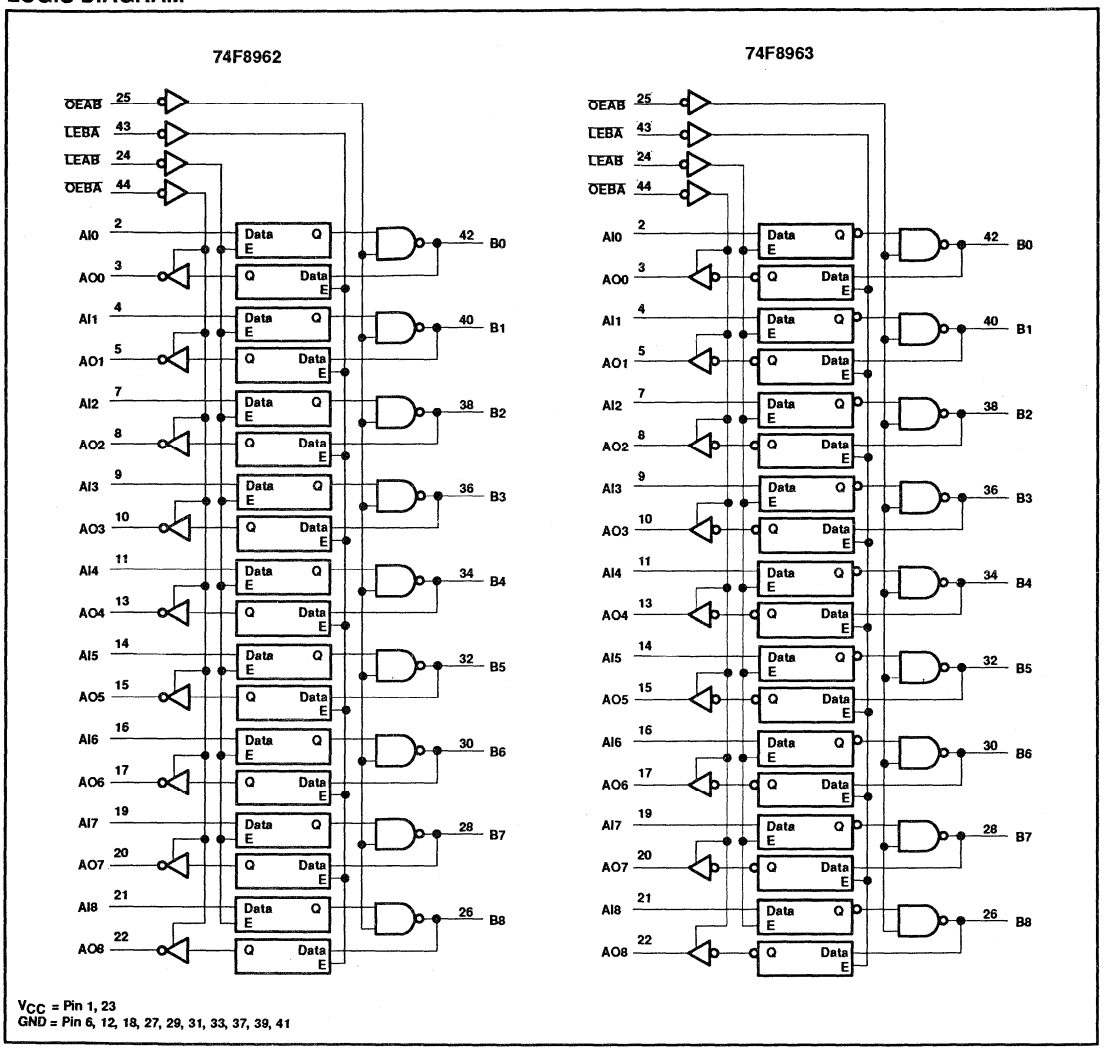
LOGIC SYMBOL FOR 74F8963



PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
AI0 – AI8	2, 4, 7, 9, 11, 14, 16, 19, 21	Input	PNP latched inputs.
B0 – B8	42, 40, 38, 36, 34, 32, 30, 28, 26	I/O	Data input / open collector output, high current drives.
$\overline{OEAB}$	25	Input	Output enable input. Enables the B outputs when low.
$\overline{OEBA}$	44	Input	Output enable input. Enables the A outputs when high.
$\overline{LEAB}$	24	Input	Latch enable input. Enables the AB latches low.
$\overline{LEBA}$	43	Input	Latch enable input. Enables the BA latches low.
AO0 – AO8	3, 5, 8, 10, 13, 15, 17, 20, 22	Output	TTL 3–state outputs.
GND	6, 12, 18, 27, 29, 31, 33, 35, 37, 39, 41	Ground	Grounds
V_{CC}	1, 23	Power	Positive supply voltages

LOGIC DIAGRAM



V_{CC} = Pin 1, 23
GND = Pin 6, 12, 18, 27, 29, 31, 33, 37, 39, 41

FUNCTION TABLE FOR 74F8962

INPUTS						LATCH STATES		OUTPUTS		OPERATING MODE
AIn	Bn*	$\overline{LEAB}$	$\overline{LEBA}$	$\overline{OEAB}$	$\overline{OEBA}$	AB	BA	AOn	Bn	
H	H	L	L	H	H	H	H	Z	X	B and AO disabled
L	L	L	L	H	H	L	L	Z	X	
X	X	H	H	H	H	Qn	Qn	Z	X	
H	–	L	X	L	H	H	Qn	Z	L	AO 3–state, transparent data from AI to B
L	–	L	X	L	H	L	Qn	Z	H**	
X	H	X	L	H	L	Qn	H	L	X	B disabled, transparent data from B to AO
X	L	X	L	H	L	Qn	L	H	X	
X	X	H	X	L	H	Qn	Qn	Z	$\overline{Qn}$	AO 3–state, latched data to B
X	X	X	H	H	L	Qn	Qn	$\overline{Qn}$	X	B disabled, latched to AO
X	X	H	H	L	L	Qn	Qn	$\overline{Qn}$	$\overline{Qn}$	Latched state to AO and B
H	–	L	L	L	L	H	L	H	L	Read back from AI to B to AO
L	–	L	L	L	L	L	H	L	H**	(both latches transparent)

Notes to function table for 74F8962
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. – = Input not externally driven
5. Z = High impedance "off' state
6. Q_n = High or low voltage level one setup time prior to the low–to–high $\overline{LEXX}$ transition.
7. H**= Goes to level of pullup voltage.
8. B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to low state.

FUNCTION TABLE FOR 74F8963

INPUTS						LATCH STATES		OUTPUTS		OPERATING MODE
AIn	Bn*	$\overline{LEAB}$	$\overline{LEBA}$	$\overline{OEAB}$	$\overline{OEBA}$	AB	BA	AOn	Bn	
H	H	L	L	H	H	L	L	Z	X	B and AO disabled
L	L	L	L	H	H	H	H	Z	X	
X	X	H	H	H	H	$\overline{Qn}$	$\overline{Qn}$	Z	X	
H	–	L	X	L	H	L	$\overline{Qn}$	Z	H	AO 3–state, transparent data from AI to B
L	–	L	X	L	H	H	$\overline{Qn}$	Z	L	
X	H	X	L	H	L	$\overline{Qn}$	L	H	X	B disabled, transparent data from B to AO
X	L	X	L	H	L	$\overline{Qn}$	H	L	X	
X	X	H	X	L	H	$\overline{Qn}$	$\overline{Qn}$	Z	$\overline{Qn}$	AO 3–state, latched data to B
X	X	X	H	H	L	$\overline{Qn}$	$\overline{Qn}$	Qn	X	B disabled, latched to AO
X	X	H	H	L	L	$\overline{Qn}$	$\overline{Qn}$	Qn	Qn	Latched state to AO and B
H	–	L	L	L	L	L	L	H	H**	Read back from AI to B to AO
L	–	L	L	L	L	H	L	L	L	(both latches transparent)

Notes to function table for 74F8963
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. – = Input not externally driven
5. Z = High impedance "off" state
6. Q_n = High or low voltage level one setup time prior to the low–to–high $\overline{LEXX}$ transition.
7. H**= Goes to level of pullup voltage.
8. B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEBA}$, $\overline{OEAB}$, $\overline{LEBA}$, $\overline{LEAB}$	–0.5 to +7.0	V
		AI0 – AI8, B0 – B8	–0.5 to +5.5	V
I_{IN}	Input current		–40 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	AO0 – AO8	48	mA
		B0 – B8	200	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Except B0 – B8	2.0			V
		B0 – B8	1.62			V
V_{IL}	Low–level input voltage	Except B0 – B8			0.8	V
		B0 – B8			1.47	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current	AO0 – AO8			–3	mA
I_{OL}	Low–level output current	AO0 – AO8			24	mA
		B0 – B8			100	mA
T_{amb}	Operating free air temperature		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
I_{OH}	High–level output current	B0 – B8	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power–off output current	B0 – B8	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	AO0 – AO8[4]	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –3mA		2.5		V_{CC}	V
V_{OL}	Low-level output voltage	AO0 – AO8[4]	V_{CC} = MIN,	I_{OL} = 24mA			0.50	V
		B0 – B8	V_{IL} = MAX	I_{OL} = 100mA	0.75	1.0	1.10	V
			V_{IH} = MIN	I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, $\overline{LEBA}$, AI0 – AI8	V_{CC} = MAX, V_I = 7.0V				100	µA
		B0 – B8	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High–level input current	$\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, $\overline{LEBA}$, AI0 – AI8	V_{CC} = MAX, V_I = 2.7V				20	µA
		B0 – B8	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low–level input current	$\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, $\overline{LEBA}$, AI0 – AI8	V_{CC} = MAX, V_I = 0.5V				–100	µA
		B0 – B8	V_{CC} = MAX, V_I = 0.3V				–100	µA
I_{OZH}	Off state output current, high–level voltage applied	AO0 – AO8	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short circuit output current[3]	AO0 – AO8	74F8962	V_{CC} = MAX, Bn = 1.3V, $\overline{OEBA}$ = 0.8V, $\overline{OEAB}$ = 2.7V	-60		-150	mA
		only	74F8963	V_{CC} = MAX, Bn = 1.8V, $\overline{OEBA}$ = 0.8V, $\overline{OEAB}$ = 2.7V				
I_{CC}	Supply current (total)	I_{CCH}		V_{CC} = MAX		80	110	mA
		I_{CCL}		V_{CC} = MAX, V_{IL} = 0.5V		105	145	mA
		I_{CCZ}				80	110	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} =1.8V and V_{IL} = 1.3V.

AC ELECTRICAL CHARACTERISTICS FOR 74F8962

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 5%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Bn to AOn	Waveform 1, 2	5.0 3.5	7.0 5.5	10.0 8.5	4.5 3.5	11.0 8.5	4.5 3.5	10.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to AOn	Waveform 1, 2	5.5 4.5	7.0 6.5	10.0 9.5	5.0 4.5	10.0 9.5	5.0 4.5	10.0 9.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low, $\overline{OEBA}$ to AOn	Waveform 5, 6	7.5 8.5	9.5 10.5	12.5 13.0	6.5 7.5	13.5 14.5	6.5 7.5	13.0 13.5	ns
t_{PHZ} t_{PLZ}	Output disable from high or low, $\overline{OEBA}$ to AOn	Waveform 5, 6	3.5 4.5	5.5 6.5	8.5 9.5	2.5 4.0	10.0 10.0	2.5 4.0	9.0 9.5	ns
$t_{sk(o)}$	Skew between receivers in same package	Waveform 4		1.5	2.0		4.0		4.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D = 30pF, R_U = 9Ω		T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 5%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay AIn to Bn	Waveform 1, 2	3.5 4.0	5.5 6.0	8.5 9.5	3.0 3.5	9.0 10.5	3.0 3.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to Bn	Waveform 1, 2	4.0 5.0	6.0 7.0	8.5 10.5	3.5 5.0	9.5 10.5	3.5 5.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Output enable/disable time $\overline{OEBA}$ to Bn	Waveform 1	3.5 3.0	5.0 4.0	8.0 8.0	3.0 2.5	8.5 8.5	3.0 2.5	8.0 8.5	ns
t_{TLH} t_{THL}	Transition time, Bn port 10% to 90%, 90% to 10%	Test circuit and waveforms	1.0 1.0	1.2 2.0	1.6 2.5	1.0 1.0	2.5 3.5	1.0 1.0	2.5 3.5	ns
$t_{sk(o)}$	Skew between drivers in same package	Waveform 4		0.5	2.5		3.0		3.0	ns

AC SETUP REQUIREMENTS FOR 74F8962

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 5%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low AIn to $\overline{LEAB}$	Waveform 3	3.0 1.0			3.5 2.0		3.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low AIn to $\overline{LEAB}$	Waveform 3	3.0 0.0			3.5 0.0		3.0 0.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Bn to $\overline{LEBA}$	Waveform 3	2.0 1.0			2.5 1.0		2.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Bn to $\overline{LEBA}$	Waveform 3	3.0 1.5			3.5 2.0		3.0 2.0		ns
$t_w(L)$	$\overline{LEAB}$ or $\overline{LEBA}$ pulse width, low	Waveform 3	4.5			4.5		4.5		ns

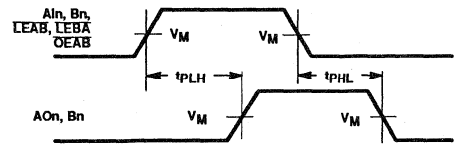
AC ELECTRICAL CHARACTERISTICS FOR 74F8963

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 5%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Bn to AOn	Waveform 1, 2	3.5 2.5	5.5 4.0	8.0 7.0	3.0 2.0	9.0 7.5	3.0 2.0	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to AOn	Waveform 1, 2	6.0 4.0	7.5 5.5	10.0 8.5	5.0 3.5	11.5 9.0	5.0 3.5	10.0 8.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low, $\overline{OEBA}$ to AOn	Waveform 5, 6	9.0 10.0	11.0 12.0	14.0 15.0	8.5 9.0	15.5 17.0	8.5 9.0	14.5 15.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low, $\overline{OEBA}$ to AOn	Waveform 5, 6	4.0 5.5	6.0 7.0	9.0 10.0	3.0 5.0	10.5 11.0	3.0 5.0	9.5 10.0	ns
$t_{sk(o)}$	Skew between receivers in same package	Waveform 4		1.5	2.0		4.0		4.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D = 30pF, R_U = 9Ω		T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 5%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay AIn to Bn	Waveform 1, 2	2.0 2.0	4.0 3.5	6.5 6.5	1.5 1.5	7.0 6.5	2.0 2.0	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to Bn	Waveform 1, 2	3.5 2.5	5.0 4.0	8.0 7.0	3.0 2.0	8.5 8.0	3.5 2.5	8.5 8.0	ns
t_{PLH} t_{PHL}	Output enable/disable time $\overline{OEBA}$ to Bn	Waveform 1	3.5 3.0	5.5 5.0	8.0 7.5	2.5 2.5	8.5 8.5	2.5 2.5	8.0 8.0	ns
t_{TLH} t_{THL}	Transition time, Bn port 10% to 90%, 90% to 10%	Test circuit and waveforms	1.0 1.0	1.2 2.0	1.6 2.5	1.0 1.0	2.5 3.5	1.0 1.0	2.5 3.5	ns
$t_{sk(o)}$	Skew between drivers in same package	Waveform 4		0.5	2.0		3.0		3.0	ns

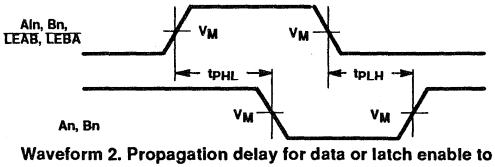
AC SETUP REQUIREMENTS FOR 74F8963

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 5%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low AIn to $\overline{LEAB}$	Waveform 3	4.0 1.0			4.5 1.5		4.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low AIn to $\overline{LEAB}$	Waveform 3	2.5 0.0			3.0 0.0		2.5 0.0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Bn to $\overline{LEBA}$	Waveform 3	2.0 1.0			2.5 1.0		2.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Bn to $\overline{LEBA}$	Waveform 3	2.5 1.0			3.0 1.5		3.0 1.0		ns
$t_w(L)$	$\overline{LEAB}$ or $\overline{LEBA}$ pulse width, low	Waveform 3	4.5			5.5		5.5		ns

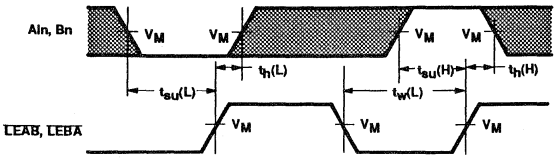
AC WAVEFORMS



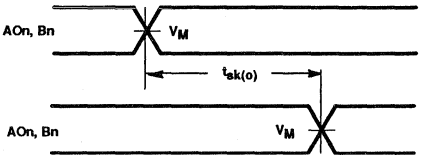
Waveform 1. Propagation delay for data or output enable or latch enable to output



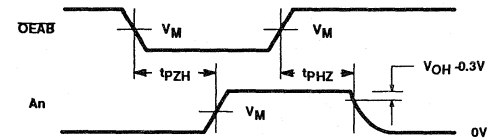
Waveform 2. Propagation delay for data or latch enable to output



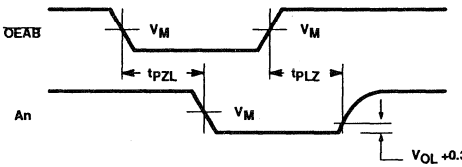
Waveform 3. Data setup and hold times and LEAB/LEBA pulse widths



Waveform 4. Output skew



Waveform 5. 3–state output enable time to high level and output disable time from high level



Waveform 6. 3-state output enable time to low level and output disable time from low level

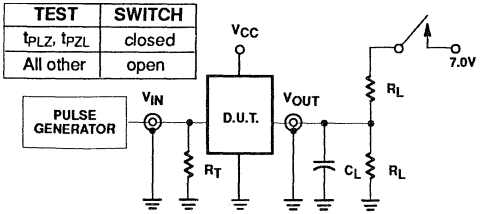
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

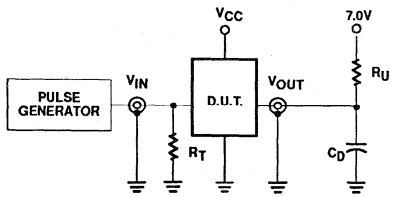
TEST CIRCUITS AND WAVEFORMS

SWITCH POSITION

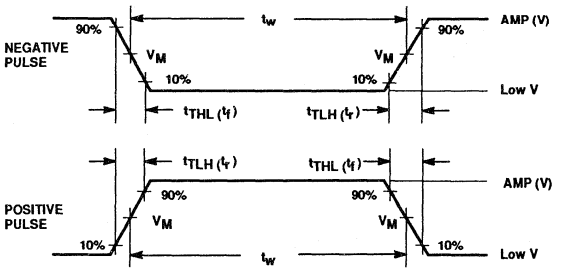
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–state outputs on A port



Test circuit for outputs on B port



Input pulse definition

family 74F	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	3.0V	1.0V	1.5V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_U = Pull up resistor; see AC electrical characteristics for value.
C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Futurebus address data transceiver

FAST 74F8965/74F8966

9–bit address/data futurebus transceiver, ADT

FEATURES

- 9–bit transceiver (both directions)
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1V to 2V) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE 896 futurebus standards and IEEE 1194 BTL standard
- Built–in precision band–gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch–free power up/power down operation
- Guaranteed skew of less than 2ns

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F8965	3.5ns	80mA
74F8966	3.5ns	80mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
44–pin PLCC	N74F8965A, N74F8966A

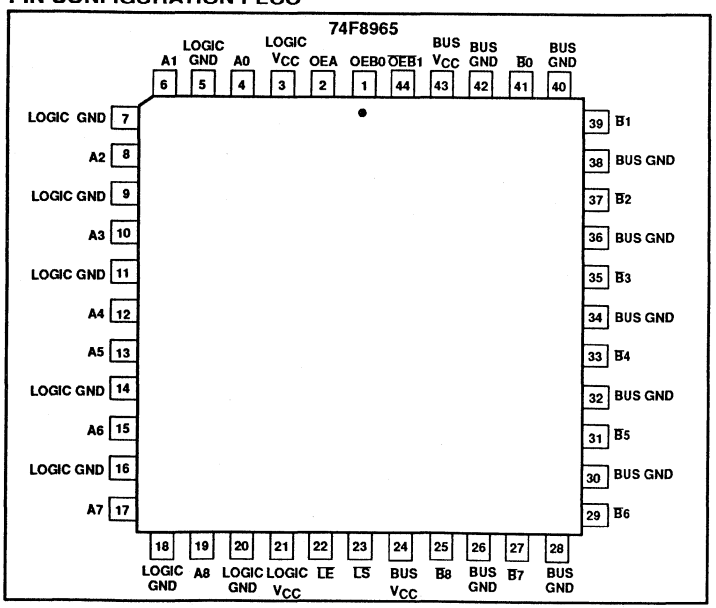
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A8	TTL data inputs	1.0/0.033	20µA/20µA
$\overline{B0}$ – $\overline{B8}$	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA, OEB0, $\overline{OEB1}$	Output enable inputs	1.0/0.167	20µA/100µA
$\overline{LS}$	Latch select (active low) ('F8965)	1.0/0.167	20µA/100µA
$\overline{IAREQ}$	Idle arbitration request (active low) ('F8965)	1.0/0.167	20µA/100µA
$\overline{LE}$	Latch enable input (active low)	1.0/0.167	20µA/100µA
A0 – A8	3–state TTL outputs	150/40	3mA/24mA
$\overline{B0}$ – $\overline{B8}$	Open collector BTL outputs	OC/166.7	OC/100mA
$\overline{IAMC}$	Idle arbitration/multiple competitors output ('F8966)	OC/80	OC/48mA

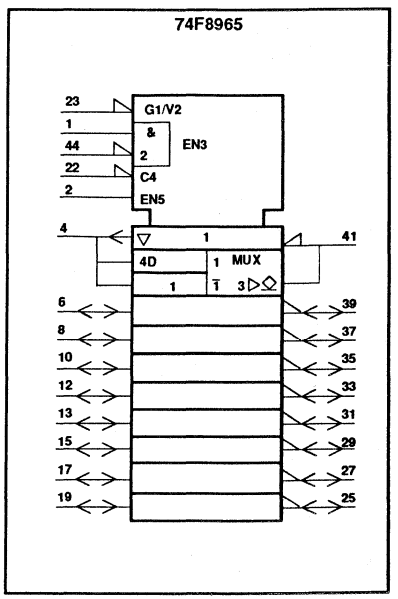
Notes to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.
2. OC = Open collector.

PIN CONFIGURATION PLCC



IEC/IEEE SYMBOL



Futurebus address data transceiver

FAST 74F8965/74F8966

DESCRIPTION

The 74F8965 and 74F8966 are 9–bit bidirectional latchable transceivers and are intended to provide the electrical interface to a high performance wired–OR bus. The B port inverting drivers are low–capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a precision band gap references for improved noise margins.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading.

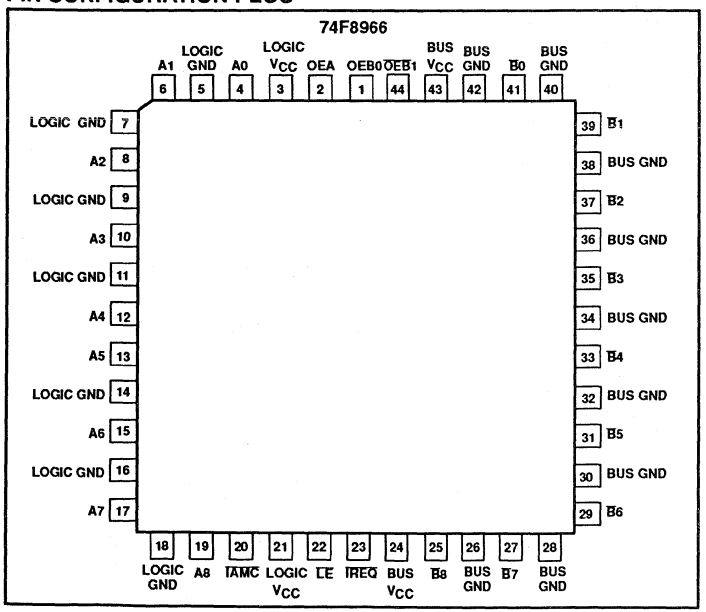
Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

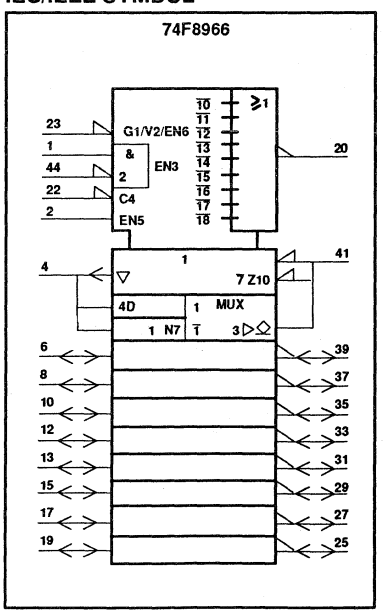
The 74F8965 and 74F8966 A ports have TTL 3–state drivers and TTL receivers.
The B ports have standard BTL I/O with 100mA current sink capability. The B–to–A path is a simple inverted buffered path. When going from A–to–B the user may choose between a buffered path or a latching function.

The 74F8966 also has an idle arbitrator/multiple competitors output. The $\overline{IAMC}$ output compares, using a wired–OR configuration, the data on the bus to the latched data presented to the bus. If the bus data matches the data presented by the 74F8966 then $\overline{IAMC}$ is high. If the data doesn't match then $\overline{IAMC}$ goes low.

PIN CONFIGURATION PLCC



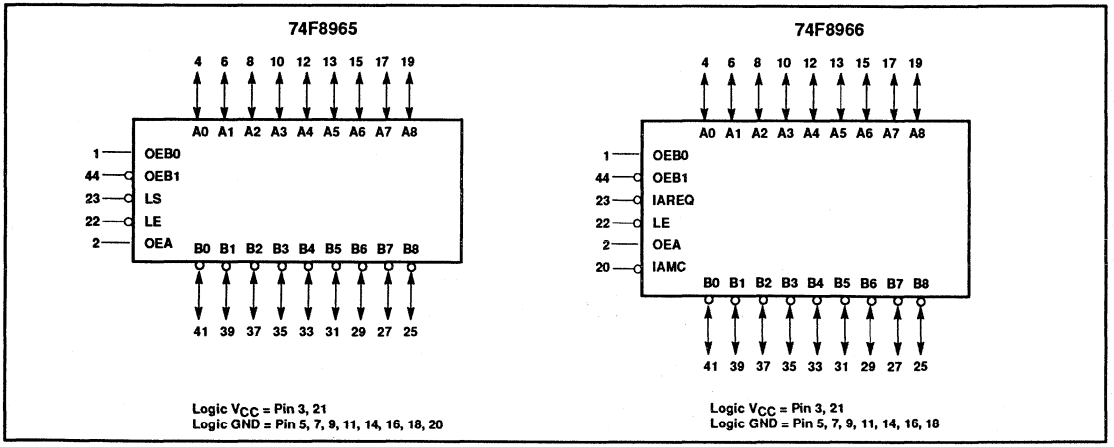
IEC/IEEE SYMBOL



Futurebus address data transceiver

FAST 74F8965/74F8966

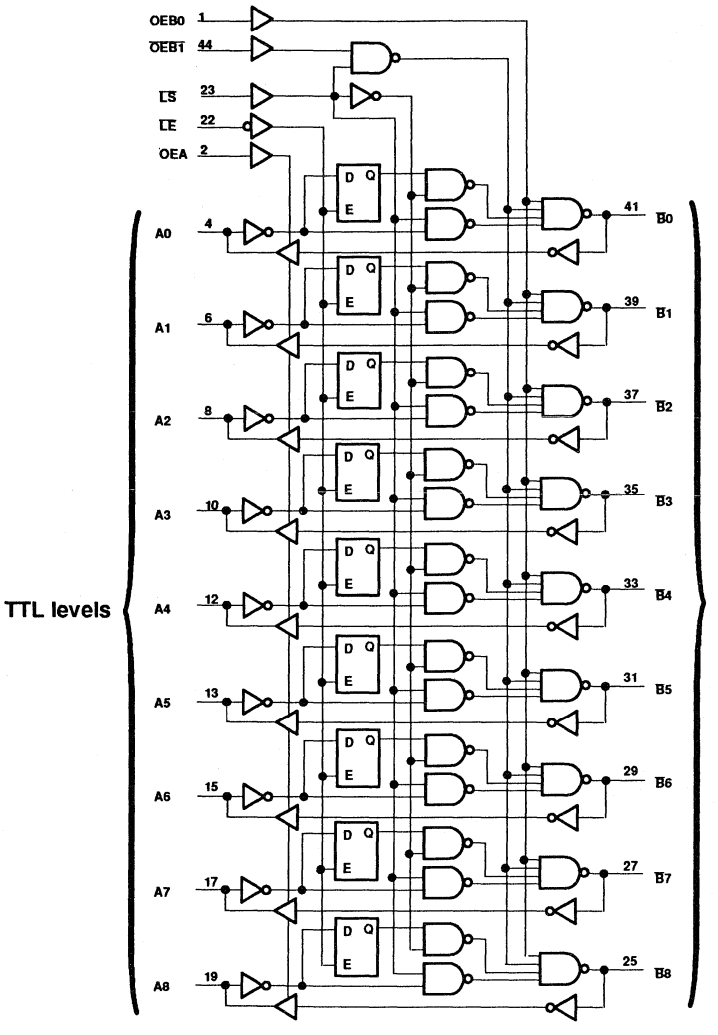
LOGIC SYMBOL



PIN DESCRIPTION

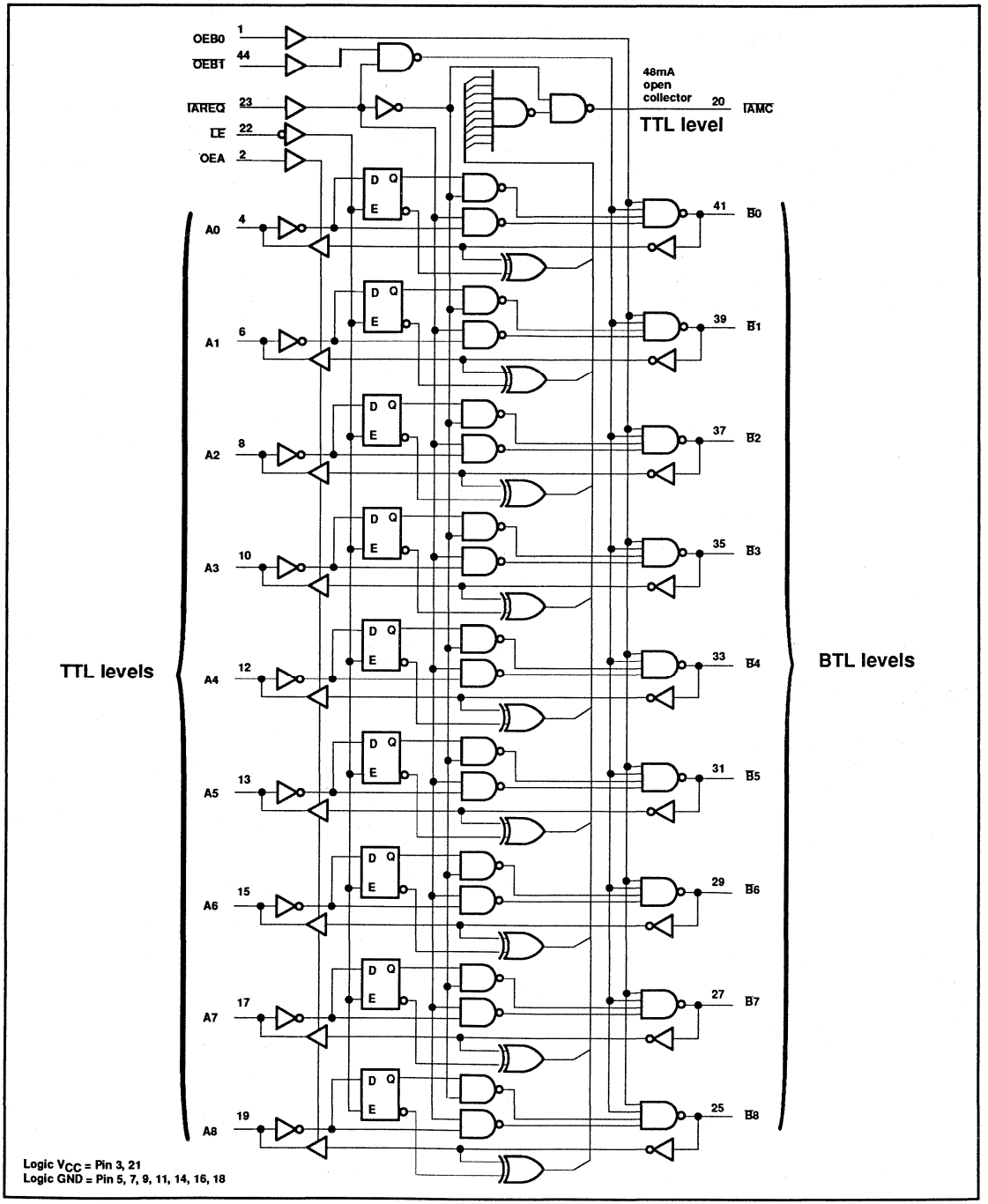
SYMBOL	PINS	TYPE	NAME AND FUNCTION
A0 – A8	4, 6, 8, 10, 12, 13, 15, 17, 19	I/O	Data inputs/TTL 3–state outputs
$\overline{B0}$ – $\overline{B8}$	41, 39, 37, 35, 33, 31, 29, 27, 25	I/O	Data inputs / open collector outputs, high current drives.
OEB0	1	Input	Output enable input. Enables the B outputs when high.
$\overline{OEB1}$	44	Input	Output enable input. Enables the B outputs when low.
OEA	2	Input	Output enable input. Enables the A outputs when high.
$\overline{LE}$	22	Input	Latch enable input. Enables latch when low.
$\overline{LS}$	23	Input	Latch select input. Selects latch when low (74F8965).
$\overline{IAREQ}$	23	Input	Idle arbitration request input (74F8966).
$\overline{IAMC}$	20	Output	Idle arbitration/multiple competitors output (open collector output) (74F8966).
Bus GND	26, 28, 30, 32, 34, 36, 38, 40, 42	Ground	Bus ground (0V)
Logic GND	5, 7, 9, 11, 14, 16, 18, 20 (74F8965)	Ground	Logic ground (0V)
Bus V_{CC}	24, 43	Power	Positive supply voltages
Logic V_{CC}	3, 21	Power	Positive supply voltages

LOGIC DIAGRAM FOR 74F8965



Logic V_{CC} = Pin 3, 21
Logic GND = Pin 5, 7, 9, 11, 14, 16, 18, 20

LOGIC DIAGRAM FOR 74F8966



FUNCTION TABLE FOR 74F8965

INPUTS							LATCH	OUTPUTS		OPERATING MODE
AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	$\overline{LS}$	OEA	$\overline{LE}$	STATE	An	$\overline{Bn}$	
L	–	H	L	H	L	X	X	input	H**	An to $\overline{Bn}$ bypass latch
H	–	H	L	H	L	X	X	input	L	
L	–	H	L	L	L	L	H	input	H**	An to $\overline{Bn}$ transparent latch
H	–	H	L	L	L	L	L	input	L	
l	–	H	L	L	L	↑	H	input	H**	An to $\overline{Bn}$ latch and read
h	–	H	L	L	L	↑	L	input	L	
–	–	H	L	L	H	H	H	L	H**	An to $\overline{Bn}$ outputs latched and read
–	–	H	L	L	H	H	L	H	L	(preconditioned latch)
X	–	H	L	L	L	H	NC	input	L	An to $\overline{Bn}$ hold
X	X	L	X	X	X	X	X	X	H**	Disable $\overline{Bn}$ outputs
X	X	X	H	H	X	X	X	X	H**	
–	L	L	H	H	H	X	X	H	input	$\overline{Bn}$ to An
–	H	L	H	H	H	X	X	L	input	
–	X	X	X	X	L	X	X	Z	X	Disable An outputs

Notes to function table for 74F8965
1. H = High voltage level
2. h = High voltage level one setup time prior to the low–to–high $\overline{LE}$ transition
3. L = Low voltage level
4. l = Low voltage level one setup time prior to the low–to–high $\overline{LE}$ transition
5. NC= No change
6. X = Don't care
7. Z = High impedance "off' state
8. – = Input not externally driven
9. ↑ = Low–to–high transition
10. H**= Goes to level of pullup voltage.
11. B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to low state.

FUNCTION TABLE FOR 74F8966

INPUTS								LATCH	OUTPUTS			OPERATING MODE
AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	$\overline{IAREQ}$	$\overline{LS}$	OEA	$\overline{LE}$	STATE	An	$\overline{Bn}$	$\overline{IAMC}$	
L	–	H	L	L	H	L	X	X	input	H**	H**	An to $\overline{Bn}$ bypass latch
H	–	H	L	L	H	L	X	X	input	L	H**	
L	–	H	L	L	L	L	L	H	input	H**	H**	An to $\overline{Bn}$ transparent latch
H	–	H	L	L	L	L	L	L	input	L	H**	
l	–	H	L	L	L	L	↑	H	input	H**	H**	An to $\overline{Bn}$ latch and read
h	–	H	L	L	L	L	↑	L	input	L	H**	
–	–	H	L	L	L	H	H	H	L	H**	H**	An to $\overline{Bn}$ outputs latched and read
–	–	H	L	L	L	H	H	L	H	L	H**	(preconditioned latch)
X	–	H	L	L	L	L	H	NC	input	NC	H**	An to $\overline{Bn}$ hold
X	X	L	X	X	X	X	X	X	X	H**	H**	Disable $\overline{Bn}$ outputs
X	X	X	H	H	H	X	X	X	X	H**	H**	
–	L	L	H	H	H	H	X	X	H	input	H**	$\overline{Bn}$ to An
–	H	L	H	H	H	H	X	X	L	input	H**	
–	Bn	L	H	H	↓*	H	H	$\overline{Bn}$	Z	Bn	L	Latch $\overline{Bn}$ data idle arbitration request
–	Bn	L	H	H	↓*	H	H	$\overline{Bn}$	Z	Bn	H**	(preconditioned latch)
–	X	X	X	X	X	L	X	X	Z	X	X	Disable An outputs

Notes to function table for 74F8966

1. H = High voltage level
2. h = High voltage level one setup time prior to the low–to–high $\overline{LE}$ transition
3. L = Low voltage level
4. l = Low voltage level one setup time prior to the low–to–high $\overline{LE}$ transition
5. NC= No change
6. X = Don't care
7. Z = High impedance "off' state
8. – = Input not externally driven
9. ↑ = Low–to–high transition
10. ↓* = High–to–low transition, latch must be preconditioned before $\overline{AREQ}$
11. H**= Goes to level of pullup voltage.
12. B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB0}$, $\overline{OEB1}$, LEA, $\overline{LE}$	–0.5 to +7.0	V
		A0 – A8, $\overline{B0}$ – $\overline{B8}$	–0.5 to +5.5	V
I_{IN}	Input current		–40 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output	A0 – A8	48	mA
		$\overline{AMC}$ (74F8966 only)	96	mA
		$\overline{B0}$ – $\overline{B8}$	200	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Except $\overline{B0}$ – $\overline{B8}$	2.0			V
		$\overline{B0}$ – $\overline{B8}$	1.625	1.55		V
V_{IL}	Low–level input voltage	Except $\overline{B0}$ – $\overline{B8}$			0.8	V
		$\overline{B0}$ – $\overline{B8}$			1.475	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	A0 – A8			–3	mA
V_{OH}	High–level output voltage	$\overline{AMC}$ (74F8966 only)	4.5			V
I_{OL}	Low–level output current	A0 – A8			24	mA
		$\overline{AMC}$ (74F8966 only)			48	mA
		$\overline{B0}$ – $\overline{B8}$			100	mA
T_{amb}	Operating free air temperature		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
I_{OH}	High–level output current	$\overline{B0} - \overline{B8}$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
		$\overline{IAMC}$ (74F8966)	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 4.5V				100	µA
I_{OFF}	Power–off output current	$\overline{B0} - \overline{B8}$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
		$\overline{IAMC}$ (74F8966)	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 4.5V				100	µA
V_{OH}	High-level output voltage	A0 – A8[4]	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –3mA		2.4		V_{CC}	V
V_{OL}	Low-level output voltage	A0 – A8[4]	V_{CC} = MIN,	I_{OL} = 24mA			0.50	V
		$\overline{IAMC}$ (74F8966)	V_{IL} = MAX	I_{OL} = 48mA			0.50	V
		$\overline{B0} - \overline{B8}$	V_{IH} = MIN	I_{OL} = 100mA	0.75	1.0	1.10	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	OEB0, $\overline{OEB1}$, OEA, $\overline{LE}$, $\overline{LS}$, $\overline{IAREQ}$	V_{CC} = MAX, V_I = 7.0V				100	µA
		A0 – A8, $\overline{B0}$ – $\overline{B8}$	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High–level input current	OEB0, $\overline{OEB1}$, OEA, $\overline{LE}$, $\overline{LS}$, $\overline{IAREQ}$	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{B0} - \overline{B8}$	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low–level input current	OEB0, $\overline{OEB1}$, OEA, $\overline{LE}$, $\overline{LS}$, $\overline{IAREQ}$	V_{CC} = MAX, V_I = 0.5V				–100	µA
		$\overline{B0} - \overline{B8}$	V_{CC} = MAX, V_I = 0.3V				–100	µA
$I_{IH} + I_{OZH}$	Off–state output current, high–level voltage applied	A0 – A8	V_{CC} = MAX, V_O = 2.7V				50	µA
$I_{IL} + I_{OZL}$	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short circuit output current[3]	A0 – A8 only	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			80	140	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			85	145	mA
		I_{CCZ}				75	100	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} =1.8V and V_{IL} = 1.3V.

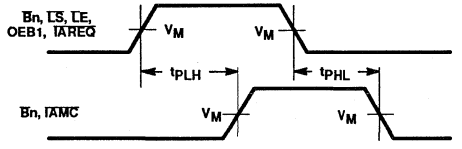
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay $\overline{B}n$ to An	Waveform 2	3.0 2.5	5.0 4.5	8.0 7.5	2.5 2.5	8.5 8.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low, OEA to An	Waveform 5, 6	7.5 9.0	9.0 11.0	12.0 13.5	6.0 7.5	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output disable from high or low, OEA to An	Waveform 5, 6	3.0 4.0	5.0 6.0	8.0 9.0	2.5 4.0	9.0 10.0	ns
$t_{sk(o)}$	Skew between receivers in same package	Waveform 4		0.5	1.0		1.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{B}n$ (transparent latch)	Waveform 2	2.5 3.0	4.0 5.0	7.0 7.5	2.0 2.5	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{B}n$ (bypass latch)	Waveform 2	1.0 1.5	3.0 3.0	5.5 5.5	1.0 1.0	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to $\overline{B}n$	Waveform 1, 2	3.0 4.0	5.0 5.5	8.0 8.5	3.0 3.5	8.5 9.5	ns
t_{PLH} t_{PHL}	Output enable/disable time, OEB0 to $\overline{B}n$	Waveform 2	4.0 5.0	6.0 6.5	8.5 9.5	3.5 3.5	10.0 11.5	ns
t_{PLH} t_{PHL}	Output enable/disable time, $\overline{OEB}$1 to $\overline{B}n$	Waveform 1	5.5 3.0	7.5 5.0	10.0 8.0	5.0 2.5	11.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{IAREQ}$ or $\overline{LS}$ to $\overline{B}n$	Waveform 1, 2	4.5 2.0	7.5 6.5	10.0 9.5	4.0 2.0	11.0 11.0	ns
t_{TLH} t_{THL}	Transition time, $\overline{B}n$ port 10% to 90%, 90% to 10%	Test circuit and waveforms		2.0 2.0		1.0 1.0	3.0 3.0	ns
$t_{sk(o)}$	Skew between drivers in same package	Waveform 4		1.0	2.0		2.0	ns
SYMBOL	PARAMETER	TEST CONDITION	$\overline{IAMC}$ PORT LIMITS (74F8966 only)					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{IAMC}$ (latches preset)	Waveform 2	10.5 7.0	14.5 12.0	18.0 15.0	9.5 6.0	20.0 17.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{IAREQ}$ to $\overline{IAMC}$	Waveform 2	6.5 2.5	8.0 4.5	11.0 7.0	6.0 2.0	11.5 8.0	ns

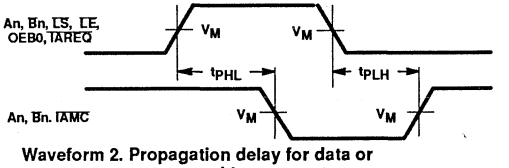
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to $\overline{LE}$	Waveform 3	2.5 0.0			3.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to $\overline{LE}$	Waveform 3	4.0 2.5			5.0 3.0		ns
$t_w(L)$	$\overline{LE}$ pulse width, low	Waveform 3	4.0			4.5		ns

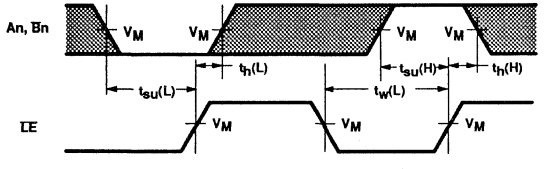
AC WAVEFORMS



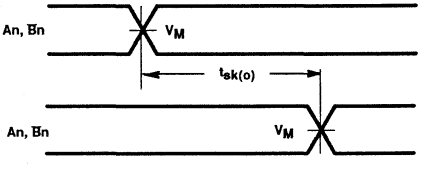
Waveform 1. Propagation delay for data or output enable to output



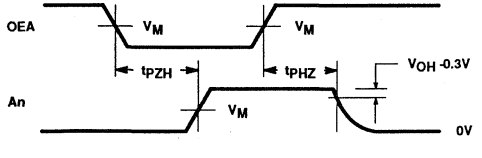
Waveform 2. Propagation delay for data or output enable to output



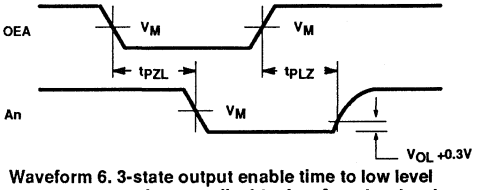
Waveform 3. Data setup and hold times and $\overline{LE}$ pulse width



Waveform 4. Output skew



Waveform 5. 3–state output enable time to high level and output disable time from high level



Waveform 6. 3-state output enable time to low level and output disable time from low level

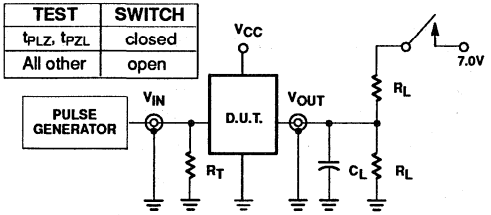
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

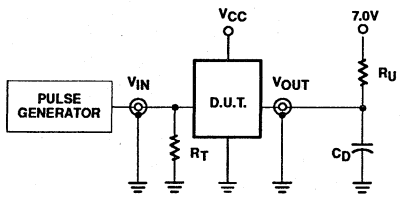
TEST CIRCUITS AND WAVEFORMS

SWITCH POSITION

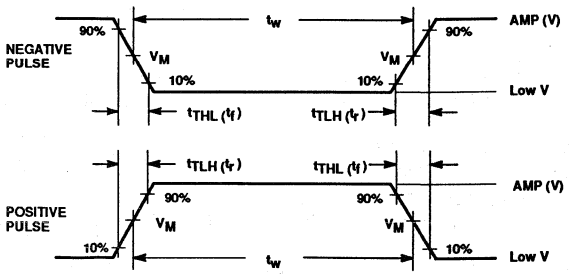
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–state outputs on A port



Test circuit for outputs on B port



Input pulse definition

family 74F	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	3.0V	1.0V	1.5V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_U = Pull up resistor; see AC electrical characteristics for value.
C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Philips Semiconductors-Signetics

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Date of issue	September 15, 1989
Status	Product Specification
FAST Products	

FAST 74F30240,74F30244 30Ω Line Drivers

'F30240 Octal 30Ω Line Driver With Enable, Inverting (Open Collector)
'F30244 Octal 30Ω Line Driver With Enable, Non-Inverting (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30240	9.5ns	62.5mA
74F30244	10.5ns	69mA

FEATURES

- **Ideal for driving transmission lines or backplanes. 160mA I_{OL} ideal for applications with impedance as low as 30Ω**
- **Guaranteed threshold voltages on the incident wave while driving line as low as 30Ω.**
- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal interface**
- **'F30240 Inverting**
- **'F30244 Non-Inverting**
- **Open-Collector outputs sink 160mA**
- **Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)**
- **Available in 24-pin standard slim DIP (300mil) plastic, SOL or CERDIP packages**

DESCRIPTION

The 74F30240/F30244 are high current open collectors octal buffers composed of eight inverters. The 'F30240 has inverting data paths and the 'F30244 has non-inverting paths. Each device has eight inverters with two Output Enables($\overline{OE}_0$, $\overline{OE}_1$) each controlling four outputs. Both drivers are designed to deal with the low-impedance transmission line effects found on printed circuit boards when fast edge rates are used. The 160 mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Cerdip (300 mil)	N74F30240F, N74F30244F
24-Pin Plastic Slim DIP(300 mil)[1]	N74F30240N, N74F30244N
24-Pin Plastic SOL[2]	N74F30240D, N74F30244D

NOTE:
1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.
2. Because of the high current sinking capability of these parts, the SOL package should only be used under the following conditions: a) 50% duty cycle AND b) 3/5 of remaining 50% driving ≤ 100 mA (leaving the remaining 2/5 of the to drive ≤ 160 mA) OR c) use ≥ 450 linear feet per minute forced air or other thermal mounting techniques.

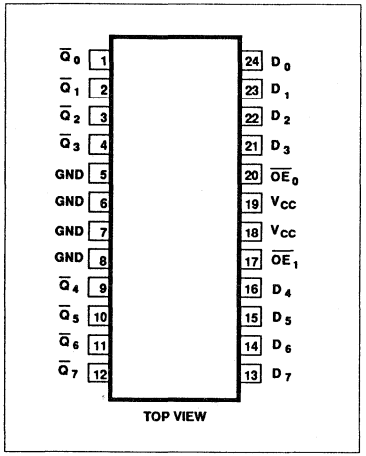
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$- $\overline{OE}_1$	Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{Q}_0$- $\overline{Q}_7$	Data outputs (OC) for 'F30240	OC/266.7	OC/160mA
Q_0- Q_7	Data outputs (OC) for 'F30244	OC/266.7	OC/160mA

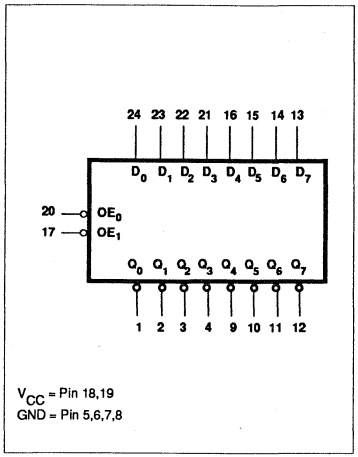
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

30Ω Line Drivers | FAST 74F30240. 74F30244

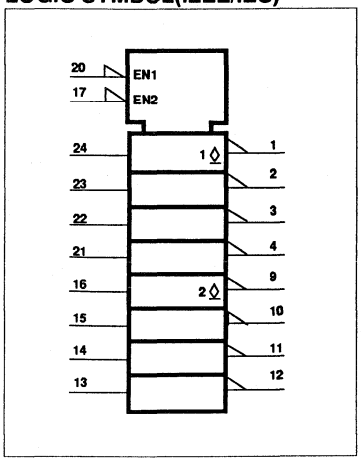
PIN CONFIGURATION



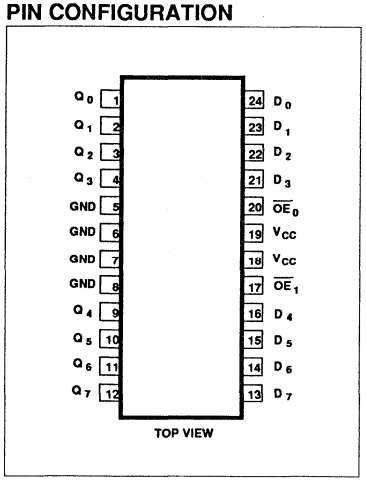
LOGIC SYMBOL



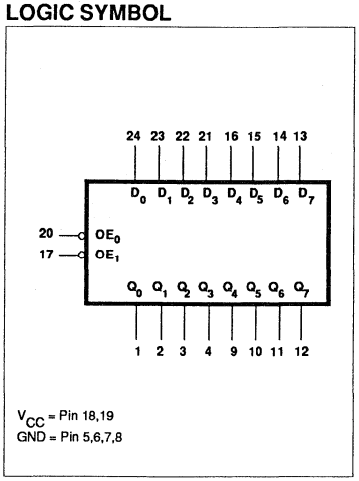
LOGIC SYMBOL(IEEE/IEC)



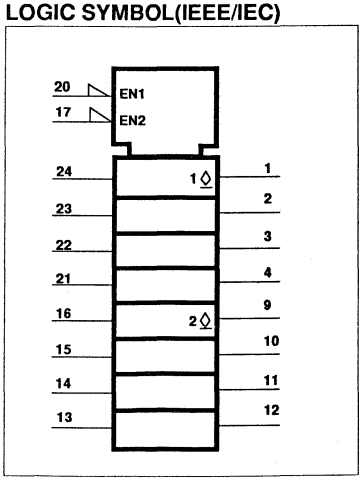
PIN CONFIGURATION



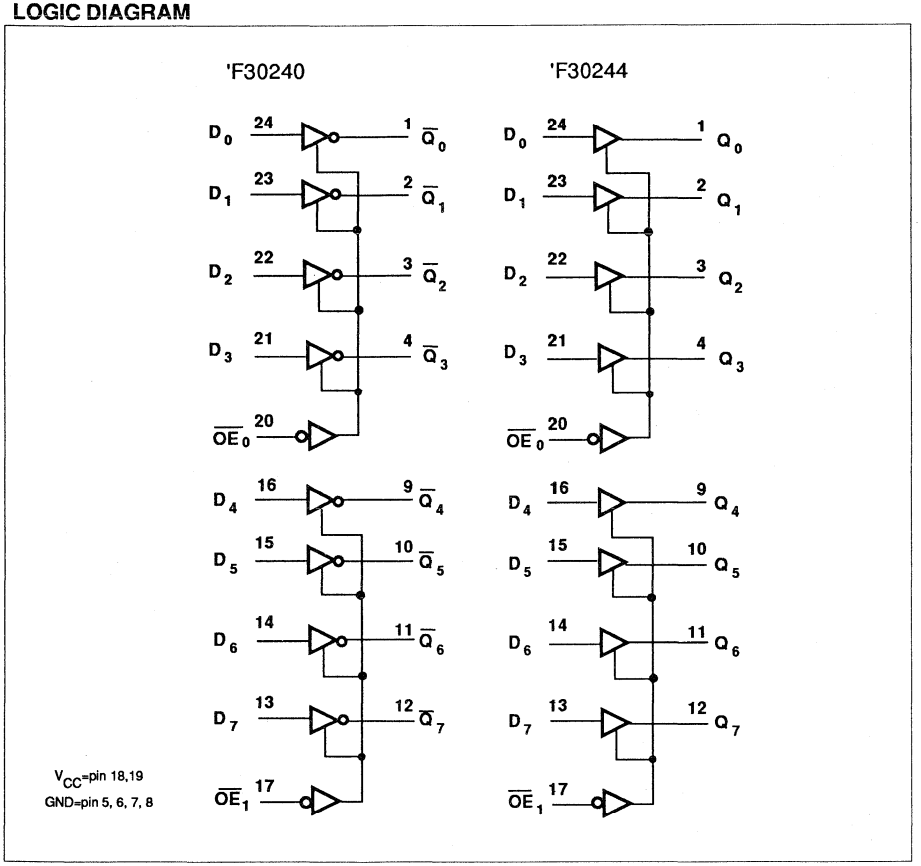
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS	
		'F30240	'F30244
$\overline{OE}_n$	D_n	$\overline{Q}_n$	Q_n
L	L	H	L
L	H	L	H
H	X	OFF	OFF

H=High voltage level
L=Low voltage level
X=Don't care
OFF=Pulled up through resistor (open collector)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		.42	.55	V
					I_{OL} = 160mA[3]	±5%V_{CC}			.80	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{CC}	Supply current [total]	'F30240	I_{CCH}	V_{CC} = MAX				13	23	mA
			I_{CCL}					70	95	mA
		'F30244	I_{CCH}					19	27	mA
			I_{CCL}					70	100	mA

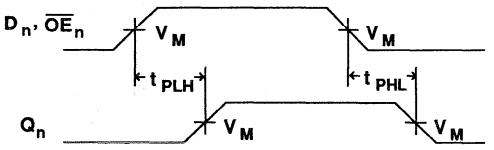
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

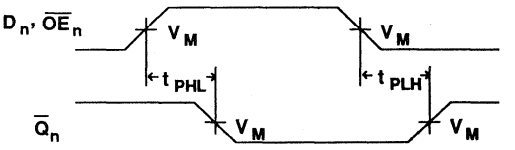
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F30240	Waveform 2	4.0 1.0	10.0 2.0	14.5 5.0	4.0 1.0	15.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 1,2	4.0 3.5	10.0 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F30244	Waveform 1	4.0 3.0	10.5 5.5	14.5 9.0	4.0 3.0	15.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 1,2	4.0 3.5	9.5 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns

AC WAVEFORMS



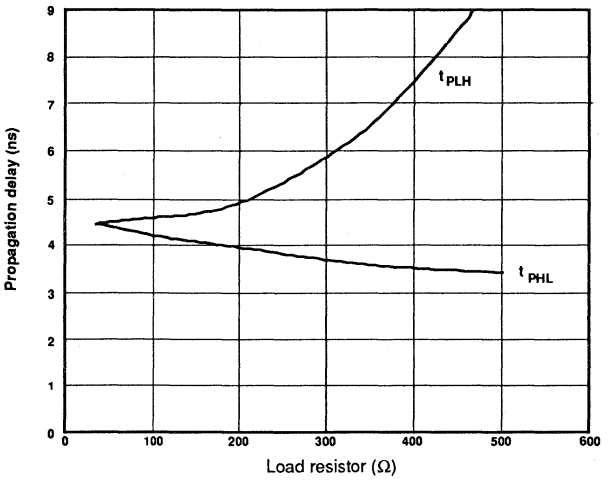
Waveform 1. Propagation Delay For Data To Output



Waveform 2. Propagation Delay For Data To Output

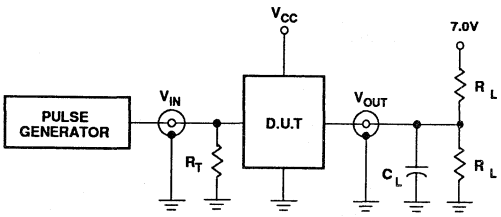
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

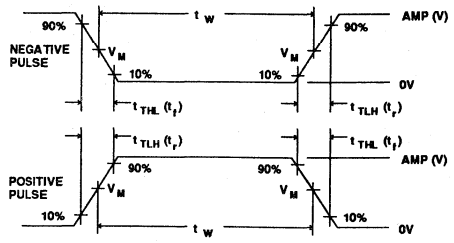


NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Synchronizing dual J–$\overline{K}$ positive edge-triggered flip-flop with metastable immune characteristics

74F50109

FEATURE

- Metastable immune characteristics
- Output skew guaranteed less than 1.5ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- Pinout compatible with 74F109
- See 74F5074 for synchronizing dual D-type flip-flop
- See 74F50728 for synchronizing cascaded D-type flip-flop
- See 74F50729 for synchronizing dual D-type flip-flop with edge-triggered set and reset

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F50109	150MHz	22mA

ORDERING INFORMATION

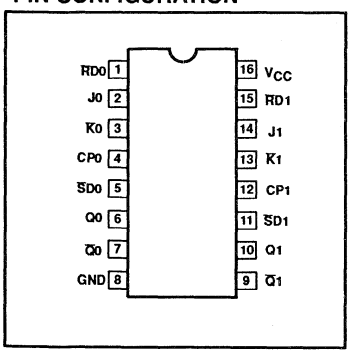
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16–pin plastic DIP	N74F50109N
16–pin plastic SO	N74F50109D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

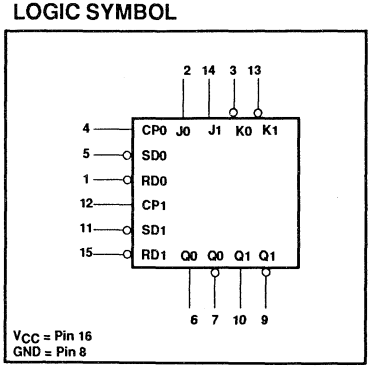
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
J0, J1	J inputs	1.0/0.417	20µA/250µA
$\overline{K}$0, $\overline{K}$1	K inputs	1.0/0.417	20µA/250µA
CP0, CP1	Clock inputs (active rising edge)	1.0/0.033	20µA/20µA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active low)	1.0/0.033	20µA/20µA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active low)	1.0/0.033	20µA/20µA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	750/33	15mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

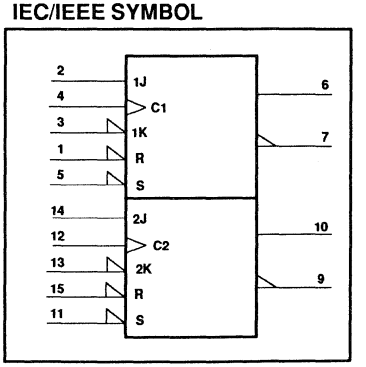
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



Synchronizing dual J–$\overline{K}$ positive edge-triggered flip-flop with metastable immune characteristics

74F50109

DESCRIPTION

The 74F50109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, clock, set, and reset inputs; also true and complementary outputs.

Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock (CP) input.

The J and $\overline{K}$ are edge–triggered inputs which control the state changes of the flip–flops as described in the function table.
The J and $\overline{K}$ inputs must be stable just one setup time prior to the low–to–high transition of the clock for guaranteed propagation delays. The J$\overline{K}$ design allows operation as a D flip–flop by tying J and $\overline{K}$ inputs together.
The 74F50109 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50109 are: $\tau \cong 135$ps and $\tau \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

METASTABLE IMMUNE CHARACTERISTICS

Signtetics uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family. Specifically the 74F50XXX family presently consist of 4 products which displays metastable immune characteristics. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations.

This claim is easily verified on the 74F5074. By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10MHz clock and 10.02 MHz data) the device–under–test can be often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform.0 An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device–under–test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Fig. 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5V volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device–under–test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will appear as in Fig. 3. The 74F5074 Q output will not vary with respect to the Q trigger point even when the a part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Components–Signetics patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased clock–to–Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_0.

The metastability characteristics of the 74F5074 and related part types represent state–of–the–art TTL technology.

After determining the T_0 and t of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74F50729 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74F50109 10 nanoseconds after the clock edge. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/\tau)} / T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' < h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula MTBF is 1.51×10^{10} seconds or about 480 years.

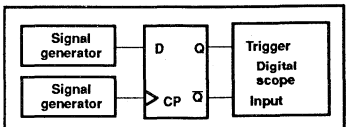


Figure 20. Test setup

COMPARISON OF METASTABLE IMMUNE AND NON–IMMUNE CHARACTERISTICS

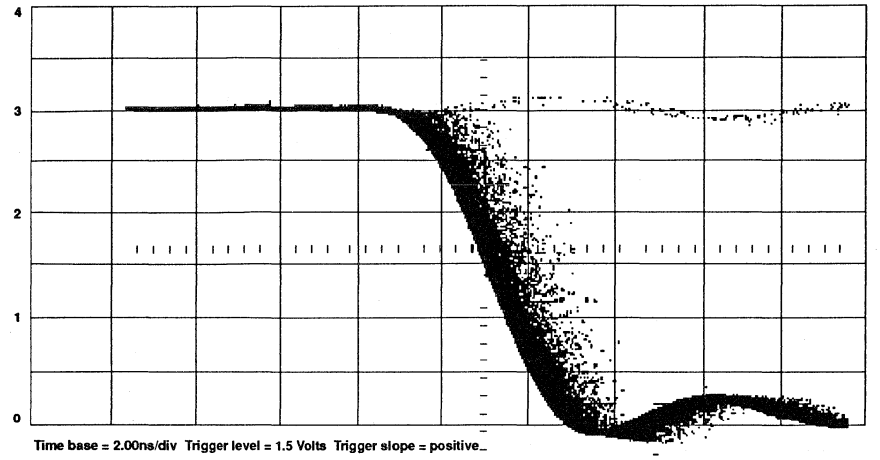


Figure 21. 74F74 $\overline{Q}$ output triggered by Q output, Setup and Hold times violated

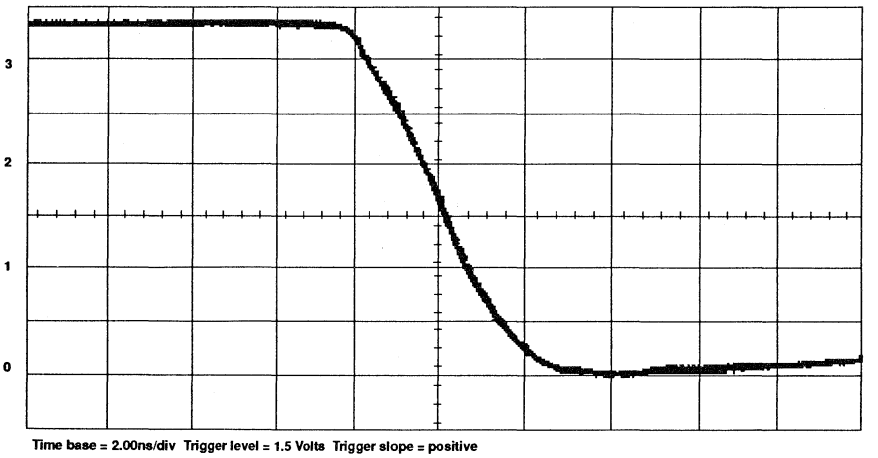


Figure 22. 74F74 $\overline{Q}$ output triggered by Q output, Setup and Hold times violated

MEAN TIME BETWEEN FAILURES (MTBF) VERSUS t'

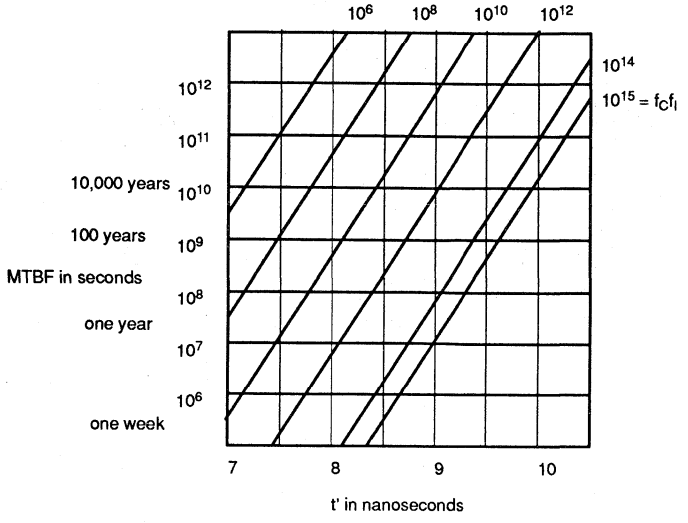


Figure 23.

NOTE: V_{CC} = 5V, T_{amb} = 25°C, τ =135ps, To = 9.8 X 10^8 sec

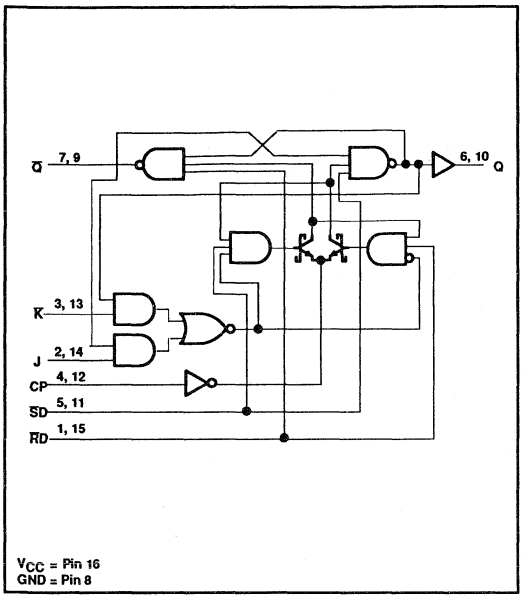
TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.5V	125ps	1.0 X 10^9 sec	138ps	5.4 X 10^6 sec	160ps	1.7 X 10^5 sec
5.0V	115ps	1.3 X 10^{10} sec	135ps	9.8 X 10^6 sec	167ps	3.9 X 10^4 sec
4.5V	115ps	3.4 X 10^{13} sec	132ps	5.1 X 10^8 sec	175ps	7.3 X 10^4 sec

Synchronizing dual J–$\overline{K}$ positive edge-triggered flip-flop with metastable immune characteristics

74F50109

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	J	$\overline{K}$	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous set
H	L	X	X	X	L	H	Asynchronous reset
L	L	X	X	X	H	H	Undetermined*
H	H	↧	X	X	q	$\overline{q}$	Hold
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	h	h	H	L	Load "1" (set)
H	H	↑	l	l	L	H	Load "0" (reset)
H	H	↑	l	h	q	$\overline{q}$	Hold 'no change"

NOTES:
1. H = High–voltage level
2. h = High–voltage level one setup time prior to low–to–high clock transition
3. L = Low–voltage level
4. l = Low–voltage level one setup time prior to low–to–high clock transition
5. q = Lower case indicate the state of the referenced output prior to the low–to–high clock transition
6. X = Don't care
7. ↑ = Low–to–high clock transition
8. ↧ = Not low–to–high clock transition
9. * = Both outputs will be high if both $\overline{SD}$ and $\overline{RD}$ go low simultaneously

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

Synchronizing dual J–$\overline{K}$ positive edge-triggered flip-flop with metastable immune characteristics

74F50109

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Jn, $\overline{K}$n	V_{CC} = MAX, V_I = 0.5V					-250	µA
		CPn, $\overline{SD}$n, $\overline{RD}$n	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				22	32	mA

NOTES:

3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
4. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

Synchronizing dual J–$\overline{K}$ positive edge-triggered flip-flop with metastable immune characteristics

74F50109

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	130	150		90		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	3.8 3.8	6.0 6.0	2.0 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, $\overline{R}$Dn to Qn or $\overline{Q}$n	Waveform 2	3.5 3.5	5.5 5.5	8.0 8.0	3.0 3.0	8.5 8.5	ns
$t_{sk(o)}$	Output skew[1, 2]	Waveform 4			1.5		1.5	ns

NOTES:

1. $|t_{PN}$ actual $- t_{PM}$ actual$|$ for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

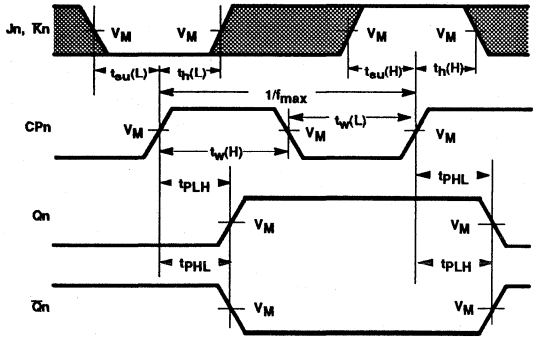
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Jn, $\overline{K}$n to CPn	Waveform 1	1.5 1.5			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low Jn, $\overline{K}$n to CPn	Waveform 1	1.0 1.0			1.5 1.5		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 1	3.0 4.0			3.5 5.0		ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn pulse width, low	Waveform 2	3.5			4.0		ns
t_{rec}	Recovery time $\overline{S}$Dn or $\overline{R}$Dn to CP	Waveform 3	3.0			3.5		ns

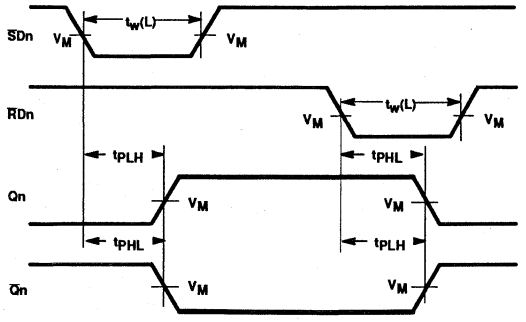
Synchronizing dual J–$\overline{K}$ positive edge-triggered flip-flop with metastable immune characteristics

74F50109

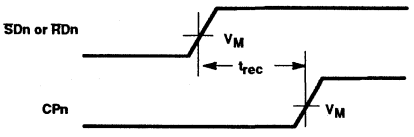
AC WAVEFORMS



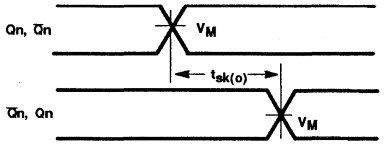
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width



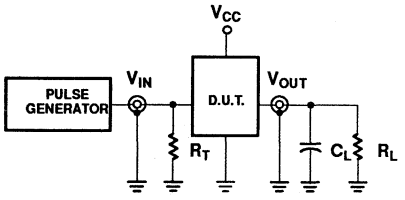
Waveform 3. Recovery time for set or reset to output



Waveform 4. Output skew

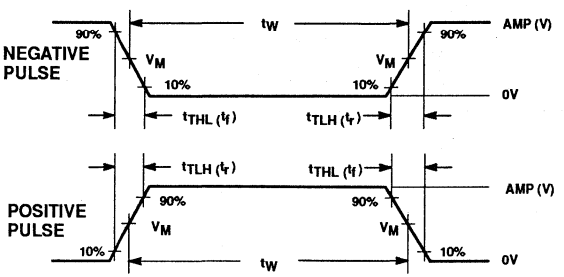
NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test circuit for totem-pole outputs

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Synchronizing cascaded dual positive edge-triggered D-type flip-flop

74F50728

FEATURES

- Metastable immune characteristics
- Output skew less than 1.5ns
- See 74F5074 for synchronizing dual D-type flip-flop
- See 74F50109 for synchronizing dual J–K positive edge-triggered flip-flop
- See 74F50729 for synchronizing dual dual D-type flip-flop with edge-triggered set and reset
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F50728 is a cascaded dual positive edge–triggered D–type featuring individual data, clock, set and reset inputs; also true and complementary outputs.

Set ($\overline{S}$Dn) and reset ($\overline{R}$Dn) are asynchronous active low inputs and operate independently of the clock (CPn) input. They set and reset both flip–flops of a cascaded pair simultaneously. Data must be stable just one setup time prior to the low–to–high transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive–going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output. Data entering the 74F50728 requires two clock cycles to arrive at the outputs.

The 74F50728 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50728 are: $\tau \cong 135$ps and $T_0 \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50728	145 MHz	23mA

ORDERING INFORMATION

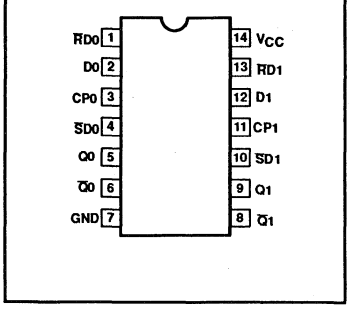
DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F50728N	I74F50728N
14–pin plastic SO	N74F50728D	I74F50728D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

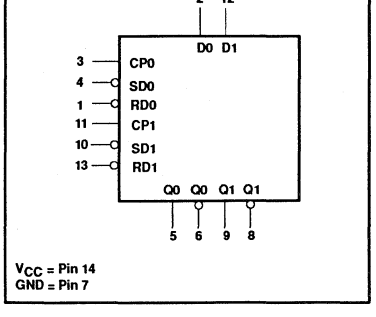
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
D0, D1	Data inputs	1.0/0.417	20µA/250µA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/20µA
$\overline{S}$D0, $\overline{S}$D1	Set inputs (active low)	1.0/1.0	20µA/20µA
$\overline{R}$D0, $\overline{R}$D1	Reset inputs (active low)	1.0/1.0	20µA/20µA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

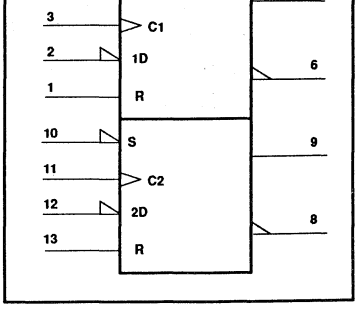
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



Synchronizing cascaded dual positive edge-triggered D-type flip-flop

74F50728

SYNCHRONIZING SOLUTIONS

Synchronizing incoming signals to a system clock has proven to be costly, either in terms of time delays or hardware. The reason for this is that in order to synchronize the signals a flip–flop must be used to "capture" the incoming signal. While this is perhaps the only way to synchronize a signal, to this point, there have been problems with this method. Whenever the flop's setup or hold times are violated the flop can enter a metastable state causing the outputs in turn to glitch, oscillate, enter an intermediate state or change state in some abnormal fashion. Any of these conditions could be responsible for causing a system crash. To minimize this risk, flip–flops are often cascaded so that the input signal is captured on the first clock pulse and released on the second clock pulse (see Fig.1). This gives the first flop about one clock period minus the flop delay and minus the second flop's clock–to–Q setup time to resolve any metastable condition. This method greatly reduces the probability of the outputs of the synchronizing device displaying an abnormal state but the trade-off is that one clock cycle is lost to synchronize the incoming data and two separate flip–flops are required to produce the cascaded flop circuit. In order to assist the designer of synchronizing circuits Philips Components–Signetics is offering the 74F50728.

The 50728 consists of two pair of cascaded D–type flip–flops with metastable immune features and is pin compatible with the 74F74. Because the flops are cascaded on a single part the metastability characteristics are greatly improved over using two separate flops that are cascaded. The pin compatibility with the 74F74 allows for plug–in retrofitting of previously designed systems.

Because the probability of failure of the 74F50728 is so remote, the metastability characteristics of the part were empirically determined based on the characteristics of its sister part, the 74F5074. The table below shows the 74F5074 metastability characteristics.

Having determined the T_0 and τ of the flop, calculating the mean time between failures (MTBF) for the 74F50728 is simple. It is, however, somewhat different than calculating MTBF for a typical part because data requires two clock pulses to transit from the input to the output. Also, in this case a failure is considered of the output beyond the normal propagation delay.

Suppose a designer wants to use the flop for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), and is using a clock frequency of 50MHz. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/\tau)}/T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the period of the clock input (20 nanoseconds). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high data transitions. From Fig. 2 it is clear that the MTBF is greater than 10^{41} seconds. Using the above formula the actual MTBF is 2.23×10^{42} seconds or about 7×10^{34} years.

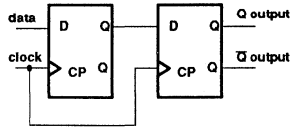


Figure 24.

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

	$T_{amb} = 0°C$		$T_{amb} = 25°C$		$T_{amb} = 70°C$	
	τ	T_0	τ	T_0	τ	T_0
$V_{CC} = 5.5V$	125ps	1.0×10^9 sec	138ps	5.4×10^6 sec	160ps	1.7×10^5 sec
$V_{CC} = 5.0V$	115ps	1.3×10^{10} sec	135ps	9.8×10^6 sec	167ps	3.9×10^4 sec
$V_{CC} = 4.5V$	115ps	3.4×10^{13} sec	132ps	5.1×10^8 sec	175ps	7.3×10^4 sec

MEAN TIME BETWEEN FAILURES VERSUS DATA FREQUENCY AT VARIOUS CLOCK FREQUENCY

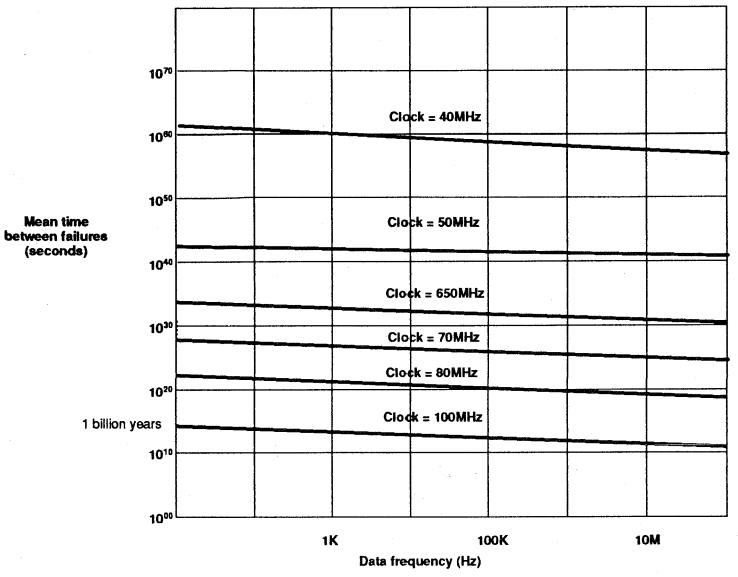
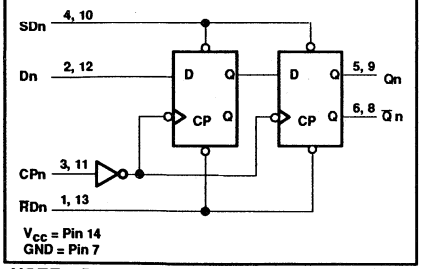


Figure 25.

NOTE: V_{CC} = 5V, T_{AMB} = 25°C, T = 135PS, TO = 9.8 X 10^8 SEC

LOGIC DIAGRAM



NOTE: Data entering the flip–flop requires two clock cycles to arrive at the output.

FUNCTION TABLE

INPUTS				INTERNAL REGISTER	OUTPUTS		OPERATING MODE
S̄Dn	R̄Dn	CPn	Dn	Q	Qn	Q̄n	
L	H	X	X	H	H	L	Asynchronous set
H	L	X	X	L	L	H	Asynchronous reset
L	L	X	X	X	H	H	Undetermined*
H	H	↑	h	h	H	L	Load "1"
H	H	↑	l	l	L	H	Load "0"
H	H	L	X	NC	NC	NC	Hold

NOTES:
1. H = High voltage level
2. h = High voltage level one setup time prior to low–to–high clock transition
3. L = Low voltage level
4. l = Low voltage level one setup time prior to low–to–high clock transition
5. NC = No change from the previous setup
6. X = Don't care
7. * = This setup is unstable and will change when either set of reset return to the high–level
8. ↑ = Low–to–high clock transition.
9. ** = Data entering the flip–flop requires two clock cycles to arrive at the output (see logic diagram)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.4			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–3	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TY.[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
			V_{IL} = MAX,		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Dn	V_{CC} = MAX, V_I = 0.5V					-250	µA
		CPn, $\overline{S}$Dn, $\overline{R}$Dn						–20	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX, V_O = 2.25V			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				23	34	mA

NOTES:

3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
4. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	145		85		70		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	3.8 3.8	6.0 6.0	1.5 2.0	6.5 6.5	1.5 2.0	7.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn $\overline{R}$Dn to Qn or $\overline{Q}$n	Waveform 2	3.5 3.5	5.0 5.0	8.0 8.0	3.0 3.0	9.0 8.5	3.0 3.0	10.5 10.0	ns
$t_{sk(o)}$	Output skew[1, 2]	Waveform 4			1.5		1.5		1.5	ns

NOTES TO AC ELECTRICAL CHARACTERISTICS

1. $|t_{PLH}$ actual $- t_{PHL}$ actual $|$ for any one output compare to any other output where N and M are either LH or HL.
2. Skew lines are valid only under same conditions (temperature, V_{CC}, loading, etc.,).

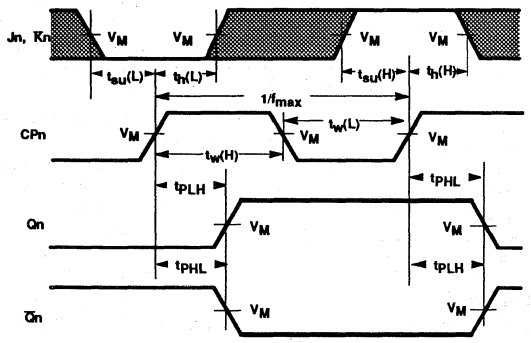
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to CPn	Waveform 1	1.5 1.5			2.0 2.0		2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	0.0 0.0			1.5 1.5		1.5 1.5		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 2	3.0 4.0			3.5 5.0		4.0 5.5		ns
t_w (L)	$\overline{S}$Dn, $\overline{R}$Dn pulse width, low	Waveform 2	4.5			4.0		4.5		ns
t_{rec}	Recovery time $\overline{S}$Dn, $\overline{R}$Dn to CPn	Waveform 3	3.5			3.5		3.5		ns

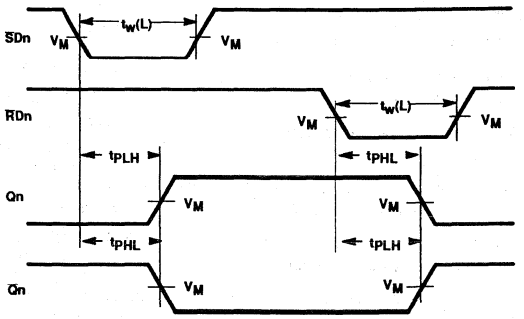
Synchronizing cascaded dual positive edge-triggered D-type flip-flop

74F50728

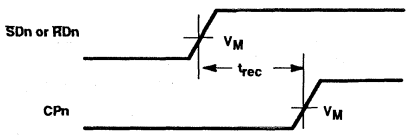
AC WAVEFORMS



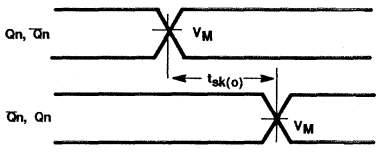
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width



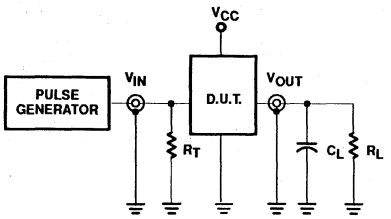
Waveform 3. Recovery time for set or reset to output



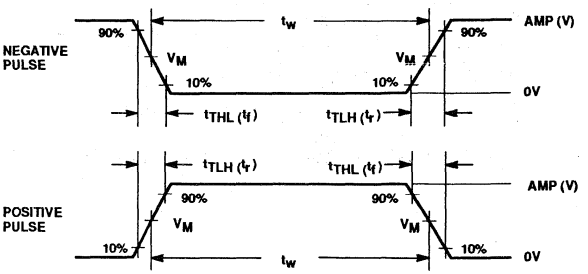
Waveform 4. Output skew

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics

74F50729

FEATURES

- Metastable immune characteristics
- Output skew less than 1.5ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- See 74F5074 for synchronizing dual D–type flip–flop
- See 74F50109 for synchronizing dual J–$\overline{K}$ positive edge–triggered flip–flop
- See 74F50728 for synchronizing cascaded dual D–type flip–flop
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F50729 is a dual positive edge–triggered D–type featuring individual data, clock, set and reset inputs; also true and complementary outputs.

The 74F50729 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50729 are: $\tau \cong 135$ps and $\tau \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_o represents a function of the measurement of the propensity of a latch to enter a metastable state.

Set (SDn) and reset (RDn) are asynchronous positive–edge triggered inputs and operate independently of the clock (CPn) input. Data must be stable just one setup time prior to the low–to–high transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive–going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50729	120 MHz	19mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
14–pin plastic DIP	N74F50729N	I74F50729N
14–pin plastic SO	N74F50729D	I74F50729D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

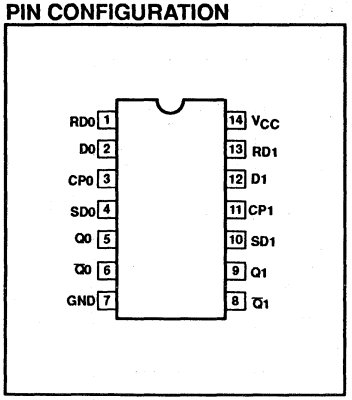
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
D0, D1	Data inputs	1.0/0.417	20µA/250µA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/20µA
SD0, SD1	Set inputs (active rising edge)	1.0/1.0	20µA/20µA
RD0, RD1	Reset inputs (active rising edge)	1.0/1.0	20µA/20µA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	750/33	15mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

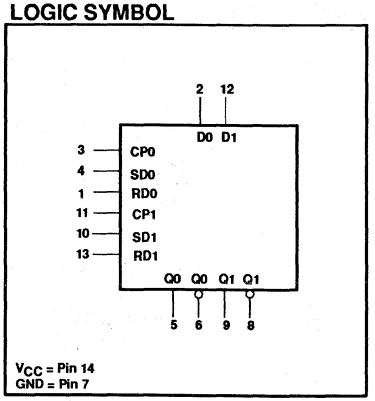
Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics

74F50729

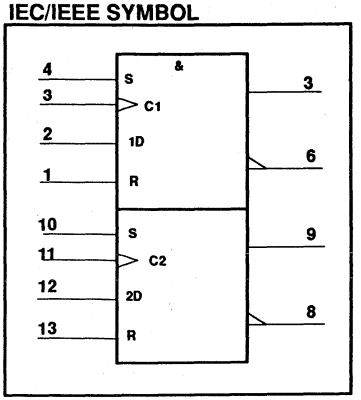
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



METASTABLE IMMUNE CHARACTERISTICS

Philips Components–Signetics uses the term 'metastable immune' to describe characteristics of some of the products in its family. Specifically the 74F50XXX family presently consist of 4 products which will not glitch or display metastable immune characteristics. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074. By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10MHz clock and 10.02 MHz data) the device–under–test can be often be driven into metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device–under–test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Figure 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5V volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volt, the trigger point of the scope.

When the device–under–test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will appear as in Fig. 3. The 74F5074 Q output will not vary with respect to the Q trigger point even when the a part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Components–Signetics patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased clock–to–Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_0.

The metastability characteristics of the 74F5074 and related part types represent state–of–the–art TTL technology.

After determining the T_0 and t of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74F50729 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74F50729 10 nanoseconds after the clock edge. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/\tau)} / T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' < h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51 X 10^{10} seconds or about 480 years.

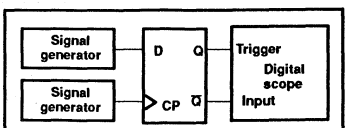


Figure 26. Test Setup

COMPARISON OF METASTABLE IMMUNE AND NON–IMMUNE CHARACTERISTICS

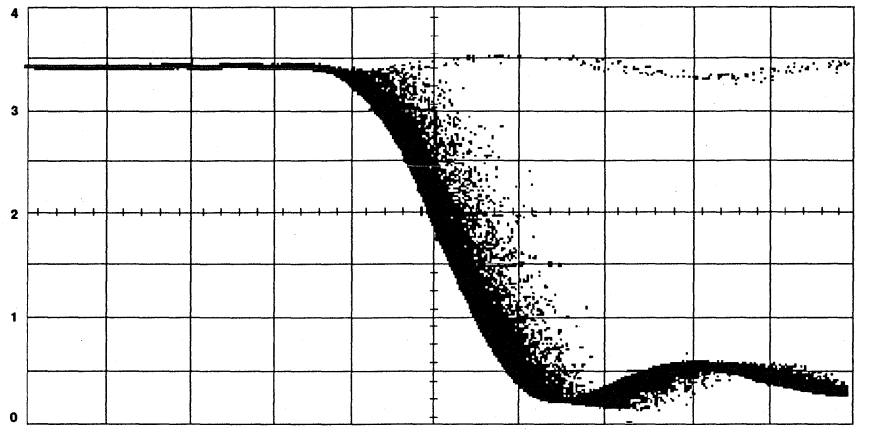


Figure 27. 74F74 $\overline{Q}$ output triggered by Q output, setup and hold times violated

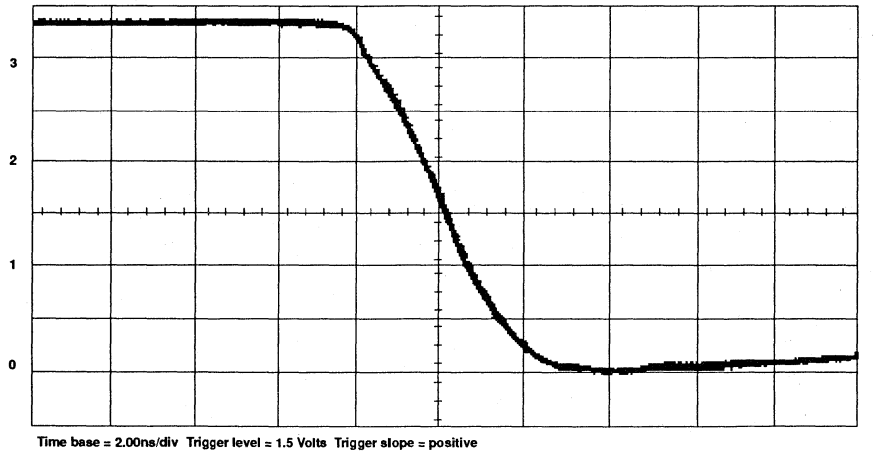


Figure 28. 74F74 $\overline{Q}$ output triggered by Q output, setup and hold times violated

MEAN TIME BETWEEN FAILURES (MTBF) VERSUS t'

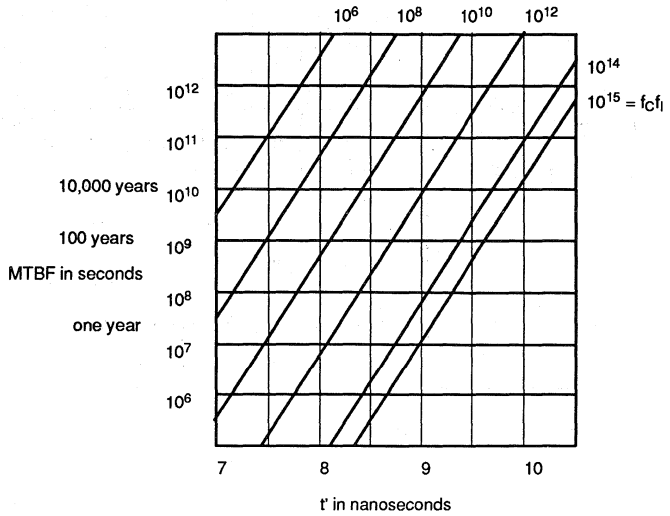


Figure 29.

NOTE: V_{CC} = 5V, T_{amb} = 25°C, τ =135ps, To = 9.8 X 10^6 sec

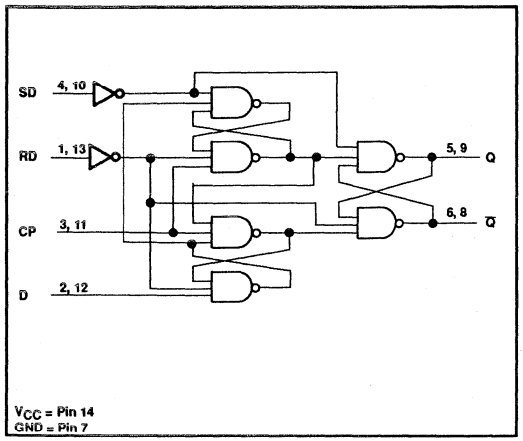
TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.5V	125ps	1.0 X 10^9 sec	138ps	5.4 X 10^6 sec	160ps	1.7 X 10^5 sec
5.0V	115ps	1.3 X 10^{10} sec	135ps	9.8 X 10^6 sec	167ps	3.9 X 10^4 sec
4.5V	115ps	3.4 X 10^{13} sec	132ps	5.1 X 10^8 sec	175ps	7.3 X 10^4 sec

Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics

74F50729

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
↑	↑	X	X	H	L	Asynchronous set
↑	↑	X	X	L	H	Asynchronous reset
↑	↑	↑	h	H	L	Load "1"
↑	↑	↑	l	L	H	Load "0"
↑	↑	↑	X	NC	NC	Hold

NOTES:
1. H = High–voltage level
2. h = High–voltage level one setup time prior to low–to–high clock transition
3. L = Low–voltage level
4. l = Low–voltage level one setup time prior to low–to–high clock transition
5. NC = No change from the previous setup
6. X = Don't care
7. ↑ = Low–to–high clock transition
8. ↑ = Not low–to–high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IH}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics

74F50729

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	V_{CC} ± 10%			–12	mA
		V_{CC} ± 5%			–15	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TY.[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
			V_{IL} = MAX,		±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Dn	V_{CC} = MAX, V_I = 0.5V					-250	µA
		CPn, SDn, RDn						–20	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX, V_O = 2.25V			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				19	27	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics

74F50729

AC ELECTRICAL CHARACTERISTICS

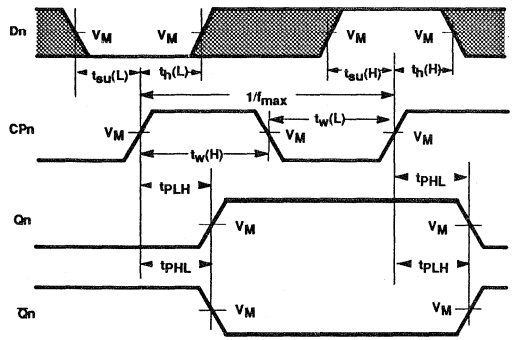
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	105	120		85		75		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	3.9 3.9	6.0 6.0	1.5 2.0	6.5 6.5	1.5 2.0	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay SDn RDn to Qn or $\overline{Q}$n	Waveform 2	2.0 3.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	1.5 2.0	7.5 8.0	ns
$t_{ok(o)}$	Output skew[1, 2]	Waveform 4			1.5		1.5		1.5	ns

NOTES:
1. $|t_{PLH}$ actual $- t_{PHL}$ actual $|$ for any one output compared to any other output where N and M are either LH or HL.
2. Skew lines are valid only under same conditions (temperature, V_{CC}, loading, etc.,).

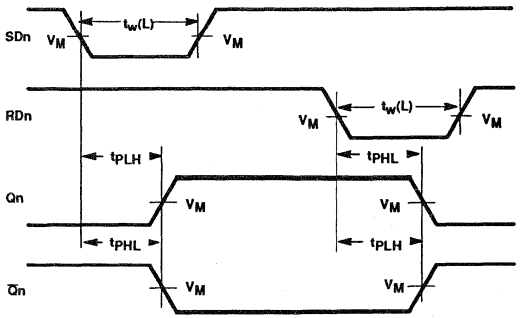
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Dn to CPn	Waveform 1	1.5 1.5			2.0 2.0		2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.5 1.5		1.5 1.5		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 2	3.0 4.0			3.5 6.0		3.5 6.0		ns
t_w (L)	SDn, RDn pulse width, low	Waveform 3	3.5			4.0		4.0		ns
t_{rec}	Recovery time SDn, RDn to CPn	Waveform 3	6.0			6.5		6.5		ns
t_{rec}	Recovery time SDn to RDn or RDn to SDn	Waveform 3	6.0			1.0		1.0		ns

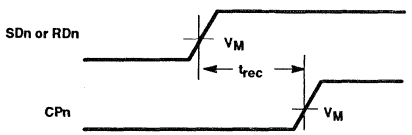
AC WAVEFORMS



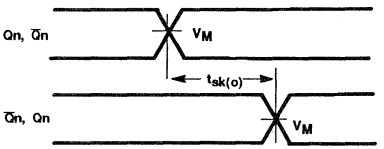
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width



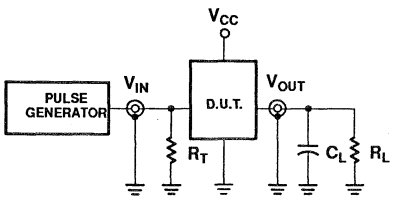
Waveform 3. Recovery time for set or reset to output



Waveform 4. Output skew

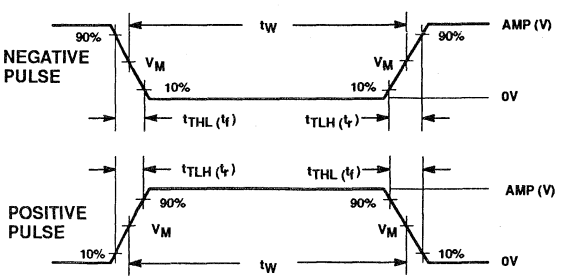
NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Section 7
Surface Mounted ICs

FAST TTL Logic Series

Surface Mounted ICs

SECTION 7

INTRODUCTION

Economic survival is driving the electronics industry to use cheaper, faster, more reliable and more dense systems and components. Assembly technologies, such as SMD (Surface Mounted Device) technology, developed and used in hybrids and for military electronics for over two decades, is being adapted to commercial electronics as part of this evolution. With SMD technology, components are soldered directly to metalized footprint on the surface of the board or substrate rather than being inserted through holes drilled in the board and then soldered. Because of this evolution, package styles specially designed to facilitate surface mounting are now in high demand.

The reasons for the change to SMD technology vary from one customer to another; but the primary motivator is higher profits through lower manufacturing and material costs, or an improved product, or both.

Improved Electrical Performance

Because SMD packages are much smaller than their DIP counterparts, they have much less capacitance and inductance, and provide improved AC performance, especially in high-speed environments. They help to minimize problems associated with ground bounce and multiple output switching found with standard DIP packages. The SO package is especially suitable for high-speed families such as FAST and High-Speed CMOS where package inductance can induce or compound problems not normally found in slower technologies.

Ease of Automation

SMD pick-and-place machines offer higher yields, faster cycle rates (3–10 times faster), and much higher throughput volumes than automatic insertion machines for DIP packages.

Greatly Increased Densities

Greatly increased densities can be achieved through surface mounting. The packages themselves are much smaller (as much as 70%) and can be placed much closer together. Furthermore, both sides of the board can be used with SMDs.

Reduced Board Costs

The number of layers, total size of the board, and the number of plated through holes can be reduced, thus lowering the total cost of the board (many companies claim savings of 30 to 50%).

Easier Board Rework

In those instances where rework is necessary, it is much faster and cheaper with SMDs.

Improved Reliability

Not only are the components proving to be at least as reliable as their DIP counterparts but, surface mounted assemblies show fewer failures in stress tests than equivalent through hole assemblies.

Lower Shipping, Storage and Handling Costs

SMD components are up to 70% smaller and weigh up to 90% less than DIPs (up to 95% savings in storage area for Tape & Reel SMD components versus DIPs and up to 90% savings in component weight). Surface mount assemblies offer additional savings in both weight and space, both of which can be linked to increased profits.

SO PACKAGE

The SO package was developed by N.V. Philips Corporation, originally for the Swiss watch industry. In the mid-1970's Signetics introduced linear ICs in SO packages to the US market (hybrid and telecommunications). As demand grew, other technologies such as FAST, Low Power Schottky, Schottky, TTL, CMOS, High-speed CMOS (HC and HCT), ECL, ROMs, RAMS, and PROMs, were made available in SO packages.

The SO is a dual-in-line plastic package with leads spaced 0.050" apart and bent down and out in a Gull-Wing format. It comes in two widths: 0.150" SO, and 0.300" SOL (SO-Large) depending on the pin count.

As ICs became more complex and the number of pins grew, the standard dual-in-line packages grew longer and wider, presenting new electrical and mechanical problems. Some of these were resolved with the introduction of the ceramic leadless chip carrier (LCC). These were square, ceramic packages without leads which can be socketed or soldered directly to a substrate if the thermal coefficient of expansion of the chip carrier and the substrate are to be matched.

In 1980, the Plastic Leaded Chip Carrier (PLCC) was introduced as a cheaper alternative to the LCC. However, this was at the same time that SMD was winning acceptance in commercial electronics and the PLCC was seen as an ideal SMD package for the higher pin count devices (those with more than 28 leads). The PLCC is a square, plastic package with leads on four sides, spaced down and under in a J-Bend configuration. It is available in the higher pin counts: 20, 28, 44, 52, 68, and 84, with even higher pin counts under development.

The smallest square PLCC is the 20-Pin package. There are many reasons for this; the primary one is that below 20 pins, the package would be as thick as it is square, resulting in a cube-like package which would be very difficult to handle in an automated environment.

Logic and linear devices are available in SO while the more complex parts such as microprocessors, microcontrollers, complex peripherals,, large memory devices,, and other higher pin count integrated circuits will be found in the PLCC.

ASSEMBLY

The assembly of these SMD packages is virtually the same as for the older DIP packages using the same materials and most of the same equipment and assembly technologies.

The only differences in the process are the smaller lead frames, different lead bends (gull-wing for SO and J-bend for PLCC), and closer spacing resulting in a much smaller package for the same basic die.

Table 1.

PIN COUNT	SO	SOL	PLCC
8	X		
14	X		
16	X	X	
18		X	X (rectangular)
20		X	X
24		X	
28		X	X
44			X
52			X
68			X
84			X

RELIABILITY

Reliability studies of SMD components, conducted not only by Signetics and Philips, but by many of our competitors and customers, have revealed that these packages are at least as reliable as the standard plastic DIP packages that have been used over the past 20 years. In several cases, test results of the SMD packages have been better than their DIP counterparts.

STANDARDIZATION

The SO package is an industry standard format. In June 1985, the JEDEC (Joint Electronics Design Engineering Council) of the EIA (Electronics Industries Association) issued a Solid State Product Outlines Standard for each of the SO formats: MS-012 AA-AC for the 0.150" body width SO and MS-013 AA-AE for the 0.300" body width SOL. In addition to the JEDEC standard, de facto standardization has been achieved in the industry in that most of the major US and European IC manufacturers (more than 15 companies currently) use this standard.

The PLCC is also a standardized format, with a JEDEC Registered Outline #MO-047 AA-AH. It also is multiple-sourced with over 10 US IC manufacturers using this standard.

Points worth noting: All SO and SOL packages have 0.50" lead spacing and a gull-wing lead bend, while all PLCC packages have the same lead spacing and a J-bend lead bend.

TAPE AND REEL

One revolutionary phenomenon in SMD is the development of Tape and Reel for the IC packages. Philips and several other companies making automatic placement equipment recognized the need for a feed system which allows for positive indexing large volumes of components at high-speed in order to get maximum efficiency out of the new pick-and-place machines. Tubes are limited to a relatively small number of parts (dictated by tube length) and depend on gravity to feed components to the placement head. After several proposed tape formats, Philips, Signetics, many of the component and placement equipment manufacturers, and board manufacturers convened under the auspices of EIA (Electronics Industries Association) and agreed on an industry standard specification for Tape and Reel for both SO and PLCC packages. The proposed EIA specification RS 481A is being used by Signetics and Philips, both of whom have shipped components on Tape and Reel since late 1984.

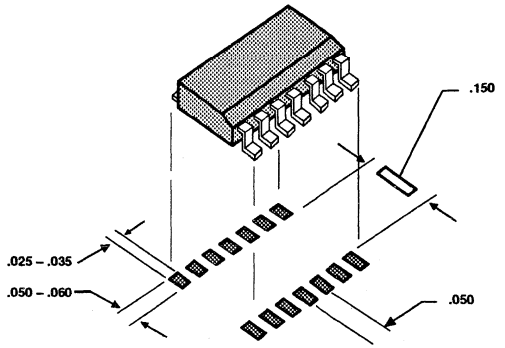
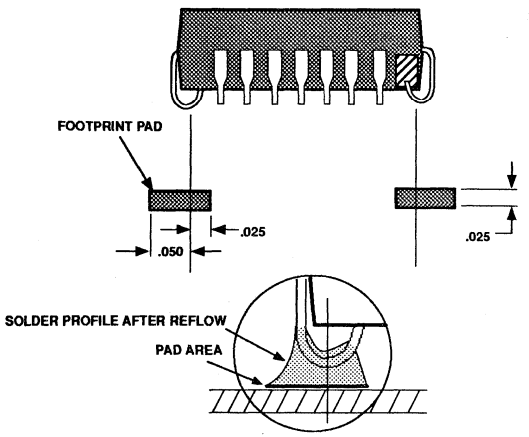
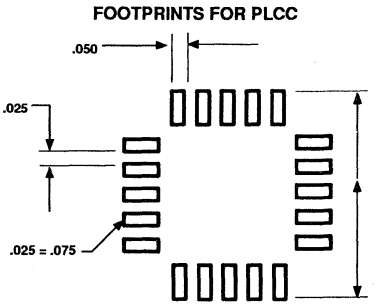


Figure 1. Manufacturer's Recommended Footprint





PINS	A
20	.425
28	.525
44	.725
52	.825
68	1.025

Figure 2. Footprint Design for the PLCC IC

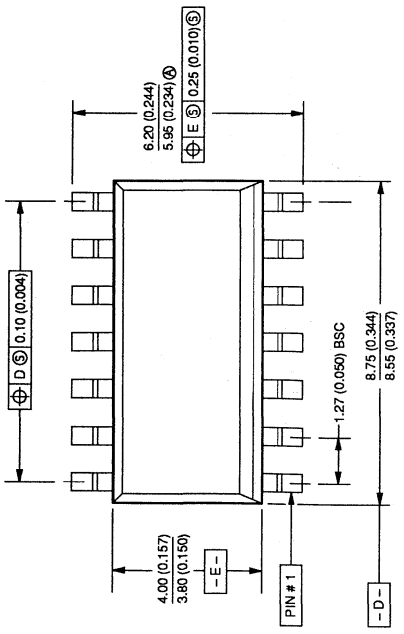
Section 8
Package Outlines

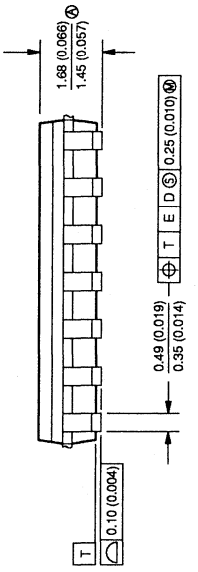
FAST TTL Logic Series

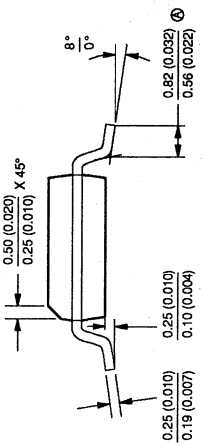
CONTENTS

Package Outlines

14-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE







NOTES

1. Package dimensions conform to JEDEC Specification MS-012-AB for standard Small Outline (SO) package, 14 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

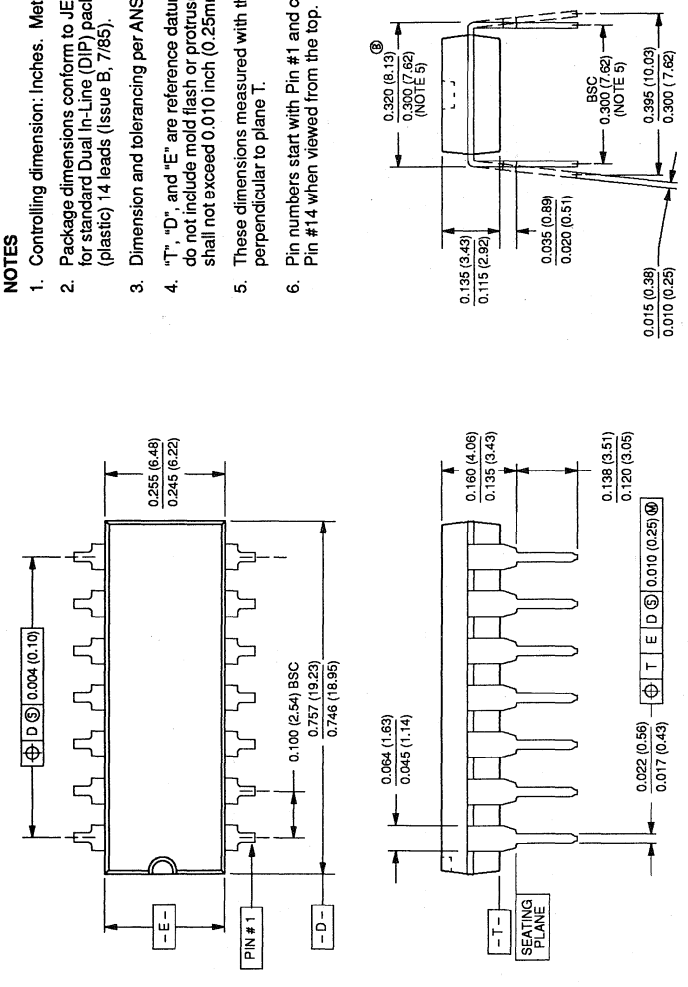
853–0175D 04697

DH1

14-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

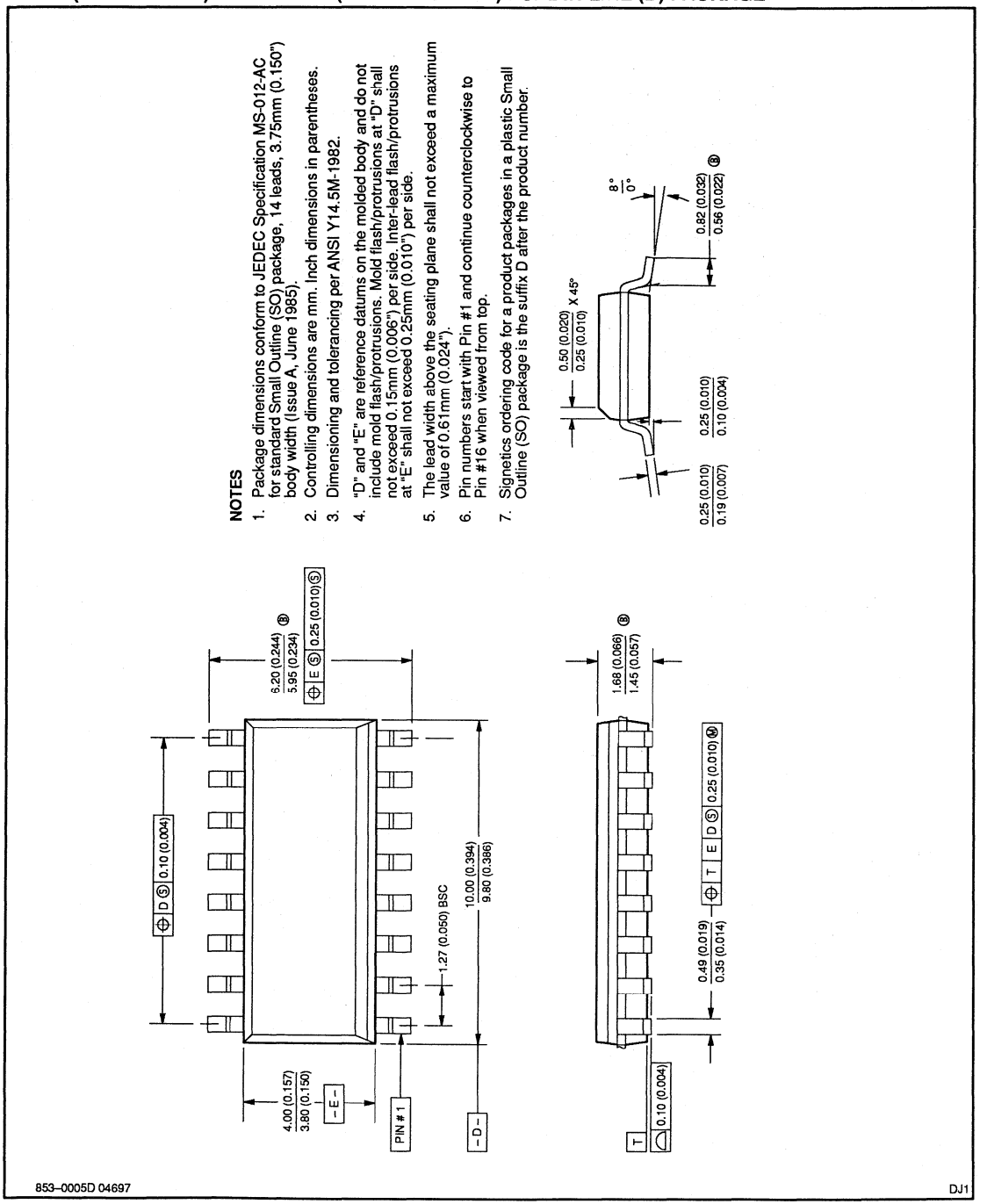
NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AC for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 14 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.

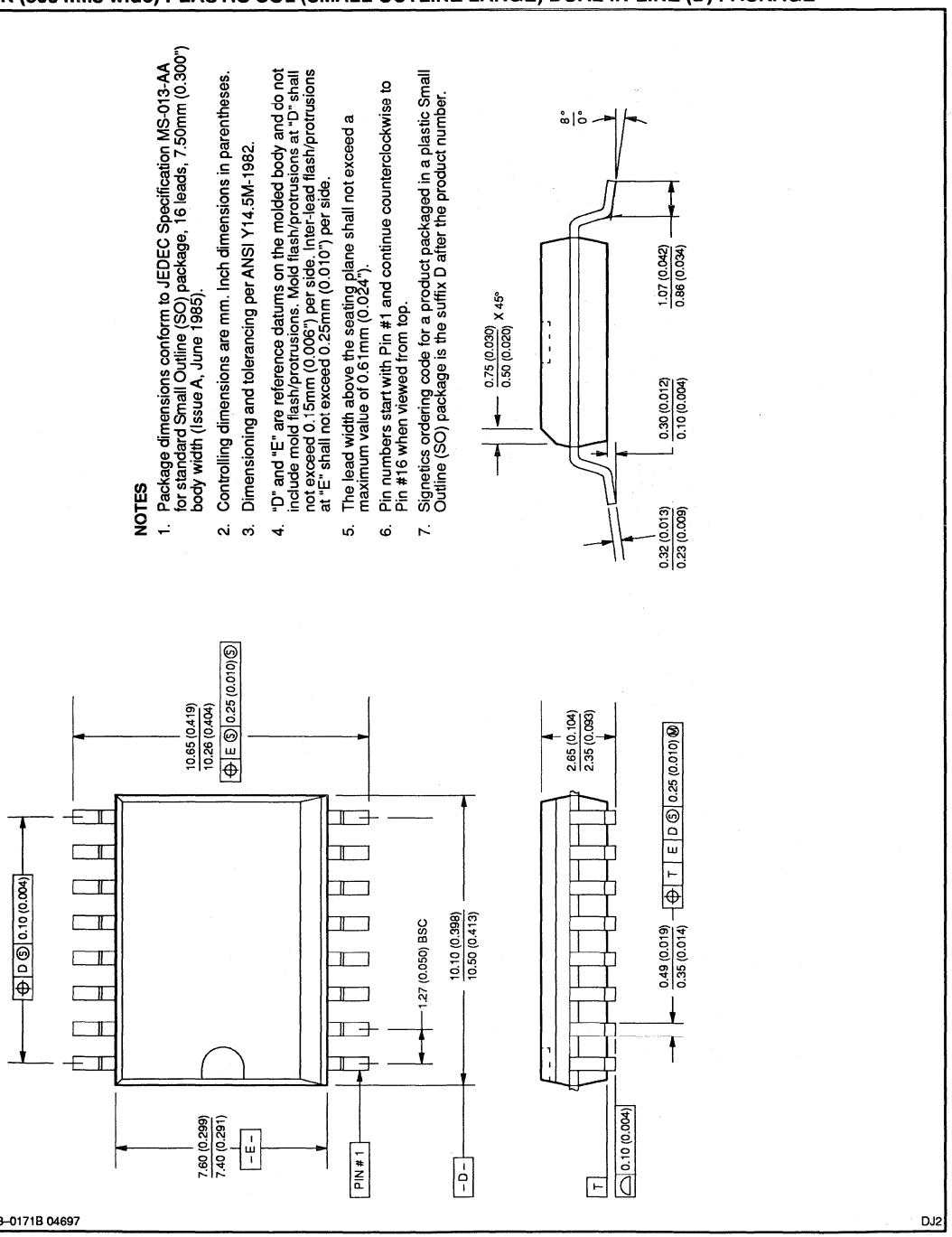


853-0405B 02880 NH1

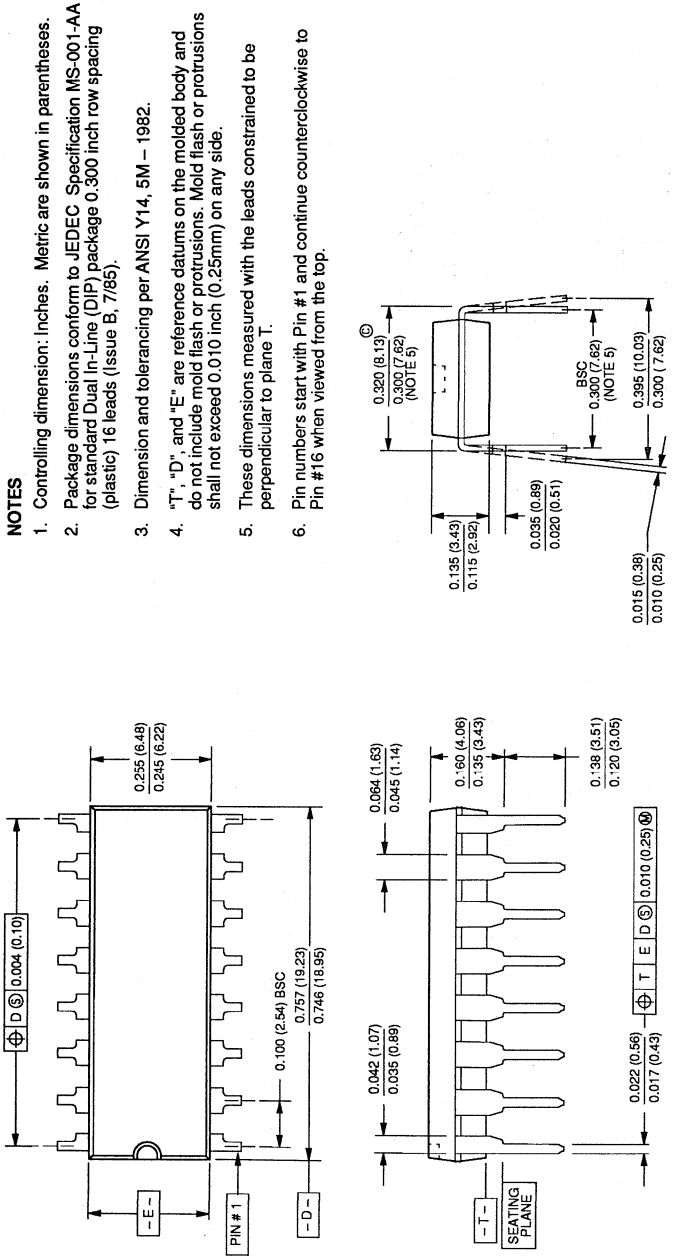
16-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



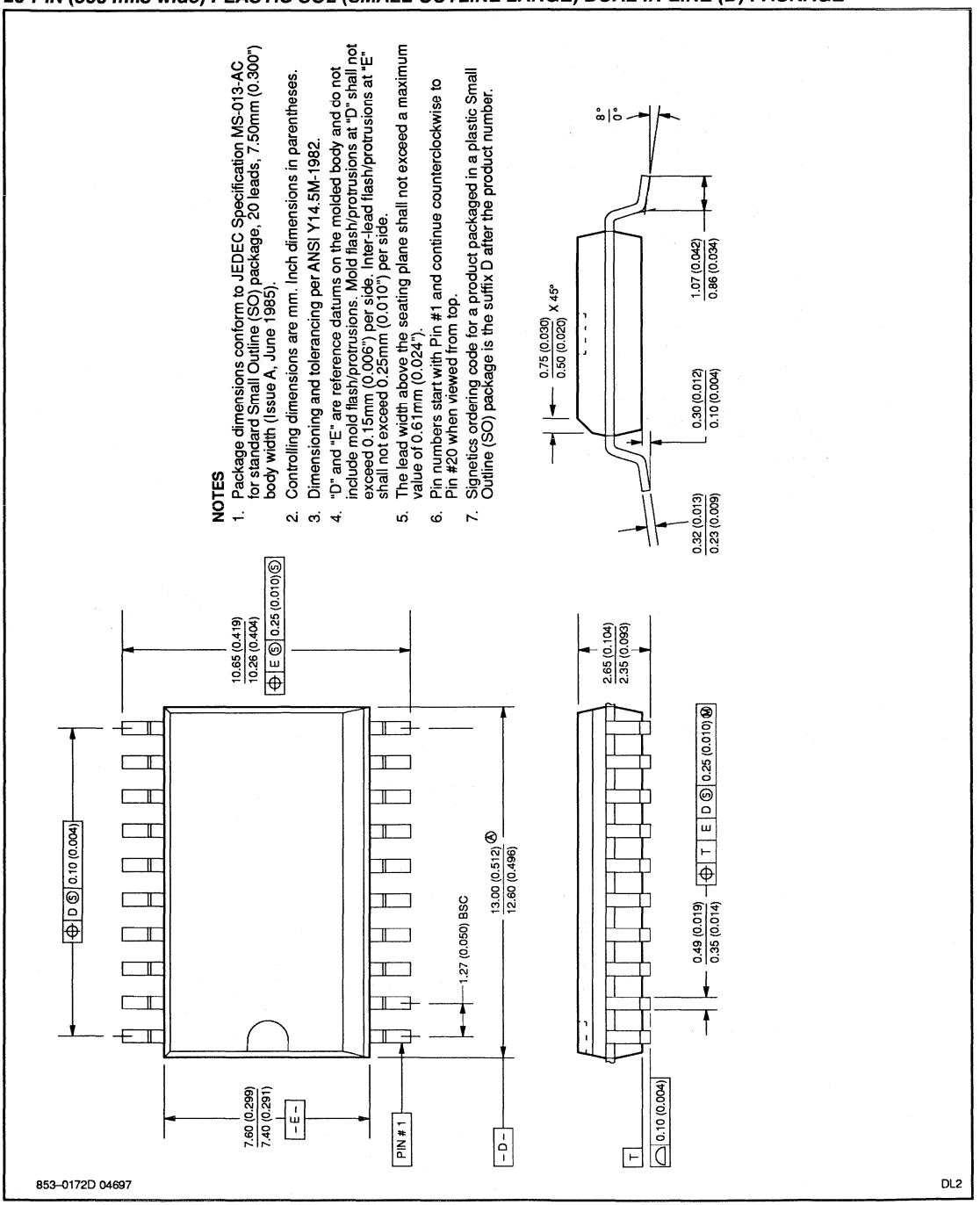
16-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



16-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



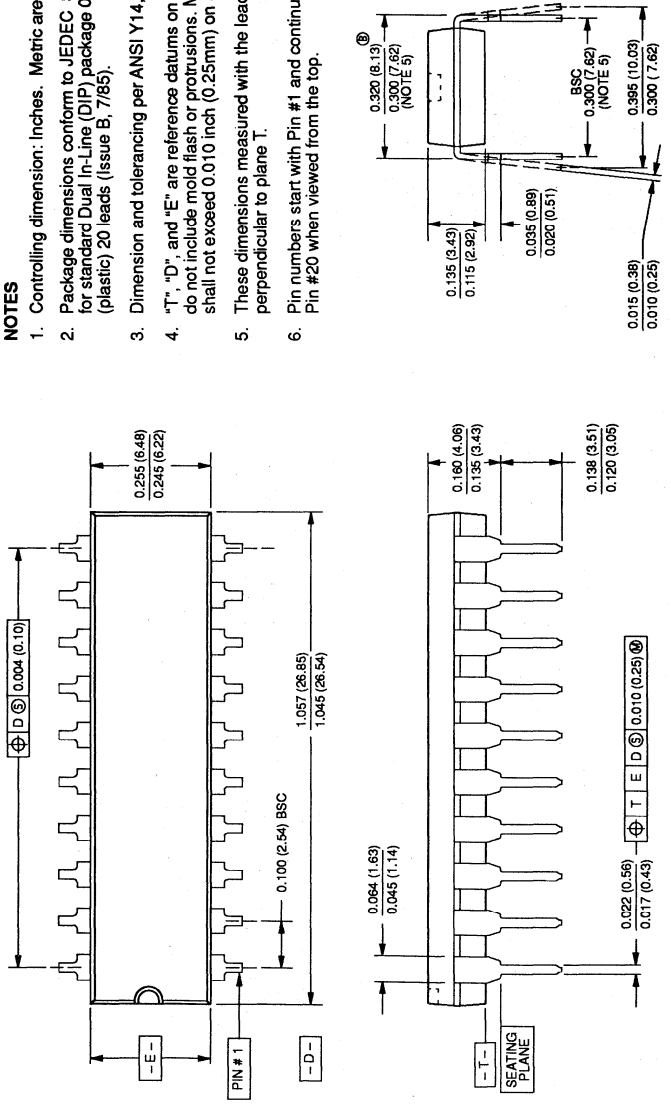
20-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



20-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

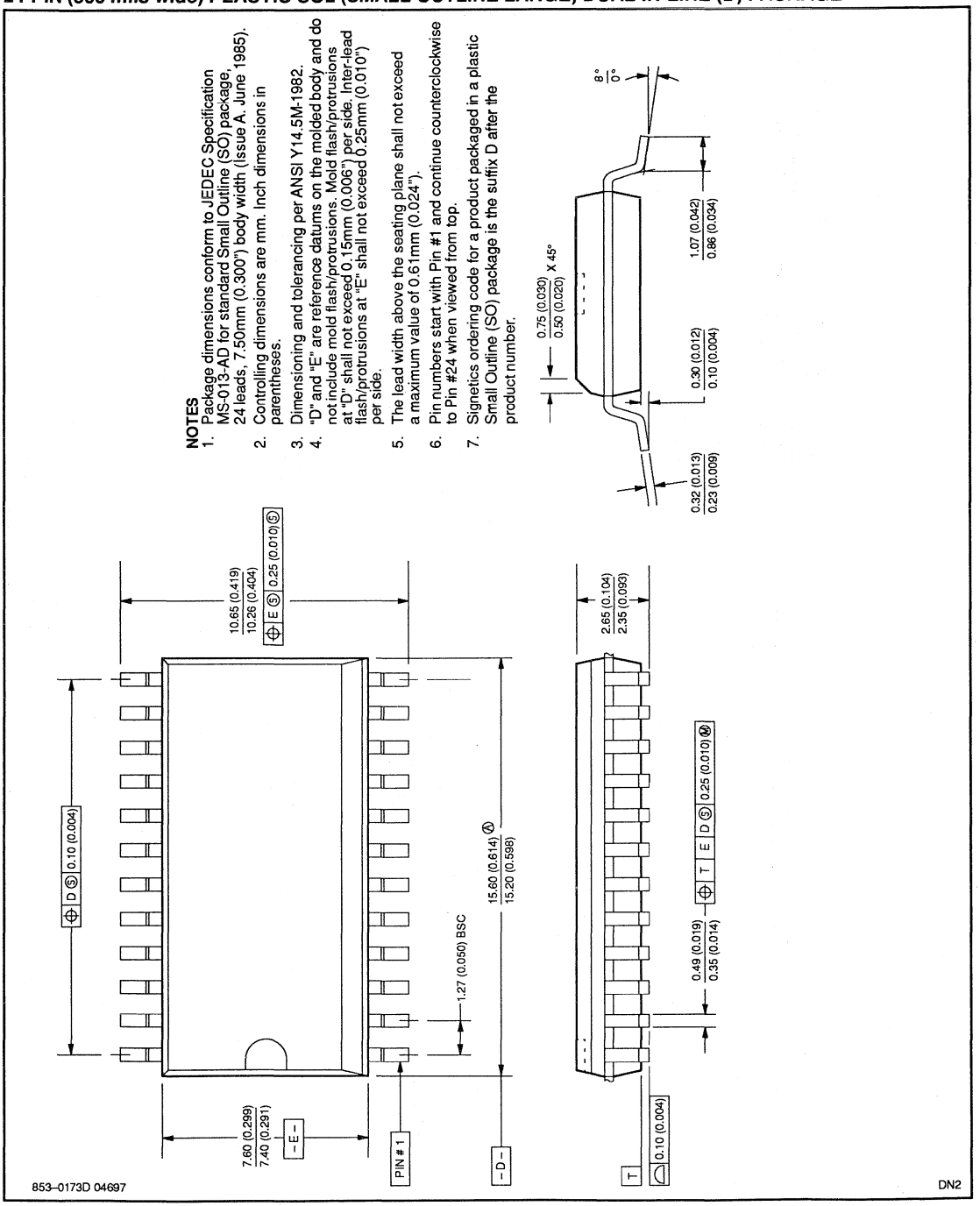
NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AE for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 20 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #20 when viewed from the top.

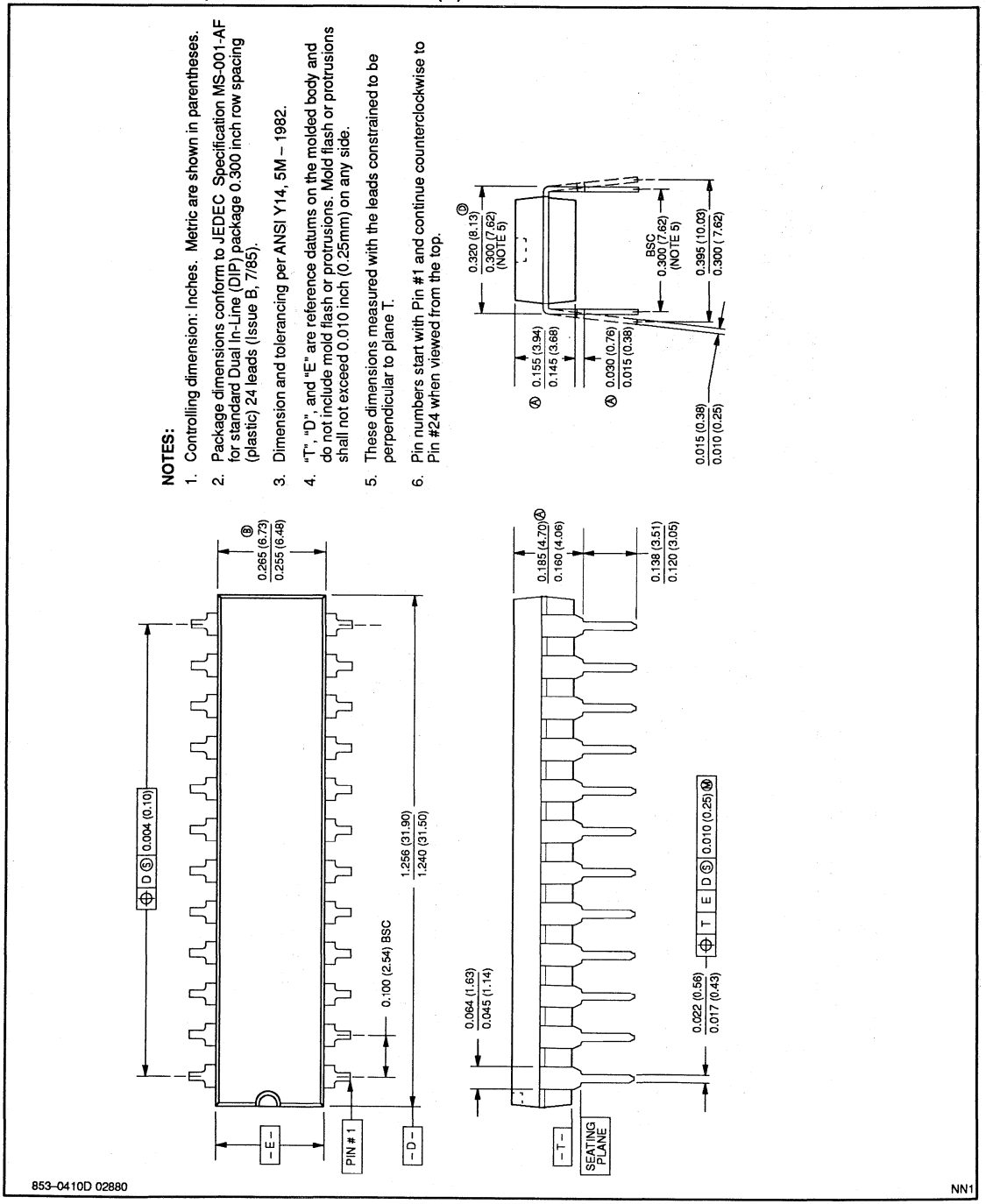


853-0408B 02880 NL1

24-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



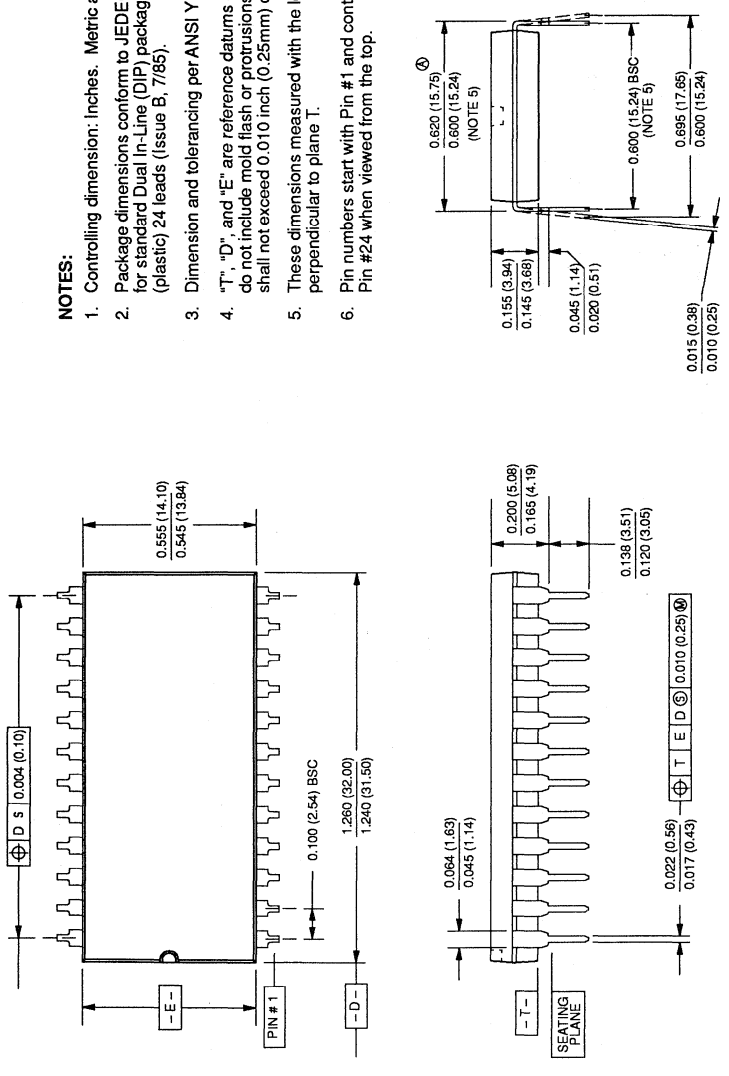
24-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



24-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

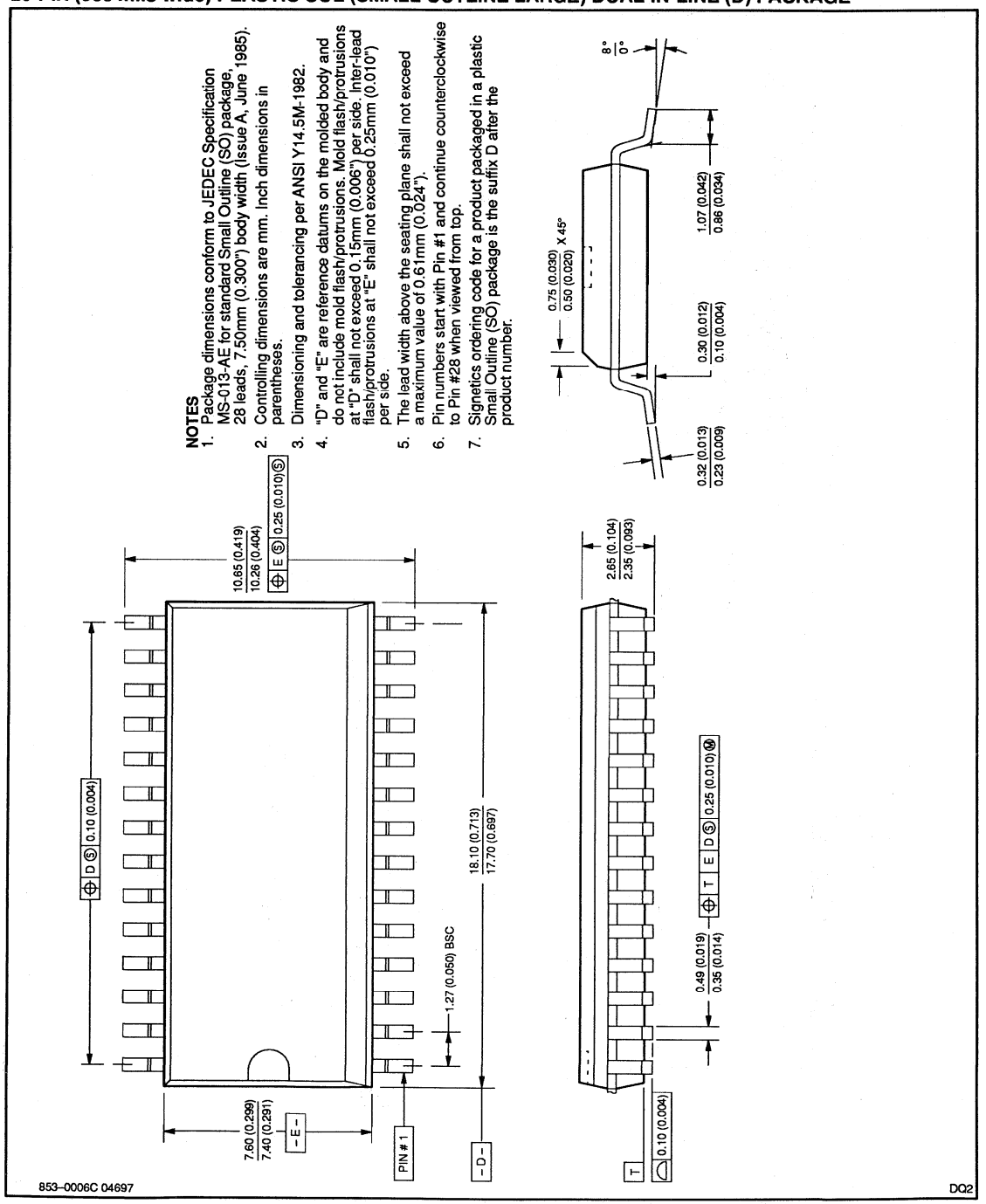
NOTES:

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-011-AA for standard Dual In-Line (DIP) package 0.600 inch row spacing (plastic) 24 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #24 when viewed from the top.



853–0412A 02880 NN3

28-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



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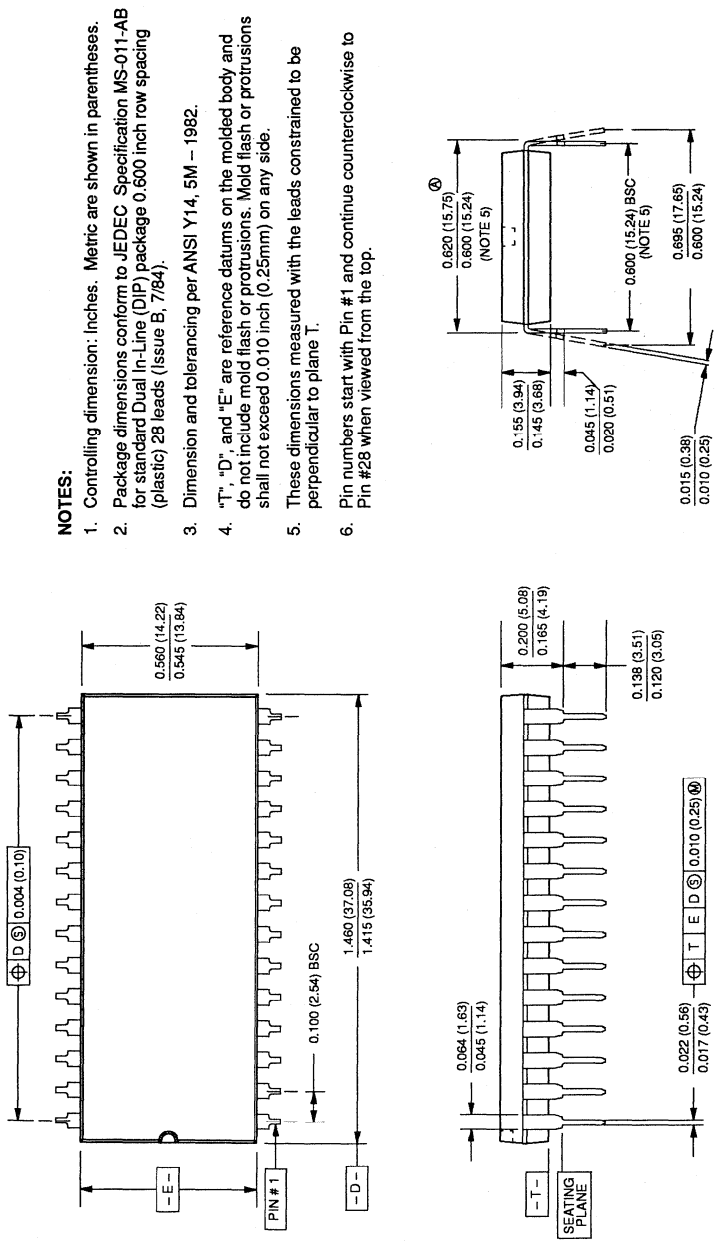
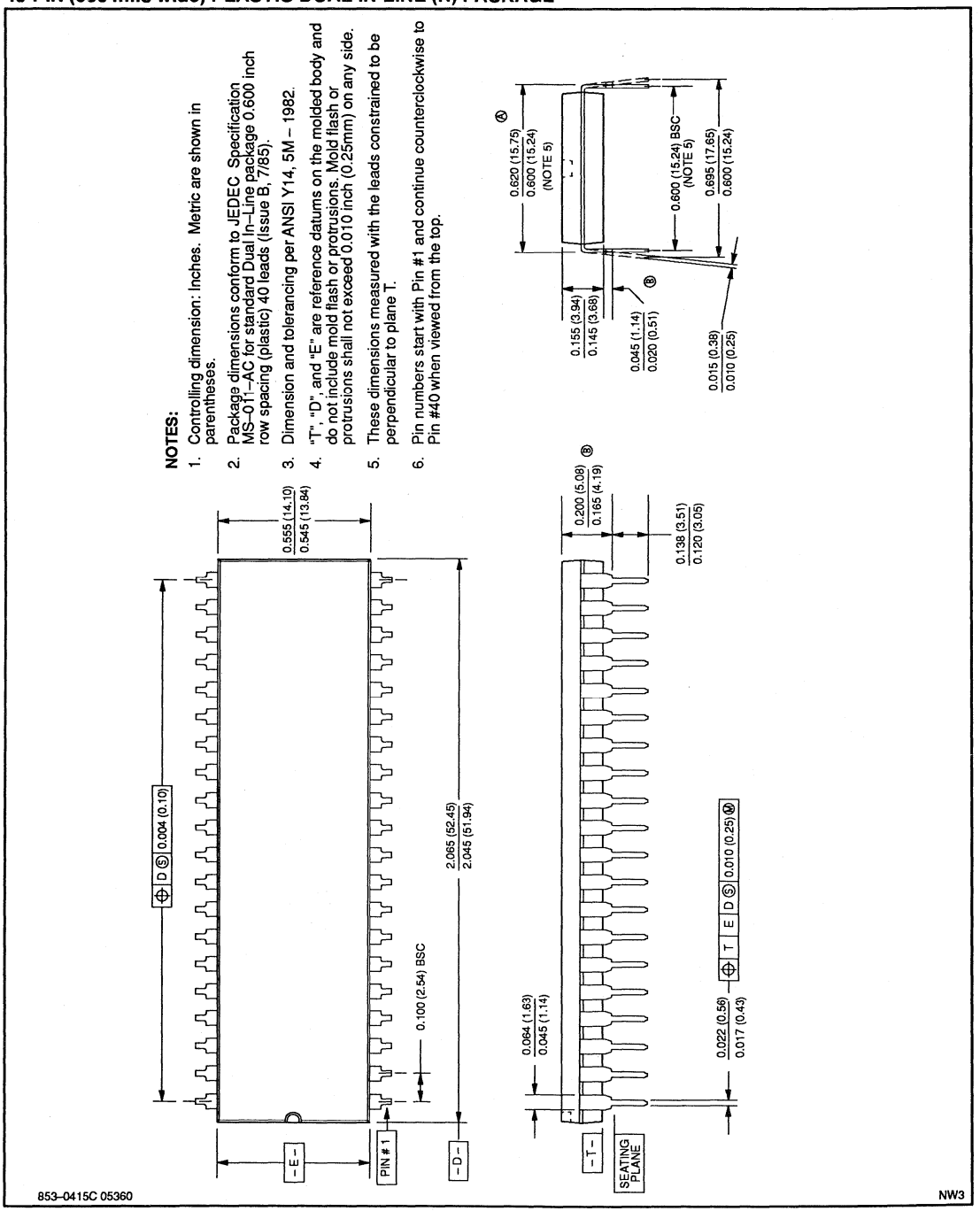
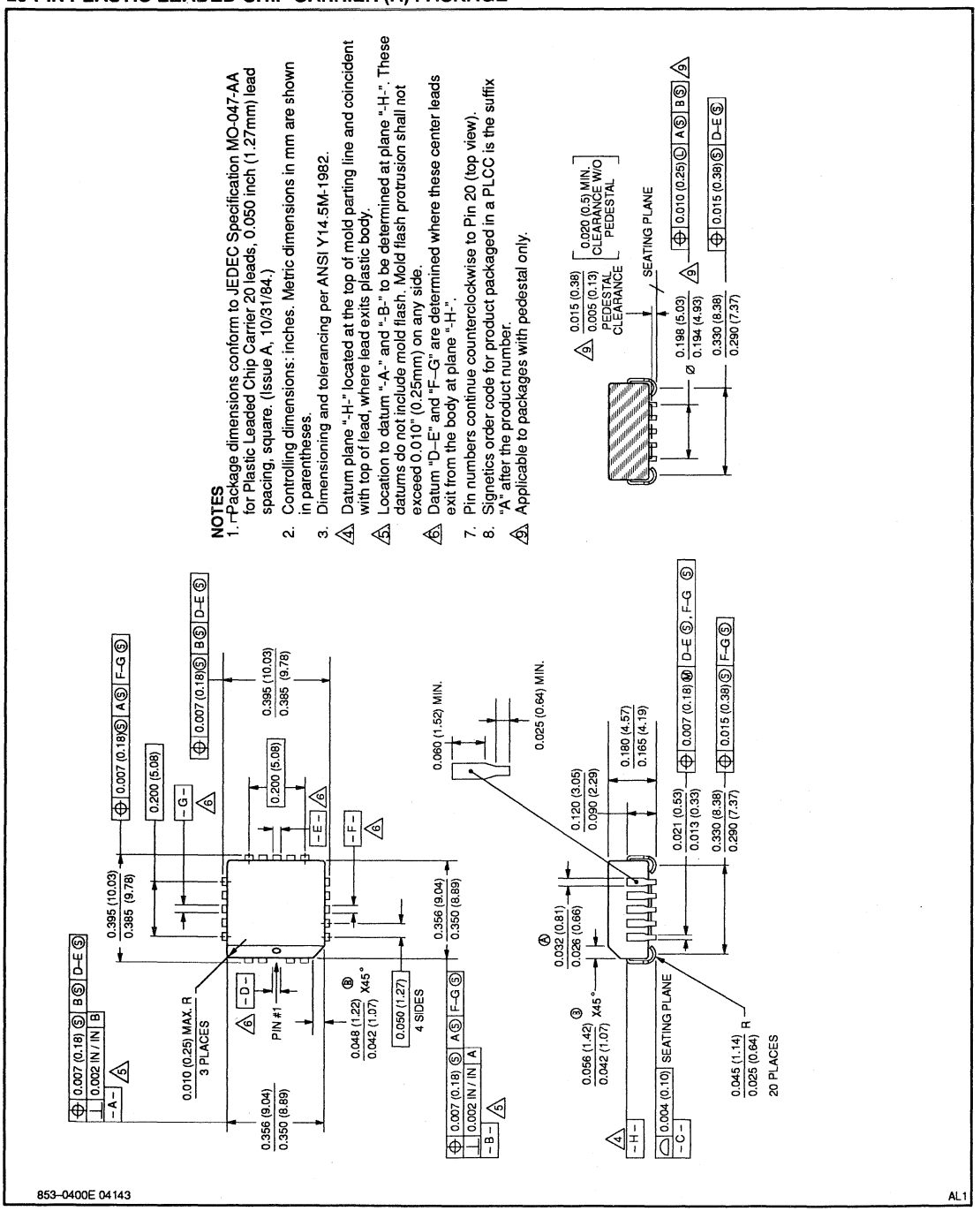


40-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



20-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



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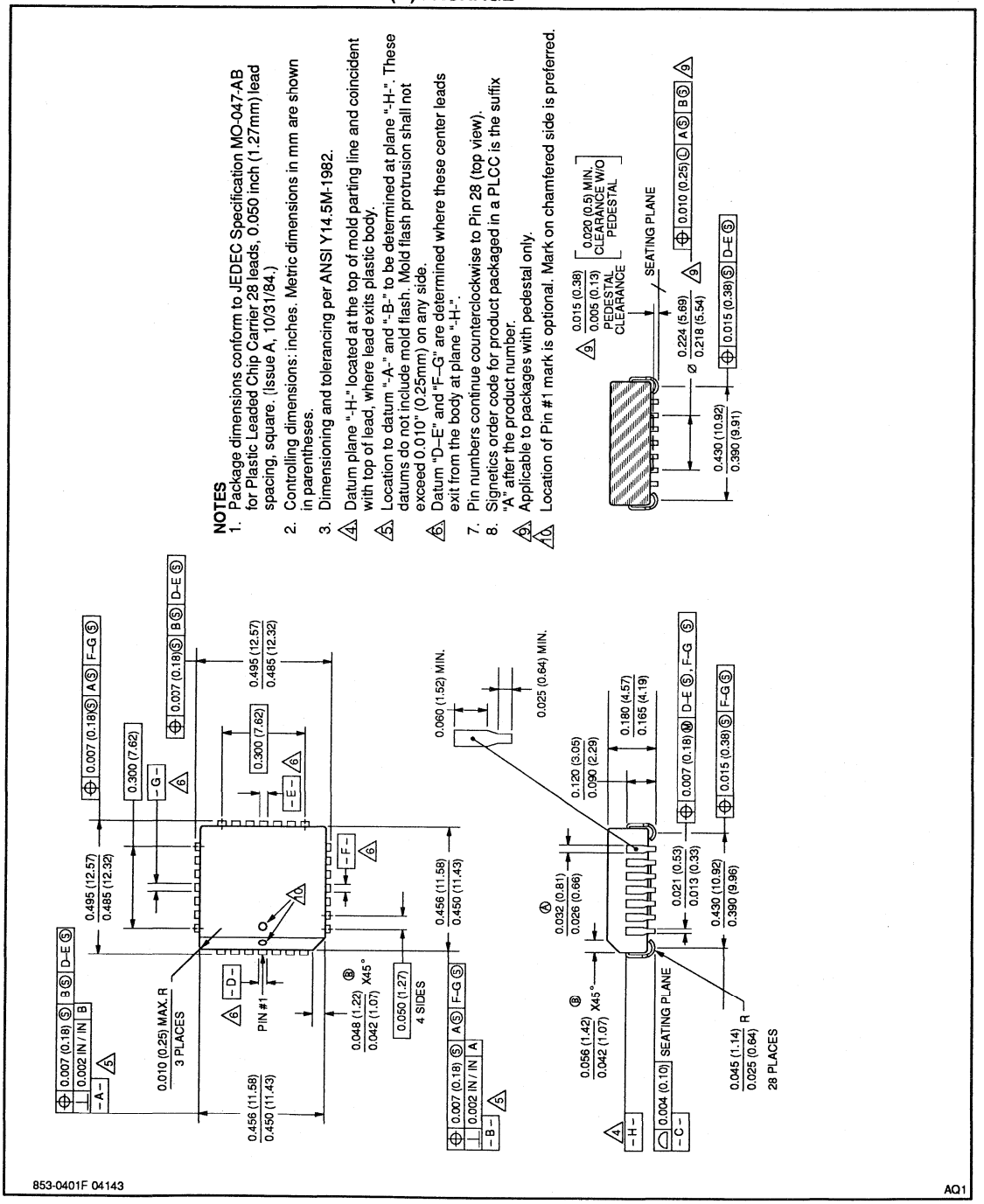
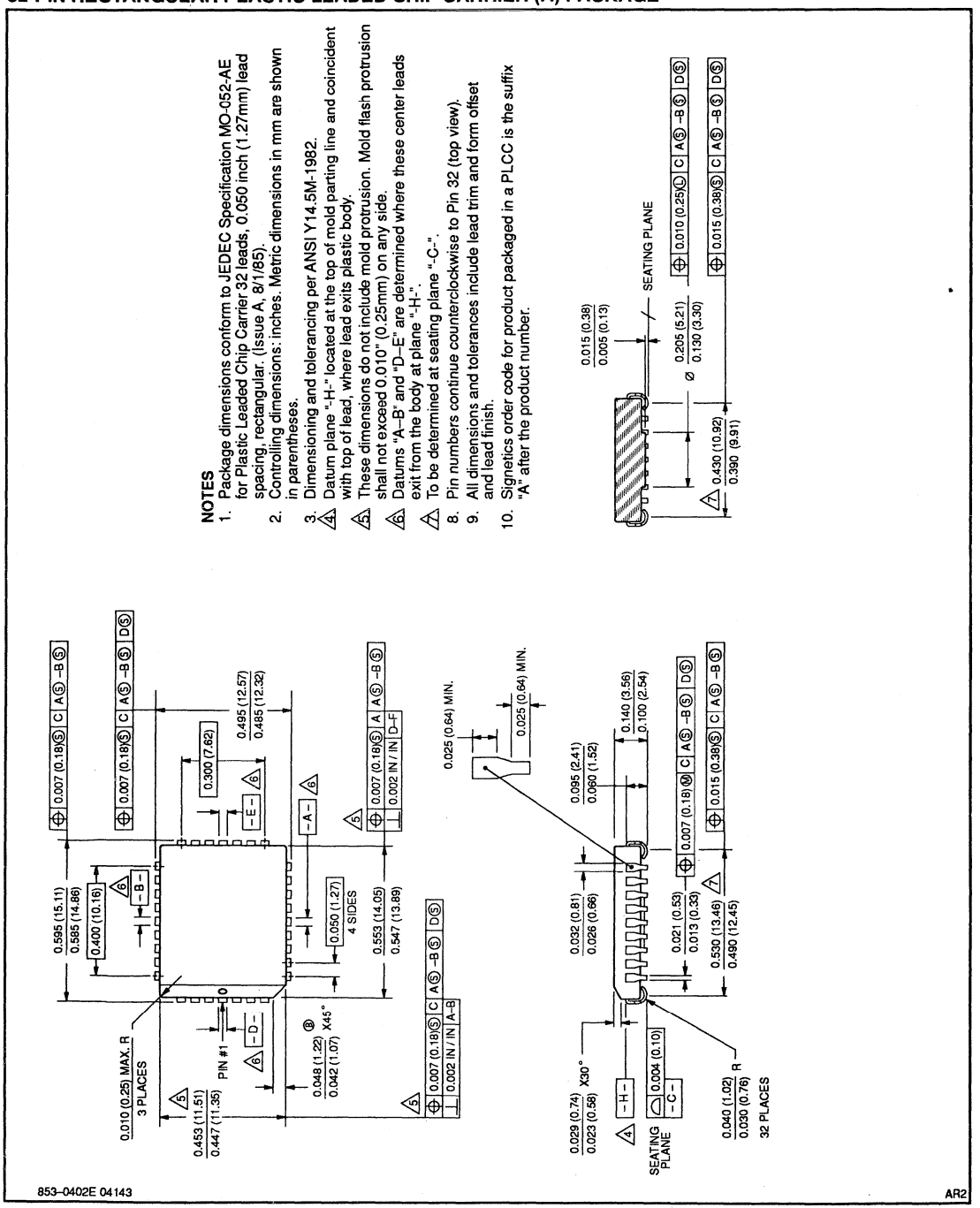


32-PIN RECTANGULAR PLASTIC LEADED CHIP CARRIER (A) PACKAGE



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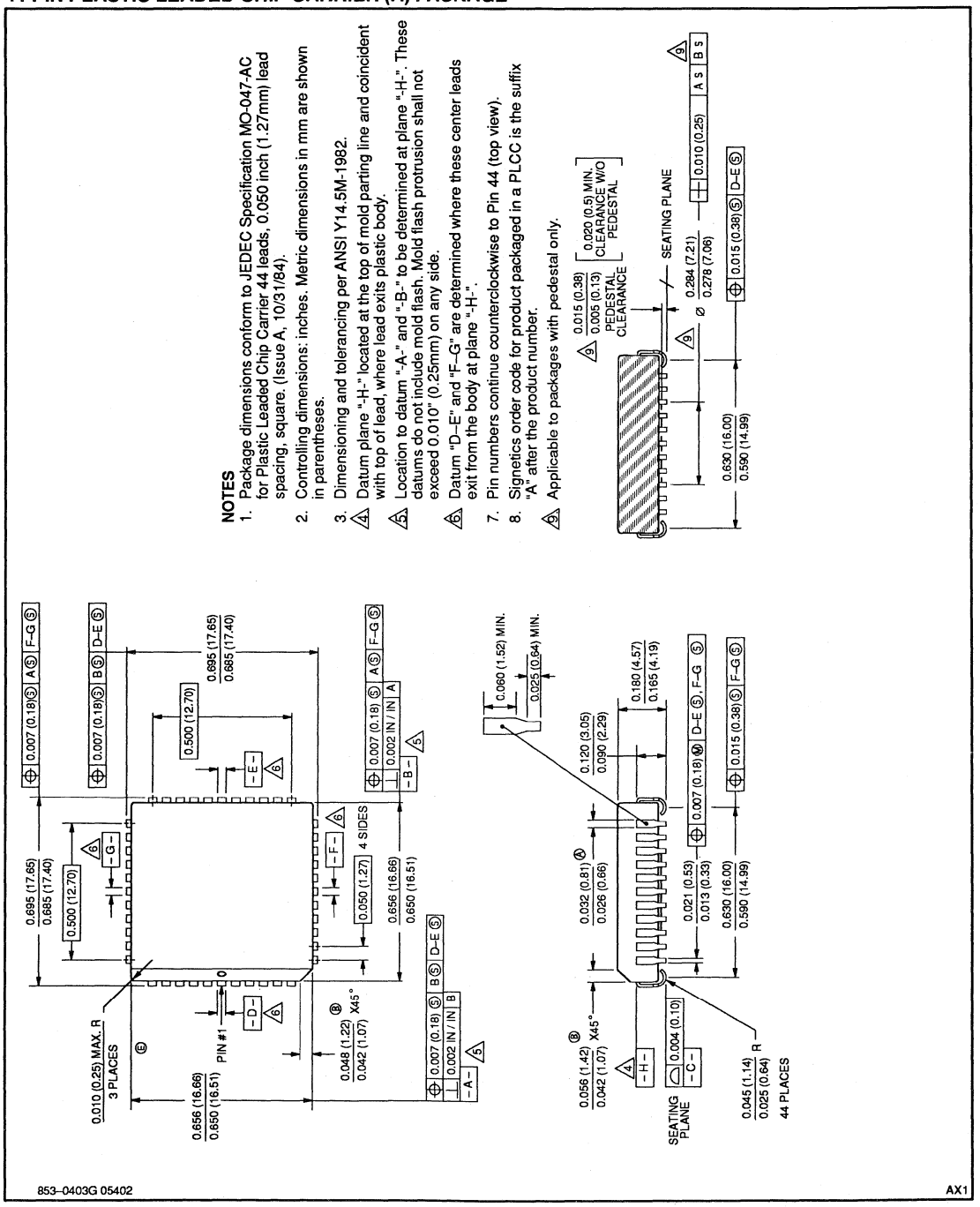

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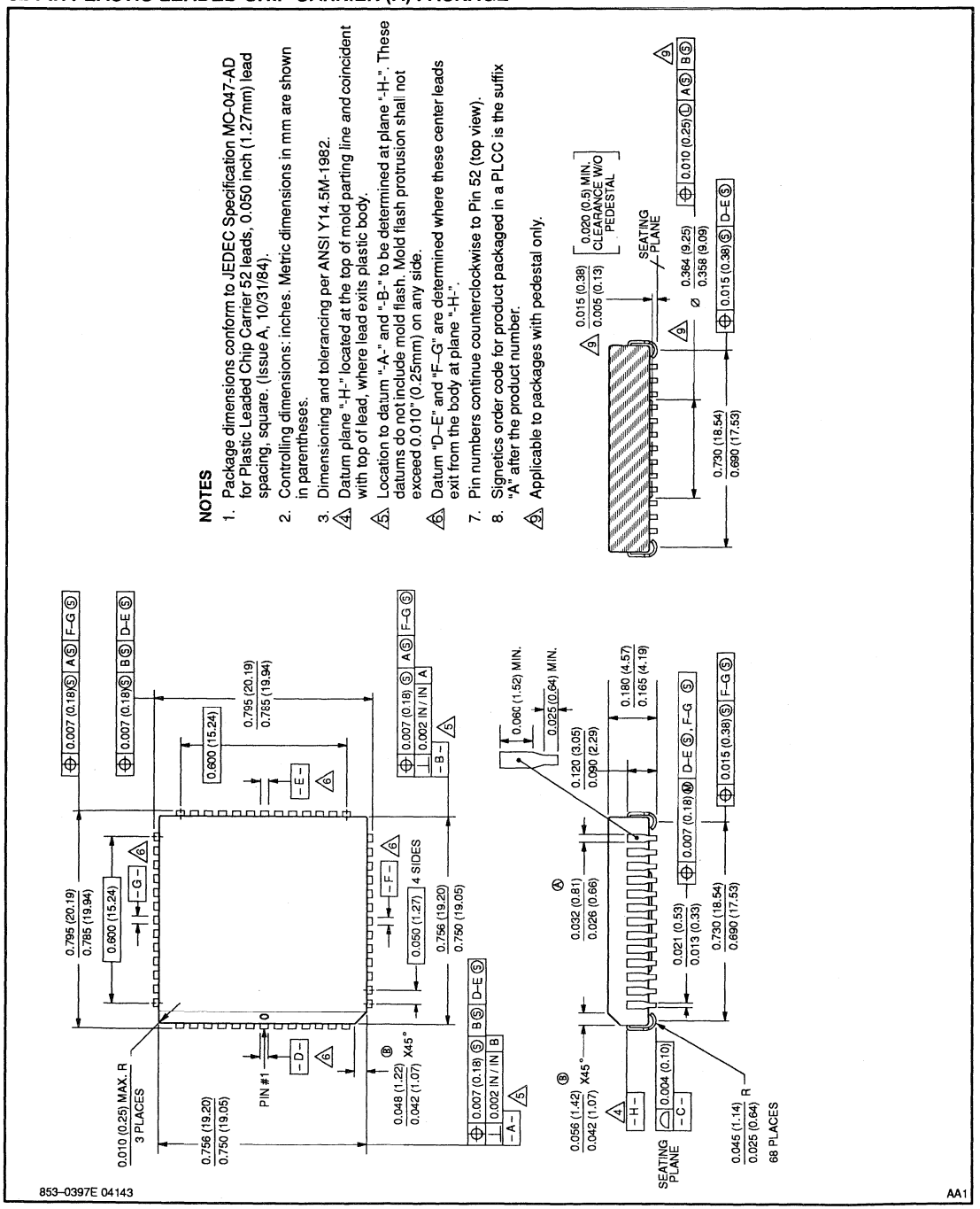

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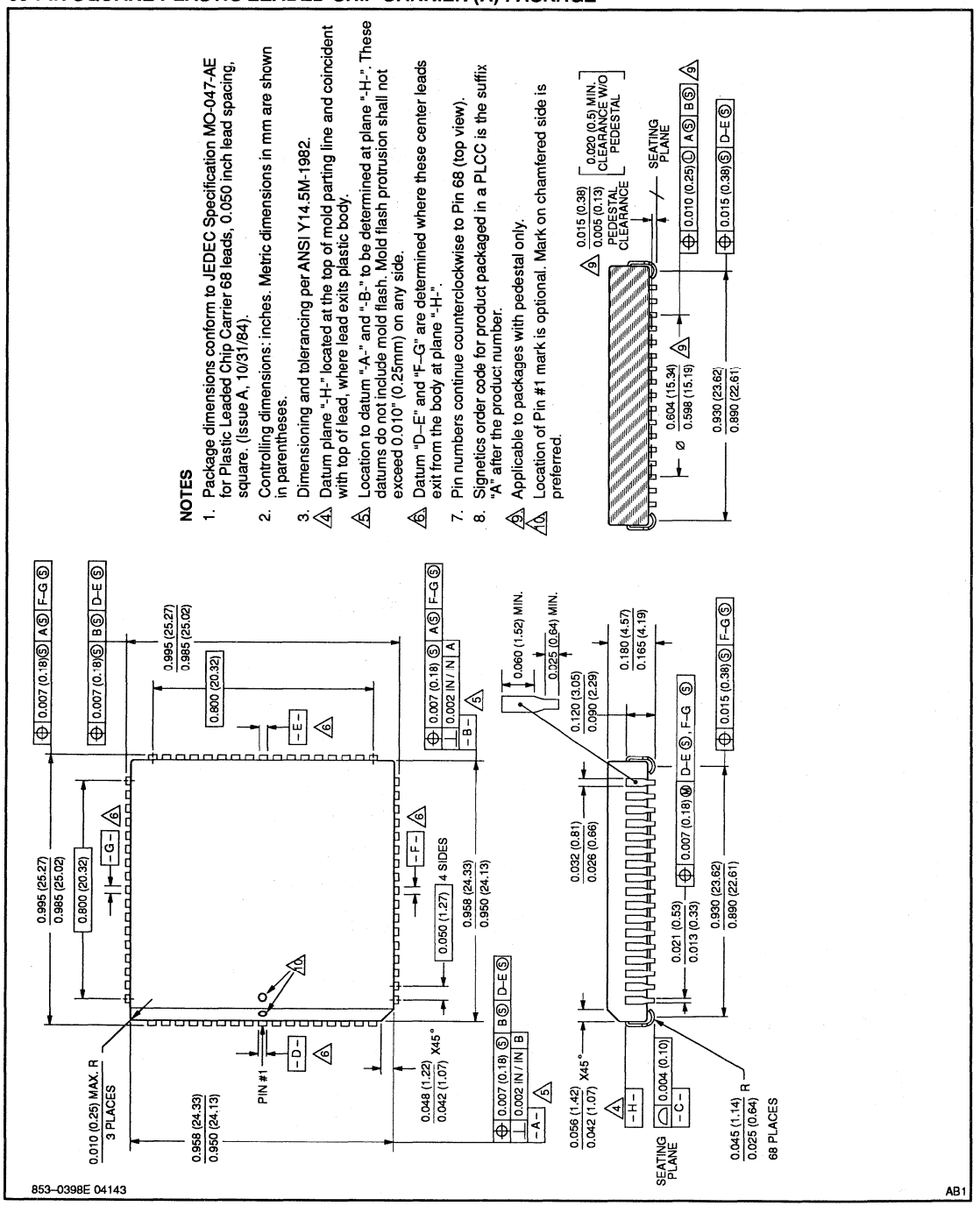

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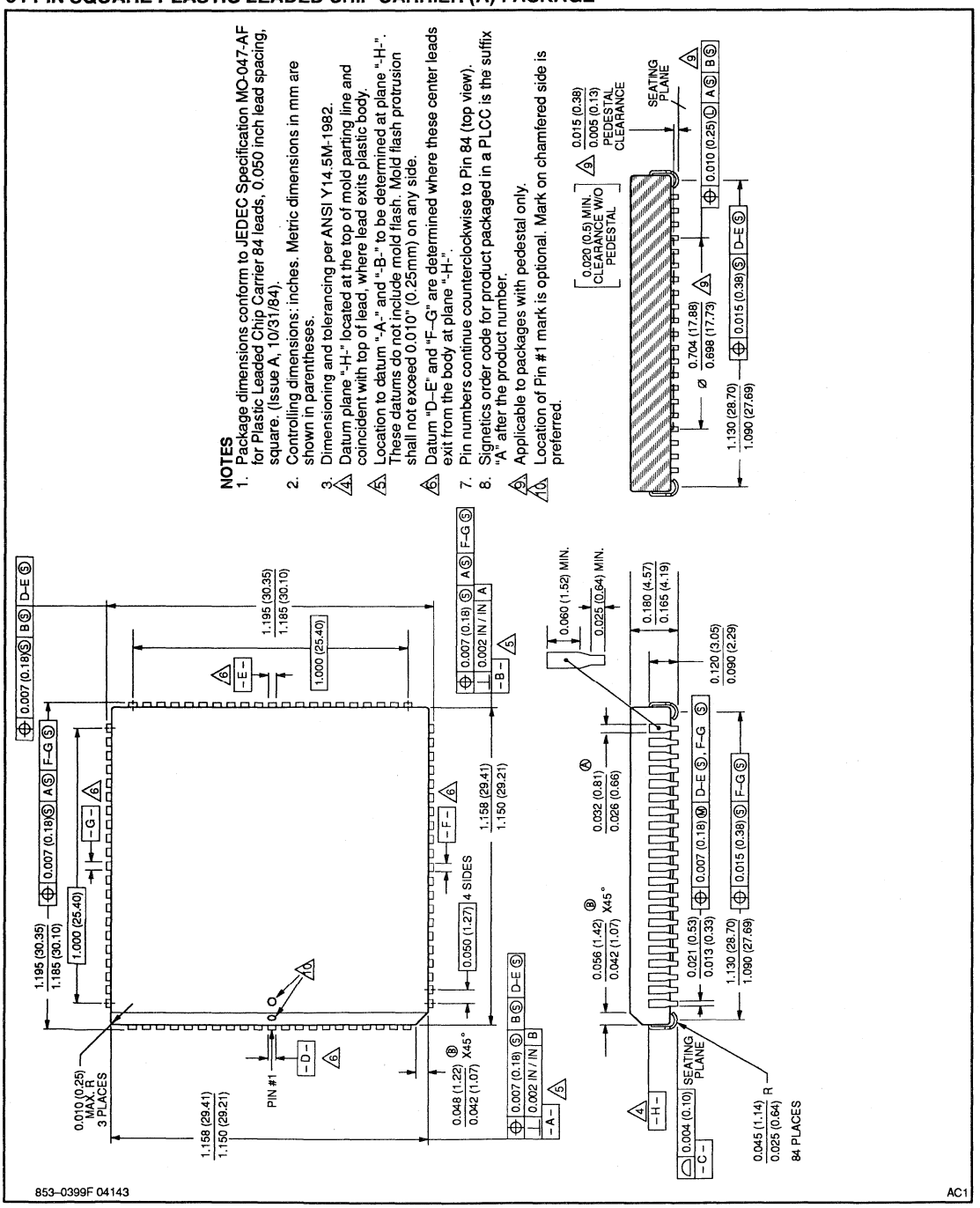

Section 9
Sales Offices, Representatives and Distributors

Sales Offices, Representatives and Distributors — SECTION 9

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Westford
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Novi
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Data handbook system

APPENDIX A

INTRODUCTION

Philips Semiconductors' data handbook system is comprised of 37 books. The handbooks are classified into two series:

INTEGRATED CIRCUITS and
DISCRETE SEMICONDUCTORS.

Data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

For more information about data handbooks, catalogs and subscriptions, contact one of the organizations listed on the back cover of this handbook. Product specialists are at your service and inquiries are answered promptly.

INTEGRATED CIRCUITS

IC01a	Semiconductors for Radio and Audio Systems
IC01b	Semiconductors for Radio and Audio Systems
IC02a	Semiconductors for Television and Video Systems
IC02b	Semiconductors for Television and Video Systems
IC02c	Semiconductors for Television and Video Systems
IC03a	Semiconductors for Telecom Systems
IC03b	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS Logic Family
IC08	ECL 100K Logic Families
IC10	Memories
IC11	General-purpose/Linear ICs
IC12	Display Drivers and Microcontroller Peripherals
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-Bit Microcontrollers
IC15	FAST TTL Logic Series

INTEGRATED CIRCUITS (Continued)

IC16	ICs for Clocks and Watches
IC18	Semiconductors for In-car Electronics and General Industrial Applications
IC19	ICs for Data Communications
IC20	80C51-based 8-Bit Microcontrollers
IC21	68000-based 16-Bit Microcontrollers
IC22	ICs for Multi-media Systems
IC23	QUBiC Advanced BiCMOS Bus Interface Logic ABT MULTIBYTE™
IC24	Low Voltage CMOS Logic

DISCRETE SEMICONDUCTORS

SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small Signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10a	Surface Mounted Semiconductors
SC10b	Surface Mounted Semiconductors
SC12	Optocouplers
SC13	Power MOS Transistors
SC14	RF Wideband Transistors
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

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